Rockwell

Data Catalog

May, 1979

# MicroPower

## Microelectronic Devices
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May, 1979

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# Microelectronic Devices

Data Catalog

R6500 NMOS PRODUCTS

NMOS MEMORY PRODUCTS

PPS PMOS PRODUCTS

MICROMODEM MODULES

BUBBLE MEMORY PRODUCTS

FILTER PRODUCTS

TELECOM DEVICES

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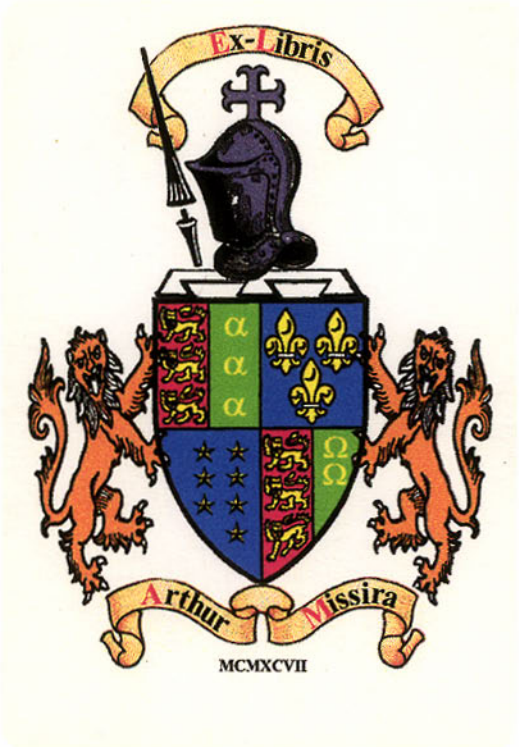
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## TABLE OF CONTENTS


**R6500 NMOS PRODUCTS**

**R6500 Family Brochure**

**R6500 CPUs & R6500/1**

R6500 CPUs
R6500B Series (3 MHz) CPUs
R6500/1 One Chip Microcomputer
R6500/1E Emulator Device
Clock Input (Application Note)

**R6500 I/O Devices**

R6520 Peripheral Interface Adapter (PIA)
R6522 Versatile Interface Adapter (VIA)
R6541 Programmable Keyboard/Display Controller (PKDC)
R6545 CRT Controller (CRTC)
R6551 Asynchonous Communication Interface Adapter (ACIA)

**R6500 Memory-I/O Combination Devices**

R6530 ROM-RAM-I/O-Timer (RRIOT)
R6531 ROM-RAM-I/O-Counter (RRIOC)
R6532 RAM-I/O-Timer (RIOT)
R6534 ROM-I/O-Counter (RIOC)

**R6500 Support Products**

AIM 65 Microcomputer

SYSTEM 65 Microcomputer Development System
M65-001, M65-002 USER 65 Option
M65-031, M65-032 16K Static RAM Module
M65-040 PROM Programmer Module
M65-045 PROM/ROM Module
M65-060 Extender Card
M65-070 Design Prototyping Module

PL/65 Compiler

**NMOS MEMORY PRODUCTS**

**RAM Memory Devices**

R2114 1024 x 4 Static RAM

**ROM Memory Devices**

R2316 2048 x 8 Static ROM
R2332 4096 x 8 Static ROM

**PPS PMOS PRODUCTS**

**PPS Family Brochure**

**PPS-4/1 One-Chip Microcomputers**

MM76 and MM76E
MM75
MM76C
MM76L and MM76EL
MM77 and MM78
MM77L and MM78L
Serial Communications Protocol for Multiple PPS-4/1 Systems (Application Note)

PPS-4/1 Prototyping with 2708 PROMs (Application Note)

XPO-1 Sytem Development Microcomputer

**MICROMODEM MODULES**

R24 2400 BPS Modular Modem

**BUBBLE MEMORY PRODUCTS**

Bubble Memory Brochure
RBM256 256K-Bit Bubble Memory Device
RLM658 1-Megabit Linear Bubble Memory Module

**ROCKWELL-COLLINS FILTER PRODUCTS**

Filter Products Flyer
Low Frequency Mechanical Filters Brochure
Surface Wave Acoustic Devices Brochure

**TELECOM DEVICES**

Telecommunication Products Flyer

CRC 8000, CRC 8001 Binary-to-Dial Pulse Dialer
CRC 8030 Dual Tone Multi-Frequency Detector
CRC 8030 Application Note
CRC 8030 Front-End Components

R8040 T-1 Tri-Port Memory
R8050 T-1 Serial Transmitter
R8060 T-1 Serial Receiver

# R6500
Family Brochure

# R6500

MICROCOMPUTER SYSTEM

R6500



Rockwell International

Printed in the U.S.A.

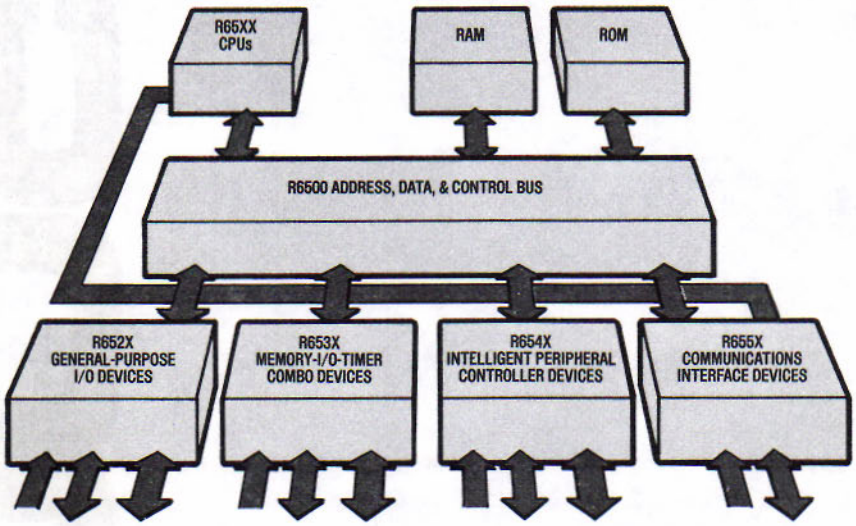
# The R6500 Family

## R6500 Family

A family of 10 software-compatible CPUs and 11 I/O, ROM, RAM and one-chip memory-I/O-timer circuits operating at proven 1 MHz and 2 MHz speeds with a single 5V power supply, provides you with economic system solutions for a broad range of applications.

The R6500/1 provides you with CPU, ROM, RAM, interrupts, counter and bi-directional data ports on a single chip. And it's totally software compatible with all other members of the R6500 family.

The R6500 promises you boosted performance and improved economics through its third generation architecture, which includes 13 powerful addressing modes, and its innovative circuit design and processing technology which reduce chip size and power consumption.




## Rockwell is solidly backing the R6500

Rockwell has dedicated facilities for the high volume manufacturing of R6500 circuits produced with its own depletion load, silicon-gate N-channel process.

And Rockwell provides complete system development support: Rockwell's SYSTEM 65, a floppy-disk based, powerful yet low-cost complete development system. Plus AIM 65, TIM or timesharing program, complete documentation and extensive applications engineering support.

For the future, Rockwell is developing new R6500 devices that will enhance your own product development opportunities.

Rockwell's R650X CPU options offer a selection of features in 40- and 28-pin versions to meet your system needs (see table below). The R6502 - R6507 Series has on-chip clock generation. The R6512 - R6515 Series allows the user to generate and control the clock externally.

## Why the R6500 is a cost performance winner

- Proven 1 MHz or 2 MHz performance
- Pipeline architecture for fast operation with fewer cycles
- Single 5-volt power supply
- On-the-chip clock or an external clock
- 56 instructions
- 13 addressing modes and true indexing capability
- Decimal/binary arithmetic mode selection
- Bi-directional Data Bus (compatible with the MC6800)
- Addressable memory range up to 65K bytes
- Multi-level interrupts – maskable/non-maskable
- Use with any type or speed memory
- Programmable stack pointer and variable length stack
- 40- and 28-pin DIP package options

## R6500 CPU Options

| | 40-Pin DIP | | 28-Pin DIP | | | | |
|---|---|---|---|---|---|---|---|
| | R6502 | R6512 | R6503<br>R6513 | R6504<br>R6514 | R6505<br>R6515 | R6506 | R6507 |
| Memory Address Space | 65K | 65K | 4K | 8K | 4K | 4K | 8K |
| Interrupts—Maskable<br>—Non-Maskable | Yes<br>Yes | Yes<br>Yes | Yes<br>Yes | Yes<br>No | Yes<br>No | Yes<br>No | No<br>No |
| SYNC—Output indicates op code fetch cycle | Yes | Yes | No | No | No | No | No |
| RDY—Single step and slow memory synchronization | Yes | Yes | No | No | Yes | No | Yes |
| $Ø_1$ Clock Output | Yes | Yes | No | No | No | Yes | No |
| DBE—Extended Data Bus Hold Time | No | Yes | No | No | No | No | No |

*The 40-pin versions provide full functional capability for memory intensive systems with extensive I/O requirements. The 28-pin versions offer flexibility in selecting the lowest cost CPU best suited to your application. 28-pin packages also provide denser board layout.*

## Thirteen addressing modes + true indexing = R6500 software power

The R6500 features 13 addressing modes. The first byte of each instruction is the operation code specifying both the instruction and the addressing mode. The addressing modes are summarized below.

- ACCUMULATOR ADDRESSING – A one byte instruction, operating on the accumulator.
- IMMEDIATE ADDRESSING – The operand is in the second byte of the instruction.
- ABSOLUTE ADDRESSING – The second and third bytes of the instruction specify the effective address in 65K bytes of addressable memory.
- ZERO PAGE ADDRESSING – Allows shorter code and execution times by assuming a zero page address.
- INDEXED ZERO PAGE ADDRESSING (X or Y, indexing.) – Zero page addressing used with an index register.
- INDEXED ABSOLUTE ADDRESSING (X or Y, indexing) – Absolute addressing used with X or Y index registers.
- IMPLIED ADDRESSING – The register containing the operand is implicitly stated in the operation code.
- RELATIVE ADDRESSING – Used only with branch instructions. The second byte is an "Offset" added to the contents of the program counter.
- INDEXED INDIRECT ADDRESSING – Uses an indirect zero page address indexed by X to fetch the effective address.
- INDIRECT INDEXED ADDRESSING – Uses a zero page address to fetch the effective base address to be indexed by Y.
- ABSOLUTE INDIRECT – Used only with JMP, the second and third bytes point to a two-byte effective address.

# R6500 Microprocessor Instruction Set

| | | Execution Time (clock cycles) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Accumulator | Immediate | Zero Page | Zero Page, X | Zero Page, Y | Absolute | Absolute, X | Absolute, Y | Implied | Relative | (Indirect, X) | (Indirect), Y | Absolute Indirect |
| ADC | Add Memory to Accumulator with Carry | • | 2 | 3 | 4 | • | 4 | 4* | 4* | • | • | 6 | 5* | • |
| AND | "AND" Memory with Accumulator | • | 2 | 3 | 4 | • | 4 | 4* | 4* | • | • | 6 | 5* | • |
| ASL | Shift Left One Bit (Memory or Accumulator) | 2 | • | 5 | 6 | • | 6 | 7 | • | • | • | • | • | • |
| BCC | Branch on Carry Clear | • | • | • | • | • | • | • | • | • | 2** | • | • | • |
| BCS | Branch on Carry Set | • | • | • | • | • | • | • | • | • | 2** | • | • | • |
| BEQ | Branch on Result Zero | • | • | • | • | • | • | • | • | • | 2** | • | • | • |
| BIT | Test Bits in Memory with Accumulator | • | • | 3 | • | • | 4 | • | • | • | • | • | • | • |
| BMI | Branch on Result Minus | • | • | • | • | • | • | • | • | • | 2** | • | • | • |
| BNE | Branch on Result not Zero | • | • | • | • | • | • | • | • | • | 2** | • | • | • |
| BPL | Branch on Result Plus | • | • | • | • | • | • | • | • | • | 2** | • | • | • |
| BRK | Force Break | • | • | • | • | • | • | • | • | • | • | • | • | • |
| BVC | Branch on Overflow Clear | • | • | • | • | • | • | • | • | • | 2** | • | • | • |
| BVS | Branch on Overflow Set | • | • | • | • | • | • | • | • | • | 2** | • | • | • |
| CLC | Clear Carry Flag | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| CLD | Clear Decimal Mode | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| CLI | Clear Interrupt Disable Bit | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| CLV | Clear Overflow Flag | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| CMP | Compare Memory and Accumulator | • | 2 | 3 | 4 | • | 4 | 4* | 4* | • | • | 6 | 5* | • |
| CPX | Compare Memory and Index X | • | 2 | 3 | • | • | 4 | • | • | • | • | • | • | • |
| CPY | Compare Memory and Index Y | • | 2 | 3 | • | • | 4 | • | • | • | • | • | • | • |
| DEC | Decrement Memory by One | • | • | 5 | 6 | • | 6 | 7 | • | • | • | • | • | • |
| DEX | Decrement Index X by One | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| DEY | Decrement Index Y by One | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| EOR | "Exclusive OR" Memory with Accumulator | • | 2 | 3 | 4 | • | 4 | 4* | 4* | • | • | 6 | 5 | • |
| INC | Increment Memory by One | • | • | 5 | 6 | • | 6 | 7 | • | • | • | • | • | • |
| INX | Increment Index X by One | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| INY | Increment Y by One | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| JMP | Jump to New Location | • | • | • | • | • | 3 | • | • | • | • | • | • | 5 |
| JSR | Jump to New Location saving Return Address | • | • | • | • | • | 6 | • | • | • | • | • | • | • |
| LDA | Load Accumulator with Memory | • | 2 | 3 | 4 | • | 4 | 4* | 4* | • | • | 6 | 5* | • |
| LDX | Load Index X with Memory | • | 2 | 3 | • | 4 | 4 | • | 4* | • | • | • | • | • |
| LDY | Load Index Y with Memory | • | 2 | 3 | 4 | • | 4 | 4* | • | • | • | • | • | • |
| LSR | Shift Right One Bit (Memory or Accumulator) | 2 | • | 5 | 6 | • | 6 | 7 | • | • | • | • | • | • |
| NOP | No Operation | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| ORA | "OR" Memory with Accumulator | • | 2 | 3 | 4 | • | 4 | 4* | 4* | • | • | 6 | 5* | • |
| PHA | Push Accumulator on Stack | • | • | • | • | • | • | • | • | 3 | • | • | • | • |
| PHP | Push Processor Status on Stack | • | • | • | • | • | • | • | • | 3 | • | • | • | • |
| PLA | Pull Accumulator from Stack | • | • | • | • | • | • | • | • | 4 | • | • | • | • |
| PLP | Pull Processor Status from Stack | • | • | • | • | • | • | • | • | 4 | • | • | • | • |
| ROL | Rotate One Bit Left (Memory or Accumulator) | 2 | • | 5 | 6 | • | 6 | 7 | • | • | • | • | • | • |
| ROR | Rotate One Bit Right (Memory or Accumulator) | 2 | • | 5 | 6 | • | 6 | 7 | • | • | • | • | • | • |
| RTI | Return from Interrupt | • | • | • | • | • | • | • | • | 6 | • | • | • | • |
| RTS | Return from Subroutine | • | • | • | • | • | • | • | • | 6 | • | • | • | • |
| SBC | Subtract Memory from Accumulator with Borrow | • | 2 | 3 | 4 | • | 4 | 4* | 4* | • | • | 6 | 5* | • |
| SEC | Set Carry Flag | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| SED | Set Decimal Mode | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| SEI | Set Interrupt Disable Status | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| STA | Store Accumulator in Memory | • | • | 3 | 4 | • | 4 | 5 | 5 | • | • | 6 | 6 | • |
| STX | Store Index X in Memory | • | • | 3 | • | 4 | 4 | • | • | • | • | • | • | • |
| STY | Store Index Y in Memory | • | • | 3 | 4 | • | 4 | • | • | • | • | • | • | • |
| TAX | Transfer Accumulator to Index X | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| TAY | Transfer Accumulator to Index Y | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| TSX | Transfer Stack Pointer to Index X | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| TXA | Transfer Index X to Accumulator | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| TXS | Transfer Index X to Stack Pointer | • | • | • | • | • | • | • | • | 2 | • | • | • | • |
| TYA | Transfer Index Y to Accumulator | • | • | • | • | • | • | • | • | 2 | • | • | • | • |

*Add one cycle if indexing across page boundary
**Add one cycle if branch is taken, and one additional cycle if branching operatic crosses page boundary

# R6500/1 One-Chip Microcomputer

## The R6500/1

In the R6500/1, Rockwell has combined the high-performance R6502 CPU with such versatile features as 2048 bytes of ROM, 64 bytes of RAM, 32 bi-directional I/O lines, four interrupts and a 16-bit programmable counter (with four separate interval/event modes) — all in a single 40-pin package.

The R6500/1 also has on-the-chip 1 MHz or 2 MHz clock operation with external single clock, crystal or RC frequency input.

The R6500/1 includes a separate power pin that maintains RAM on 10% of the operating power. In the event power is lost, this standby power retains RAM data until execution is resumed.

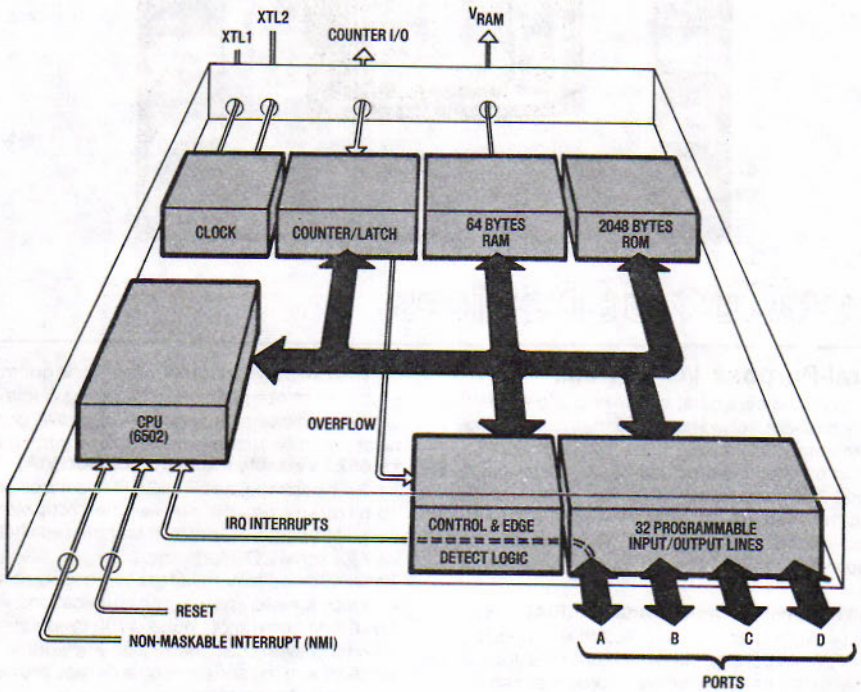
Rockwell backs up the R6500/1 with solid system development support in two ways:

The R6500/1E, a 64-pin emulator device with 40 pins electrically identical to the R6500/1, may be used for program development and prototyping with external EPROM or RAM.

A Personality option to SYSTEM 65 customizes Rockwell's popular microcomputer development system for complete R6500/1 software and hardware development.

## R6500/1 Features

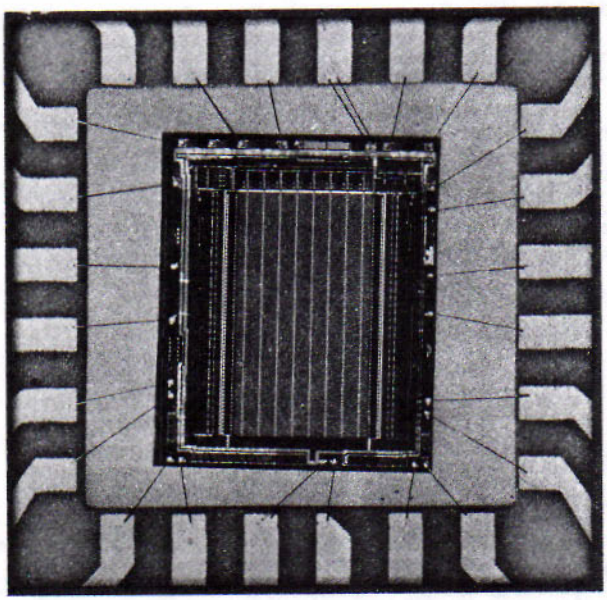
- 2K-Byte Mask Programmable ROM
- 64-Byte Static RAM
- R6502 CPU
- Four 8-Bit Bidirectional I/O Ports
- 16-Bit Programmable Counter/Latch With Four Modes:
  - — Interval Timer
  - — Pulse Generator
  - — Event Counter
  - — Pulse Width Measurement
- Five Interrupts
- Fully Upward/Downward Compatible With 6500 Family
- 64-Pin PROM-compatible Emulator Device Available



# Standard Memory Devices

The R6500 system bus enables you to use low cost, widely available standard memory devices. For your convenience, Rockwell now offers the five memory devices, described below. All are completely TTL compatible, fully static — no clocks or refresh strobes required — and operate from a single + 5 V power supply

- **R2114 4K STATIC RAM**
  1024 x 4 in high-density 18-pin package with common data I/O; 450ns access and cycle time; fully static — no clocks or strobes required; single + 5V power supply; total TTL compatibility. (Industry standard.)
- **R2316B 16K STATIC ROM**
  2048 x 8 in standard 24-pin package; pin-compatible with 2708 EPROM; 450 ns. max. cycle time; three chip selects. (Industry standard; replaces *two* 8K EPROMs.)
- **R2332 32K STATIC ROM**
  The industry's first static 4096 x 8 N-channel ROM; standard 24-pin package; 450 ns. max. cycle time; two chip selects.
- **R2332-3 32K STATIC ROM**
  Same as R2332, but has 300 ns. max. cycle time.



# Input/Output Devices

## General-Purpose I/O Devices

These versatile peripheral controllers allow effective trade-offs between software and hardware, enabling implementation of complex R6500 microcomputer systems at minimum overall cost. Both are available in 1 MHz and 2 MHz versions. All R6500 I/O devices—including the memory-I/O combos—have TTL and CMOS compatible peripheral lines with transistor drive capability and high-impedance, tri-state data outputs.

- **R6520 Peripheral Interface Adapter (PIA)**
  40-pin package, two 8-bit bi-directional I/O ports, four peripheral control/interrupt input lines, fully automatic data transfers between processor and peripheral devices.

The PIA provides individual I/O line control for keyboard strobes and returns, driving displays and discrete indicators as well as 8-bit parallel communications in *handshake* or clocked control modes.

- **R6522 Versatile Interface Adapter (VIA)**
  40-pin package, has R6520 PIA features plus two 16-bit programmable interval timers/counters, data latching on I/O ports, 8-bit buffered shift register for serial I/O interfacing.
  The enhanced features of the VIA provide a serial interface for inter-system communications, ASCII serial data generation, pulse width modulation, and waveform synthesis. The two timers work in conjunction with the serial channel or may provide interval timing for real time applications.

## Memory-I/O-Timer Combination Devices

By combining an R650X Series CPU with one-chip memory, I/O and timer combination devices, the designer nets a powerful, cost-effective two chip microcomputer system which can also be the base configuration for modular, expandable applications.

- **R6530 ROM-RAM-I/O-Timer (RRIOT)**
  40-pin package; 1 MHz operation; 1024 x 8 ROM; 64 x 8 static RAM; two 8-bit bi-directional data I/O ports; two progammable data direction registers; programmable 8-bit interval timer with prescale and interrupt control.
- **R6531 ROM-RAM-I/O-Counter (RRIOC)**
  40-pin package; 1 MHz or 2 MHz operation; 2048 x 8 ROM; 128 x 8 static RAM; 8-bit serial data channel; two bi-directional I/O ports, with a total of 15 data lines, including four external interrupts and handshake control.

  The RRIOC also provides a fully-buffered 16-bit counter/timer with four program selectable modes — interval timer, pulse generator, event counter and pulse width measurement.

  A separate 52-pin version of RRIOC offers expanded I/O in additional 8-bit output port and 4-bit input port.
- **R6532 RAM-I/O-Timer (RIOT)**
  40-pin package; 1 MHz operation; 128 x 8 static RAM; two 8-bit bi-directional data ports; two programmable data direction registers; programmable 8-bit interval timer with prescale and interrupt control; programmable edge detect interrupt, for fast service of critical events.
- **R6534 ROM-I/O-Counter (RIOC)**
  40-pin package; 1 MHz operation; 4096 x 8 ROM; 8-bit serial data channel; two bi-directional data I/O ports, with a total of 14 data lines, including four external interrupts and handshake control.

  The RIOC also provides a programmable 16-bit counter/latch with interval timer, pulse generator and event counter modes.

  A separate 52-pin version of RIOC offers an additional 8-bit output port, 3-bit input port and one additional I/O line.

## Intelligent Peripheral Controller Devices

The devices listed below get your interface design off to a solid start.

- **R6541 Programmable Keyboard/Display Controller (PKDC)**
  40-pin package, 8-character FIFO/Sensor RAM for keyboard entries, two CPU-addressable 16-byte display RAMs.

  The PKDC is a general-purpose keyboard and segmented display interface device. The keyboard portion can scan up to 128 matrix-type key switches, and can also interface with an array of 64 sensors or a strobed interface keyboard. The display portion provides a buffered scanned display interface with LED, fluorescent, Borroughs SELF-SCAN®, and other display technologies.
- **R6545 CRT Controller (CRTC)**
  40-pin package, refresh RAM, fully-programmable scanning and cursor, light pen register.

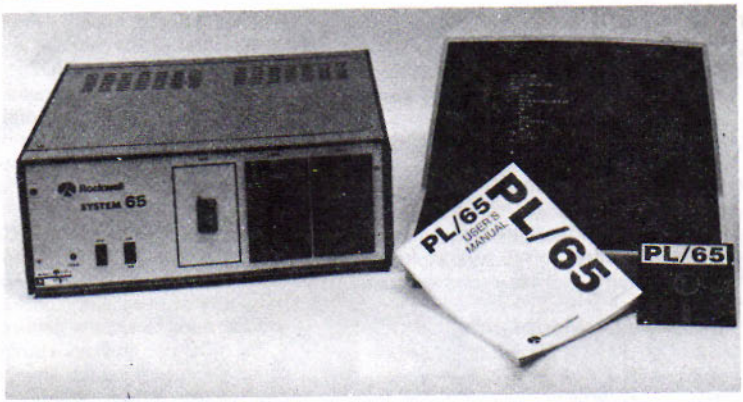
  The CRTC is designed to interface an 8-bit microprocessor to CRT raster scan video displays. It provides refresh memory addresses and character generator row addresses, which allow up to 16K characters with 32 scan lines per character to be addressed. Refresh memory may be addressed in either straight binary or by row/column.

## Communications Interface Device

- **R6551 Asynchronous Communication Interface Adapter (ACIA)**
  28-pin package provides the interface between R6500-based systems and serial communication data sets and modems. With its on-chip baud rate generator, the ACIA is capable of transmitting at 15 different program-selectable rates between 50 baud and 19,200 baud, and receiving at either the transmit rate or at 16X an external clock rate.

  The ACIA has programmable word lengths of 5, 6, 7 or 8 bits; even, odd or no parity; 1, 1-1/2 or 2 stop bits.

# Product Development




## Rockwell's SYSTEM 65

SYSTEM 65 is a new easy to use, powerful, complete development system for the R6500 family of microcomputers. The basic configuration includes two built-in, mini-floppy disk drives, 16K bytes of user memory and 16K bytes of resident operating system.

Monitor commands are self-prompting whenever memory, peripheral, or disk file assignment is required. Text editor provides line, string, and character editing functions. A resident two-pass assembler and dynamic debug package complete the operating system. Both source and object code may be maintained in memory for fast editing, assembling, and checkout. Since the total monitor, editor, debug and assembler are resident in ROM, 100% of the disk storage and drive utilization is available to the user.

The mini-floppy diskettes may be used as storage for source and object code and documentation. Each diskette has the capacity for 78K bytes of information in a maximum of 60 files.

SYSTEM 65 supports a vareity of terminals with serial data from 100 baud to 9600 baud. Connectors are provided for both RS-232 C and current loop interfacing. Reader ON/OFF signals and RTS/CTS control signals are standard. Included is a parallel port providing automatic control to high speed printers, such as Diablo, Centronics and Tally.

### And Rockwell offers these options to SYSTEM 65:

- PL/65 High-Level Language
- USER 65 in-circuit emulation option
- PROM Programmer Module, for programming a 2704/2708/2716/2758 PROM device from the front panel socket
- R6500/1 Personality option, for developing with the R6500/1 single-chip microcomputer
- 16K x 8 Static RAM Modules
- PROM/ROM Module, accepts 2316/2332 ROM or 2708/2716/2758 PROM devices
- Wire-wrap Design Prototyping Module
- Extender Card for circuit probing

## PL/65 High-Level Language

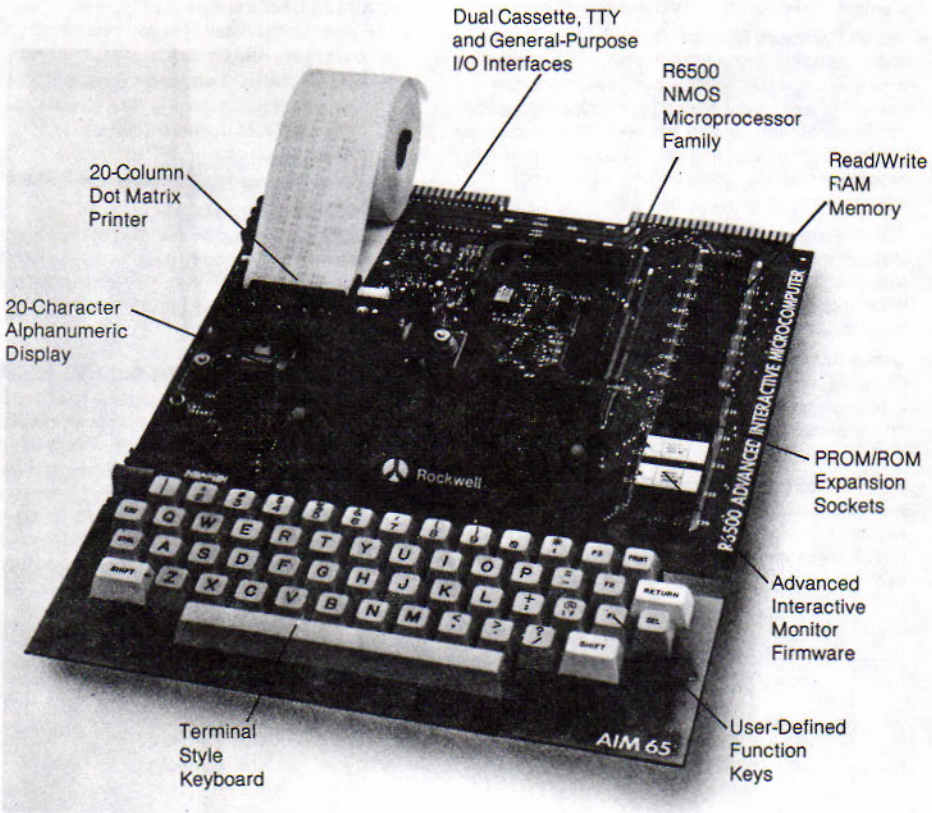
A high-level language resembling PL/1 and ALGOL is now available to designers developing programs for the R6500 microprocessor family using the SYSTEM 65 development system.

Designated PL/65, the language is considerably easier to use than assembly language or object code, thus increasing programmer productivity while reducing software development time and costs. The PL/65 compiler outputs source code to the SYSTEM 65's resident assembler. This permits enhancing or debugging at the assembler level before object code is generated. In addition, PL/65 statements may be mixed with assembly language instructions for timing or code optimization.

The PL/65 compiler is available to SYSTEM 65 users as a preprogrammed mini-floppy diskette. No additional memory is required other than the standard 16K bytes of RAM.

The PL/65 language supports modular program design. Its general control structures for conditional and iterative looping allow the language to be used effectively for structured programs. Other language features include: assignment, integer arithmetic, conditional execution, collective execution, linear array manipulation, data area declaration and array initialization. Block structures, subscripts and parenthetical expressions are also supported.

# For learning, designing, work or just plain fun. . . .




Rockwell's R6500 Advanced Interactive Microcomputer (AIM 65) can get you into the exciting world of microcomputers a lot easier and at a lot lower cost than you may have thought possible.

As a learning aid, AIM 65 gives you an assembled, tested and warranted R6502-based microcomputer system with a full-sized keyboard, an alphanumeric 20-character display and, uniquely, an alphanumeric 20-column thermal printer.

An on-board Advanced Interactive Monitor program provides extensive control and program development functions. You'll be writing your programs in assembly language — there's no need to memorize "opcodes". And for more specialized applications, we offer a two-pass, symbolic assembler and a BASIC interpreter as plug-in ROM options.

You'll master fundamentals rapidly. Then you'll appreciate the fact that unlike the computer "toys" on the market, AIM 65 offers flexibility and expandability you would expect to find only in a sophisticated microcomputer development system.

# Literature

## How to make it all work for you

Rockwell has put together a complete set of documentation and reference manuals to help you implement the R6500 microprocessor family.

- **R6500 Hardware Manual**
  A detailed description of each chip in the family, how they interface, how the peripherals are controlled, as well as the design techniques facilitating system operation, testing and maintenance. Special emphasis is on "bringing up" a system with testing techniques, scope synchronizing and general trouble-shooting procedures — $5.
- **R6500 Programming Manual**
  Defines the architecture of the R6500 Series, the function of each instruction and valuable programming information. Special emphasis is on the sophisticated addressing modes of the family — $5.
- **Cross-Assembler Manual**
  Cross-Assembler directives are described as used in time-share and batch operations, with special aids on understanding and resolving error messages — $5.
- **SYSTEM 65 User's Manual**
  Instructs the user in operating the SYSTEM 65 Microcomputer Development System and its application in developing a working microprocessor system — $5.
- **PL/65 User's Manual**
  A complete guide to PL/65, the high-level language for the R6500 family — $10.
- **AIM 65 User's Guide**
  Full technical details tell you everything you need to operate the AIM 65 — $5.
- **AIM 65 BASIC Language Reference Manual**
  A how-to guide for using AIM 65 with the BASIC language ROM option installed—$5.
- **TIM Manual**
  Defines how to apply the Teletype I/O Monitor — $2.
- **R6500 Data Sheets**
  Provides quick understanding of the capabilities and characteristics of each available R6500 device and support equipment. To order data sheets simply specify the part number or the name of the support equipment.

## Where to get more on the R6500

Rockwell's normal procedure is to provide you with free data sheets so that you can select the R6500 devices and support equipment of most interest to you. A nominal charge is made for reference manuals.

For data, devices or support equipment contact the nearest Rockwell office or distributor listed on the back page of this brochure. For in-depth assistance, obtain the name of your nearest Rockwell sales representative from any Rockwell office.

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REV. 3, FEBRUARY 1979

PART NUMBER
R650X and R651X

Rockwell

# R6500 Microcomputer System DATA SHEET





## R6500 MICROPROCESSORS (CPU's)

### SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-Channel, Silicon Gate technology. Its performance speeds are enhanced by advanced system architecture. This innovative architecture results in smaller chips — the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, described in this document. Rockwell also provides memory and microcomputer system . . . as well as low-cost design aids and documentation.

### R6500 MICROPROCESSOR (CPU) CONCEPT

Ten CPU devices are available. All are software-compatible. They provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. All are bus-compatible with earlier generation microprocessors like the M6800 devices.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for multiprocessor system applications where maximum timing control is mandatory. All R6500 microprocessors are also available in a variety of packaging (ceramic and plastic), operating frequency (1 MHz and 2 MHz) and temperature (commercial, industrial and military) versions.

### MEMBERS OF THE R6500 MICROPROCESSOR (CPU) FAMILY

Microprocessors with On-Chip Clock Oscillator

| Model | Addressable Memory |
|---|---|
| R6502 | 65K Bytes |
| R6503 | 4K Bytes |
| R6504 | 8K Bytes |
| R6505 | 4K Bytes |
| R6506 | 4K Bytes |
| R6507 | 8K Bytes |

Microprocessors with External Two Phase Clock Output

| Model | Addressable Memory |
|---|---|
| R6512 | 65K Bytes |
| R6513 | 4K Bytes |
| R6514 | 8K Bytes |
| R6515 | 4K Bytes |

### FEATURES

- Single +5V supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type of speed memory
- 8-bit Bidirectional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input
- Direct Memory Access capability
- Bus compatible with M6800
- 1 MHz and 2 MHz operation
- Choice of external or on-chip clocks
- On-the-chip clock options
  - External single clock input
  - RC time base input
  - Crystal time base input
- Commercial, industrial and military temperature versions
- Pipeline architecture

### Ordering Information

**Order Number:** R65XX___

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = -40°C to +85°C (Industrial)
  - MT = -55°C to +125°C (Military)
  - M = MIL-STD-883, Class B
- Package:
  - C = Ceramic
  - P = Plastic (Not Avaible for M or MT suffix)
- Frequency Range:
  - No suffix = 1 MHz
  - A = 2 MHz
- Model Designator:
  - XX = 02, 03, 04, ... 15

**NOTE:** Contact your local Rockwell Representative concerning availability.

## R6500 Signal Description

**Clocks ($\phi_1$, $\phi_2$)**

The R651X requires a two phase non-overlapping clock that runs at the $V_{CC}$ voltage level.

The R650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

**Address Bus (A0-A15)**

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

**Data Bus (D0-D7)**

Eight pins are used for the data bus. This is a bidirectional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pF.

**Data Bus Enable (DBE)**

This TTL compatible input allows external control of the tri-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two ($\phi_2$) clock, thus allowing data output from microprocessor only during $\phi_2$. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

**Ready (RDY)**

This input signal allows the user to halt or single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one ($\phi_1$) will halt the microprocessor with the output address lines reflecting the current address being fetched. If Ready is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent phase two ($\phi_2$) in which the Ready signal is low. This feature allows microprocessor interfacing with the low speed PROMs as well as fast (max. 2 cycle) Direct Memory Access (DMA).

**Interrupt Request ($\overline{IRQ}$)**

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3KΩ external resistor should be used for proper wire-OR operation.

**Non-Maskable Interrupt ($\overline{NMI}$)**

A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the state interrupt mask flag. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3KΩ register to $V_{CC}$ for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupts lines that are sampled during $\phi_2$ (phase 2) and will begin the appropriate interrupt routine on the $\phi_1$ (phase 1) following the completion of the current instruction.

**Set Overflow Flag (S.O.)**

A negative going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of $\phi_1$ and must be externally synchronized.

**SYNC**

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\phi_1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\phi_1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

**Reset**

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After $V_{CC}$ reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

## ADDRESSING MODES

**ACCUMULATOR ADDRESSING** – This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

**IMMEDIATE ADDRESSING** – In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

**ABSOLUTE ADDRESSING** – In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

**ZERO PAGE ADDRESSING** – The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

**INDEXED ZERO PAGE ADDRESSING** – (X, Y indexing) – This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

**INDEXED ABSOLUTE ADDRESSING** – (X, Y indexing) – This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

**IMPLIED ADDRESSING** – In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

**RELATIVE ADDRESSING** – Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

**INDEXED INDIRECT ADDRESSING** – In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

**INDIRECT INDEXED ADDRESSING** – In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

**ABSOLUTE INDIRECT** – The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

## INSTRUCTION SET – ALPHABETIC SEQUENCE

ADC Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift left One Bit (Memory or Accumulator)

BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Bits in Memory with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set

CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y

DEC Decrement Memory by One
DEX Decrement Index X by One
DEY Decrement Index Y by One

EOR "Exclusive-or" Memory with Accumulator

INC Increment Memory by One
INX Increment Index X by One
INY Increment Index Y by One

JMP Jump to New Location
JSR Jump to New Location Saving Return Address

LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right (Memory or Accumulator)

NOP No Operation

ORA "OR" Memory with Accumulator

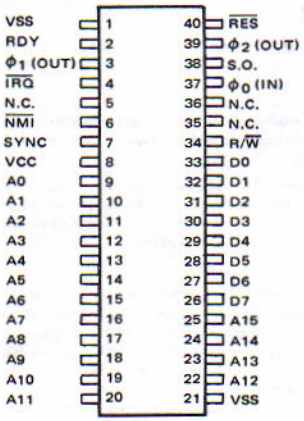
PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack

ROL Rotate One Bit Left (Memory or Accumulator)
ROR Rotate One Bit Right (Memory or Accumulator)
RTI Return from Interrupt
RTS Return from Subroutine

SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Status
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory

TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Register
TYA Transfer Index Y to Accumulator

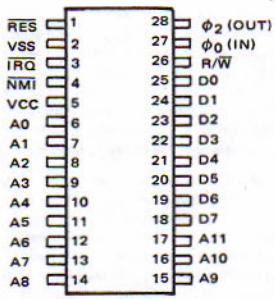
## R6502 — 40 Pin Package




### Features of R6502

- 65K Addressable Bytes of Memory (A0-A15)
- IRQ Interrupt
- On-the-chip Clock
  - TTL Level Single Phase Input
  - RC Time Base Input
  - Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- NMI Interrupt

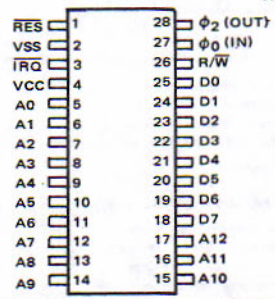
## R6503 — 28 Pin Package




### Features of R6503

- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- IRQ Interrupt
- NMI Interrupt
- 8 Bit Bidirectional Data Bus

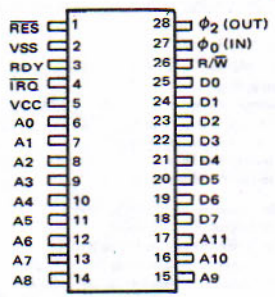
## R6504 — 28 Pin Package




### Features of R6504

- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- IRQ Interrupt
- 8 Bit Bidirectional Data Bus

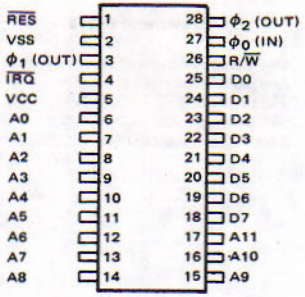
## R6505 — 28 Pin Package




### Features of R6505

- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- IRQ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus

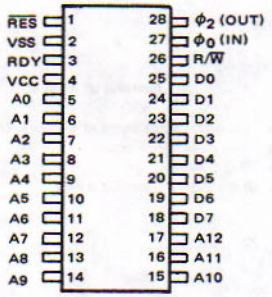
## R6506 – 28 Pin Package




### Features of R6506

- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- IRQ Interrupt
- Two phase output clock for timing of support chips
- 8 Bit Bidirectional Data Bus

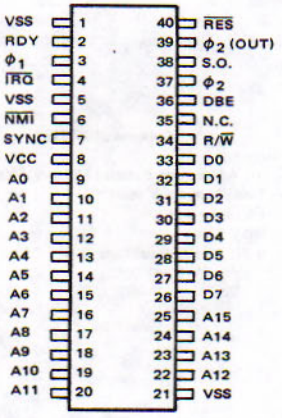
## R6507 – 28 Pin Package




### Features of R6507

- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- RDY Signal
- 8 Bit Bidirectional Data Bus

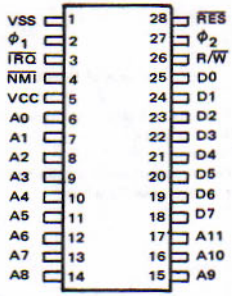
## R6512 – 40 Pin Package




### Features of R6512

- 65K Addressable Bytes of Memory (A0-A15)
- IRQ Interrupt
- NMI Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus
- SYNC Signal
- Two phase clock input
- Data Bus Enable

## R6513 – 28 Pin Package




### Features of R6513

- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- 8 Bit Bidirectional Data Bus

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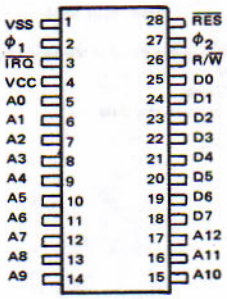
## R6514 – 28 Pin Package




### Features of R6514

- 8K Addressable Bytes of Memory (A0-A12)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- 8 Bit Bidirectional Data Bus

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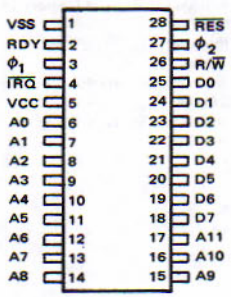
## R6515 – 28 Pin Package




### Features of R6515

- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- $\overline{IRQ}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus

# INSTRUCTION SET

| INSTRUCTIONS | | IMMEDIATE | | | ABSOLUTE | | | ZERO PAGE | | | ACCUM | | | IMPLIED | | | (IND, X) | | | (IND), Y | | | Z. PAGE, X | | | ABS. X | | | ABS. Y | | | RELATIVE | | | INDIRECT | | | Z. PAGE, Y | | | PROCESSOR STATUS CODES | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 7 6 5 4 3 2 1 0 | |
| MNEMONIC | OPERATION | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | N V - B D I Z C | MNEMONIC |
| ADC | A + M + C → A (4) (1) | 69 | 2 | 2 | 6D | 4 | 3 | 65 | 3 | 2 | | | | | | | 61 | 6 | 2 | 71 | 5 | 2 | 75 | 4 | 2 | 7D | 4 | 3 | 79 | 4 | 3 | | | | | | | | | | N V • • • • Z C | ADC |
| AND | A∧M → A (1) | 29 | 2 | 2 | 2D | 4 | 3 | 25 | 3 | 2 | | | | | | | 21 | 6 | 2 | 31 | 5 | 2 | 35 | 4 | 2 | 3D | 4 | 3 | 39 | 4 | 3 | | | | | | | | | | N • • • • • Z • | AND |
| ASL | C ← 7 6 5 4 3 2 1 0 ← 0 | | | | 0E | 6 | 3 | 06 | 5 | 2 | 0A | 2 | 1 | | | | | | | | | | 16 | 6 | 2 | 1E | 7 | 3 | | | | | | | | | | | | | N • • • • • Z C | ASL |
| BCC | BRANCH ON C = 0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 90 | 2 | 2 | | | | | | | • • • • • • • • | BCC |
| BCS | BRANCH ON C = 1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B0 | 2 | 2 | | | | | | | • • • • • • • • | BCS |
| BEQ | BRANCH ON Z = 1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | F0 | 2 | 2 | | | | | | | • • • • • • • • | BEQ |
| BIT | A∧M | | | | 2C | 4 | 3 | 24 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | $M_7$ $M_6$ • • • • Z • | BIT |
| BMI | BRANCH ON N = 1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 30 | 2 | 2 | | | | | | | • • • • • • • • | BMI |
| BNE | BRANCH ON Z = 0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D0 | 2 | 2 | | | | | | | • • • • • • • • | BNE |
| BPL | BRANCH ON N = 0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 10 | 2 | 2 | | | | | | | • • • • • • • • | BPL |
| BRK | BREAK | | | | | | | | | | | | | 00 | 7 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • 1 • • • | BRK |
| BVC | BRANCH ON V = 0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 50 | 2 | 2 | | | | | | | • • • • • • • • | BVC |
| BVS | BRANCH ON V = 1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 70 | 2 | 2 | | | | | | | • • • • • • • • | BVS |
| CLC | 0 → C | | | | | | | | | | | | | 18 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • 0 | CLC |
| CLD | 0 → D | | | | | | | | | | | | | D8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • 0 • • • | CLD |
| CLI | 0 → I | | | | | | | | | | | | | 58 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • 0 • • | CLI |
| CLV | 0 → V | | | | | | | | | | | | | B8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • 0 • • • • • • | CLV |
| CMP | A - M | C9 | 2 | 2 | CD | 4 | 3 | C5 | 3 | 2 | | | | | | | C1 | 6 | 2 | D1 | 5 | 2 | D5 | 4 | 2 | DD | 4 | 3 | D9 | 4 | 3 | | | | | | | | | | N • • • • • Z C | CMP |
| CPX | X - M | E0 | 2 | 2 | EC | 4 | 3 | E4 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z C | CPX |
| CPY | Y - M | C0 | 2 | 2 | CC | 4 | 3 | C4 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z C | CPY |
| DEC | M - 1 → M | | | | CE | 6 | 3 | C6 | 5 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | DEC |
| DEX | X - 1 → X | | | | | | | | | | | | | CA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | DEX |
| DEY | Y - 1 → Y | | | | | | | | | | | | | 88 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | DEY |
| EOR | A ∨ M → A (1) | 49 | 2 | 2 | 4D | 4 | 3 | 45 | 3 | 2 | | | | | | | 41 | 6 | 2 | 51 | 5 | 2 | 55 | 4 | 2 | 5D | 4 | 3 | 59 | 4 | 3 | | | | | | | | | | N • • • • • Z • | EOR |
| INC | M + 1 → M | | | | EE | 6 | 3 | E6 | 5 | 2 | | | | | | | | | | | | | F6 | 6 | 2 | FE | 7 | 3 | | | | | | | | | | | | | N • • • • • Z • | INC |
| INX | X + 1 → X | | | | | | | | | | | | | E8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | INX |
| INY | Y + 1 → Y | | | | | | | | | | | | | C8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | INY |
| JMP | JUMP TO NEW LOC | | | | 4C | 3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | 6C | 5 | 3 | | | | • • • • • • • • | JMP |
| JSR | JUMP SUB | | | | 20 | 6 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | JSR |
| LDA | M → A (1) | A9 | 2 | 2 | AD | 4 | 3 | A5 | 3 | 2 | | | | | | | A1 | 6 | 2 | B1 | 5 | 2 | B5 | 4 | 2 | BD | 4 | 3 | B9 | 4 | 3 | | | | | | | | | | N • • • • • Z • | LDA |
| LDX | M → X (1) | A2 | 2 | 2 | AE | 4 | 3 | A6 | 3 | 2 | | | | | | | | | | | | | | | | | | | BE | 4 | 3 | | | | | | | B6 | 4 | 2 | N • • • • • Z • | LDX |
| LDY | M → Y (1) | A0 | 2 | 2 | AC | 4 | 3 | A4 | 3 | 2 | | | | | | | | | | | | | B4 | 4 | 2 | BC | 4 | 3 | | | | | | | | | | | | | N • • • • • Z • | LDY |
| LSR | 0 → 7 6 5 4 3 2 1 0 → C | | | | 4E | 6 | 3 | 46 | 5 | 2 | 4A | 2 | 1 | | | | | | | | | | 56 | 6 | 2 | 5E | 7 | 3 | | | | | | | | | | | | | 0 • • • • • Z C | LSR |
| NOP | NO OPERATION | | | | | | | | | | | | | EA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | NOP |
| ORA | A ∨ M → A | 09 | 2 | 2 | 0D | 4 | 3 | 05 | 3 | 2 | | | | | | | 01 | 6 | 2 | 11 | 5 | 2 | 15 | 4 | 2 | 1D | 4 | 3 | 19 | 4 | 3 | | | | | | | | | | N • • • • • Z • | ORA |
| PHA | A → Ms S - 1 → S | | | | | | | | | | | | | 48 | 3 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | PHA |
| PHP | P → Ms S - 1 → S | | | | | | | | | | | | | 08 | 3 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | PHP |
| PLA | S + 1 → S Ms → A | | | | | | | | | | | | | 68 | 4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | PLA |
| PLP | S + 1 → S Ms → P | | | | | | | | | | | | | 28 | 4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | (RESTORED) | PLP |
| ROL | 7 6 5 4 3 2 1 0 ← C | | | | 2E | 6 | 3 | 26 | 5 | 2 | 2A | 2 | 1 | | | | | | | | | | 36 | 6 | 2 | 3E | 7 | 3 | | | | | | | | | | | | | N • • • • • Z C | ROL |
| ROR | C → 7 6 5 4 3 2 1 0 | | | | 6E | 6 | 3 | 66 | 5 | 2 | 6A | 2 | 1 | | | | | | | | | | 76 | 6 | 2 | 7E | 7 | 3 | | | | | | | | | | | | | N • • • • • Z C | ROR |
| RTI | RTRN INT | | | | | | | | | | | | | 40 | 6 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | (RESTORED) | RTI |
| RTS | RTRN SUB | | | | | | | | | | | | | 60 | 6 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | RTS |
| SBC | A - M - C̄ → A (1) | E9 | 2 | 2 | ED | 4 | 3 | E5 | 3 | 2 | | | | | | | E1 | 6 | 2 | F1 | 5 | 2 | F5 | 4 | 2 | FD | 4 | 3 | F9 | 4 | 3 | | | | | | | | | | N V • • • • Z (3) | SBC |
| SEC | 1 → C | | | | | | | | | | | | | 38 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • 1 | SEC |
| SED | 1 → D | | | | | | | | | | | | | F8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • 1 • • • | SED |
| SEI | 1 → I | | | | | | | | | | | | | 78 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • 1 • • | SEI |
| STA | A → M | | | | 8D | 4 | 3 | 85 | 3 | 2 | | | | | | | 81 | 6 | 2 | 91 | 6 | 2 | 95 | 4 | 2 | 9D | 5 | 3 | 99 | 5 | 3 | | | | | | | | | | • • • • • • • • | STA |
| STX | X → M | | | | 8E | 4 | 3 | 86 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | STX |
| STY | Y → M | | | | 8C | 4 | 3 | 84 | 3 | 2 | | | | | | | | | | | | | 94 | 4 | 2 | | | | | | | | | | | | | | | | | • • • • • • • • | STY |
| TAX | A → X | | | | | | | | | | | | | AA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | TAX |
| TAY | A → Y | | | | | | | | | | | | | A8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | TAY |
| TSX | S → X | | | | | | | | | | | | | BA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | TSX |
| TXA | X → A | | | | | | | | | | | | | 8A | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | TXA |
| TXS | X → S | | | | | | | | | | | | | 9A | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | TXS |
| TYA | Y → A | | | | | | | | | | | | | 98 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | TYA |

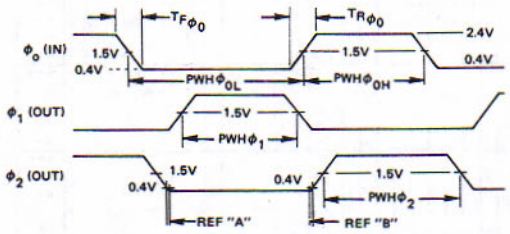
(1) ADD 1 to "N" IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT = BORROW
(4) IF IN DECIMAL MODE, Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

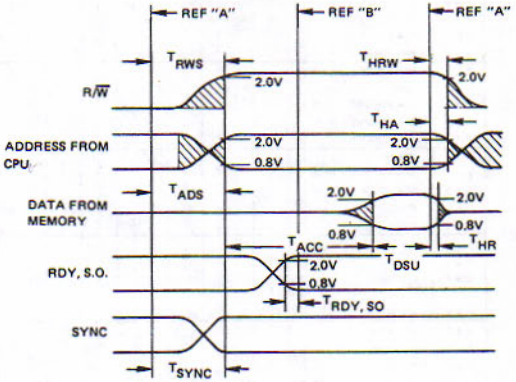
+ ADD
- SUBTRACT
∧ AND
∨ OR
∨ EXCLUSIVE OR

$M_7$ MEMORY BIT 7
$M_6$ MEMORY BIT 6
n NO. CYCLES
# NO. BYTES

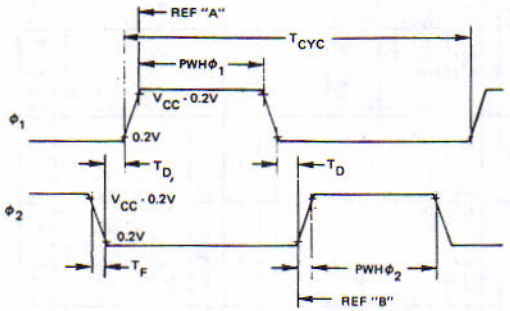
### Clock Timing – R6502, 03, 04, 05, 06, 07



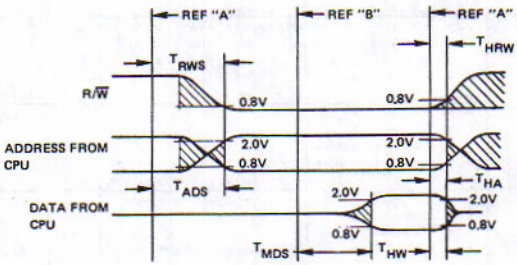

### Timing for Reading Data from Memory or Peripherals




### Clock Timing – R6512, 13, 14, 15

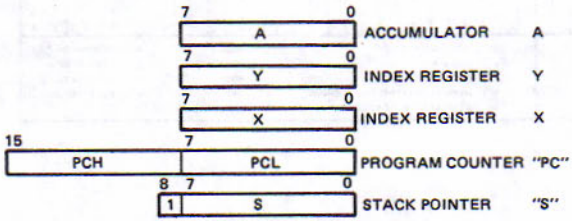


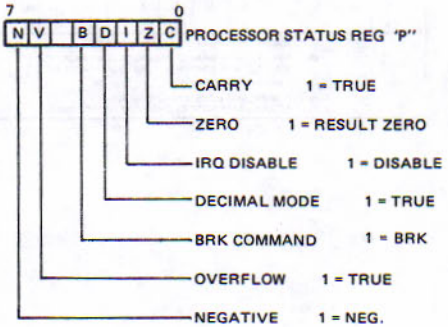

### Timing for Writing Data to Memory or Peripherals




**Note: "REF." means Reference Points on clocks.**

## PROGRAMMING MODEL



## 1 MHz Timing

### Clock Timing – R6502, 03, 04, 05, 06, 07

| Characteristic | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Cycle Time | $T_{CYC}$ | 1.0 | – | 10.0 | µs |
| $\phi_{0(IN)}$ Pulse Width (measured at 1.5V) | $PWH\phi_0$ | 460 | – | 520 | ns |
| $\phi_{0(IN)}$ Rise, Fall Time | $TR\phi_0$, $TF\phi_0$ | – | – | 10 | ns |
| Delay Time Between Clocks (measured at 1.5V) | $T_D$ | 5 | – | – | ns |
| $\phi_{1(OUT)}$ Pulse Width (measured at 1.5V) | $PWH\phi_1$ | $PWH\phi_{0L}$-20 | – | $PWH\phi_{0L}$ | ns |
| $\phi_{2(OUT)}$ Pulse Width (measured at 1.5V) | $PWH\phi_2$ | $PWH\phi_{0H}$-40 | – | $PWH\phi_{0H}$-10 | ns |
| $\phi_{1(OUT)}$, $\phi_{2(OUT)}$ Rise, Fall Time (measured at 0.8V to 2.0V) (Load = 130 pF + 1 TTL) | $T_R$, $T_F$ | – | – | 25 | ns |

### Clock Timing – R6512, 13, 14, 15

| Characteristic | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Cycle Time | $T_{CYC}$ * | 1000 | – | – | ns |
| Clock Pulse Width (Measured at Vcc - 0.2V) $\phi1$ | PWH $\phi1$ | 430 | – | – | ns |
| $\phi2$ | PWH $\phi2$ | 470 | | | |
| Fall Time (Measured from 0.2V to Vcc - 0.2V) | $T_F$ | – | – | 25 | ns |
| Delay Time between Clocks (Measured at 0.2V) | $T_D$ | 0 | – | – | ns |

### Read/Write Timing **

| Characteristic | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Read/Write Setup Time from R6500 | $T_{RWS}$ | – | 100 | 225 | ns |
| Address Setup Time from R6500 | $T_{ADS}$ | – | 100 | 225 | ns |
| Memory Read Access Time | $T_{ACC}$ | – | – | 650 | ns |
| Data Stability Time Period | $T_{DSU}$ | 100 | – | – | ns |
| Data Hold Time – Read | $T_{HR}$ | 10 | – | – | ns |
| Data Hold Time – Write | $T_{HW}$ | 60 | 90 | – | ns |
| Data Setup Time from R6500 | $T_{MDS}$ | – | 150 | 175 | ns |
| RDY, S.O. Setup Time | $T_{RDY}$ | 100 | – | – | ns |
| SYNC Setup Time from R6500 | $T_{SYNC}$ | – | – | 225 | ns |
| Address Hold Time | $T_{HA}$ | 30 | 60 | – | ns |
| R/$\overline{W}$ Hold Time | $T_{HRW}$ | 30 | 60 | – | ns |

## 2 MHz Timing

### Clock Timing – R6502, 03, 04, 05, 06, 07

| Characteristic | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Cycle Time | $T_{CYC}$ | 0.5 | – | 10.0 | µs |
| $\phi_{0(IN)}$ Pulse Width (measured at 1.5V) | $PWH\phi_0$ | 240 | – | 260 | ns |
| $\phi_{0(IN)}$ Rise, Fall Time | $TR\phi_0$, $TF\phi_0$ | – | – | 10 | ns |
| Delay Time Between Clocks (measured at 1.5V) | $T_D$ | 5 | – | – | ns |
| $\phi_{1(OUT)}$ Pulse Width (measured at 1.5V) | $PWH\phi_1$ | $PWH\phi_{0L}$-20 | – | $PWH\phi_{0L}$ | ns |
| $\phi_{2(OUT)}$ Pulse Width (measured at 1.5V) | $PWH\phi_2$ | $PWH\phi_{0H}$-40 | – | $PWH\phi_{0H}$-10 | ns |
| $\phi_{1(OUT)}$, $\phi_{2(OUT)}$ Rise, Fall Time (measured at 0.8V to 2.0V) (Load = 130 pF + 1 TTL) | $T_R$, $T_F$ | – | – | 25 | ns |

### Clock Timing – R6512, 13, 14, 15

| Characteristic | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Cycle Time | $T_{CYC}$ * | 500 | – | – | ns |
| Clock Pulse Width (Measured at Vcc - 0.2V) $\phi1$ | PWH $\phi1$ | 215 | – | – | ns |
| $\phi2$ | PWH $\phi2$ | 235 | | | |
| Fall Time (measured from 0.2V to Vcc - 0.2V) | $T_F$ | – | – | 12 | ns |
| Delay Time between Clocks (measured at 0.2V) | $T_D$ | 0 | – | – | ns |

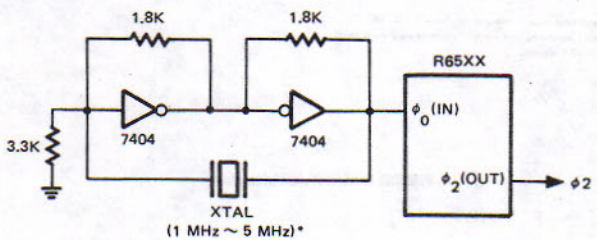
### Read/Write Timing **

| Characteristic | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Read/Write Setup Time from R6500A | $T_{RWS}$ | – | 75 | 140 | ns |
| Address Setup Time from R6500A | $T_{ADS}$ | – | 75 | 140 | ns |
| Memory Read Access Time | $T_{ACC}$ | – | – | 310 | ns |
| Data Stability Time Period | $T_{DSU}$ | 50 | – | – | ns |
| Data Hold Time – Read | $T_{HR}$ | 10 | – | – | ns |
| Data Hold Time – Write | $T_{HW}$ | 60 | 90 | – | ns |
| Data Setup Time from R6500A | $T_{MDS}$ | – | 75 | 100 | ns |
| RDY, S.O. Setup Time | $T_{RDY}$ | 50 | – | – | ns |
| SYNC Setup Time from R6500A | $T_{SYNC}$ | – | – | 150 | ns |
| Address Hold Time | $T_{HA}$ | 30 | 60 | – | ns |
| R/$\overline{W}$ Hold Time | $T_{HRW}$ | 30 | 60 | – | ns |

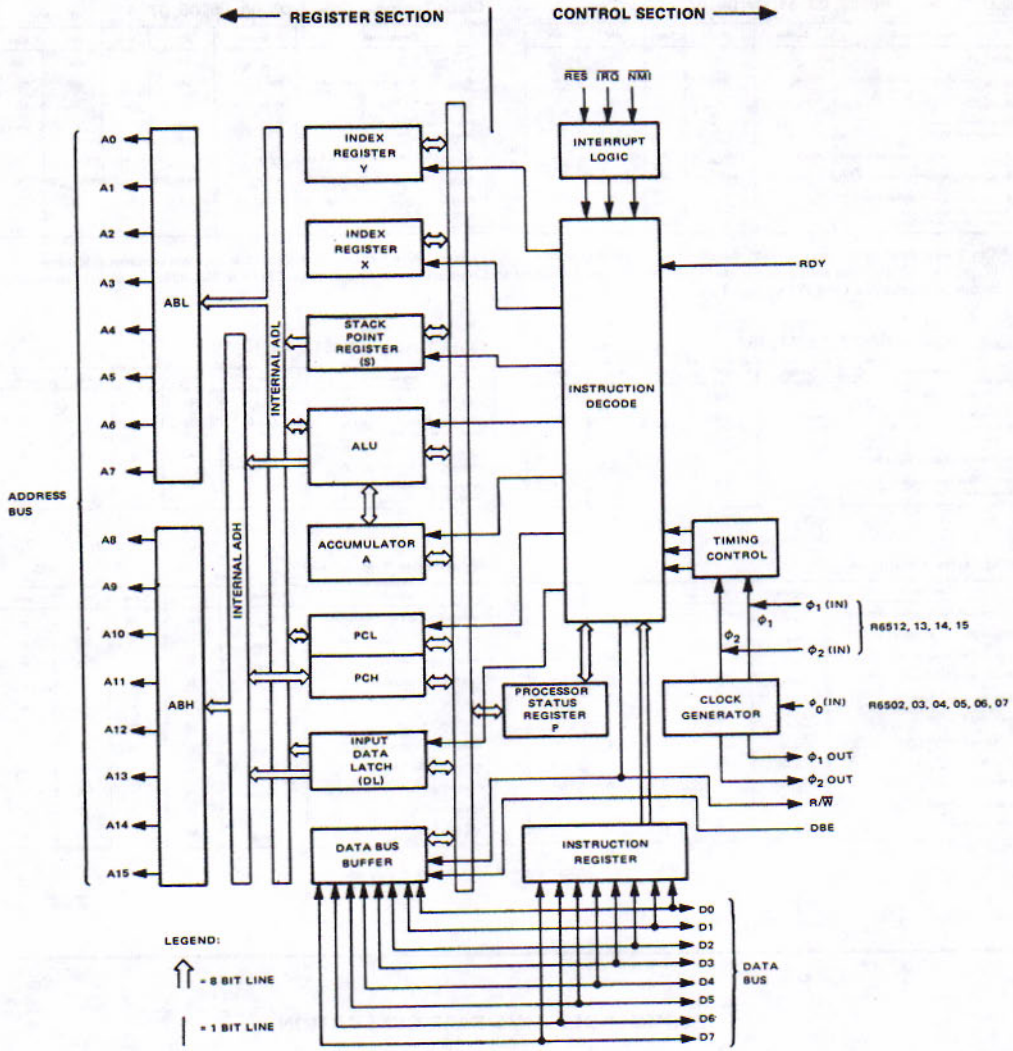
* The lowest operating frequency for the commercial temperature range CPU's is 100 KHz, which corresponds to a maximum cycle time ($T_{CYC}$) of 10 µs. The lowest operating frequency for the industrial and military temperature range CPU's is 250 KHz, which corresponds to a maximum cycle time ($T_{CYC}$) of 4 µs.

** Load Conditions = 1 TTL Load + 130 pf

## RECOMMENDED TIME BASE GENERATION




*CRYSTAL: CTS KNIGHTS MP SERIES, OR EQUIVALENT




Note: 1. Clock Generator is not included on R6512, 13, 14, 15
2. Addressing Capability and control options vary with each of the R6500 Products.

**R6500 Internal Architecture**

## SPECIFICATIONS

### Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | -0.3 to +7.0 | Vdc |
| Operating Temperature | $T_A$ | | °C |
| Commercial | | 0 to +70 | |
| Industrial | | -40 to +85 | |
| Military | | -55 to +125 | |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C |

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

### Electrical Characteristics

($V_{CC}$ = 5.0±5%, $V_{SS}$ = 0)

$\phi_1$, $\phi_2$ applies to R6512, 13, 14, 15, $\phi_{o(in)}$ applies to R6502, 03, 04, 05, 06 and 07.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | | | | Vdc |
| Logic, $\phi_{o(in)}$ | | $V_{SS}$ + 2.4 | – | $V_{CC}$ | |
| $\phi_1$, $\phi_2$ | | $V_{CC}$ - 0.3 | – | $V_{CC}$ + 0.25 | |
| Input Low Voltage | $V_{IL}$ | | | | Vdc |
| Logic, $\phi_{o(in)}$ | | $V_{SS}$ - 0.3 | – | $V_{SS}$ + 0.4 | |
| $\phi_1$, $\phi_2$ | | $V_{SS}$ - 0.3 | – | $V_{SS}$ + 0.4 | |
| Input High Threshold Voltage | $V_{IHT}$ | | | | Vdc |
| $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O. | | $V_{SS}$ + 2.0 | – | – | |
| Input Low Threshold Voltage | $V_{ILT}$ | | | | Vdc |
| $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O. | | – | – | $V_{SS}$ + 0.8 | |
| Input Leakage Current | $I_{in}$ | | | | μA |
| ($V_{in}$ = 0 to 5.25V, $V_{CC}$ = 0) | | | | | |
| Logic (Excl. RDY, S.O.) | | – | – | 2.5 | |
| $\phi_1$, $\phi_2$ | | – | – | 100 | |
| $\phi_{o(in)}$ | | – | – | 10.0 | |
| Three-State (Off State) Input Current | $I_{TSI}$ | | | | μA |
| ($V_{in}$ = 0.4 to 2.4V, $V_{CC}$ = 5.25V) | | | | | |
| Data Lines | | – | – | 10 | |
| Output High Voltage | $V_{OH}$ | | | | Vdc |
| ($I_{LOAD}$ = -100 μAdc, $V_{CC}$ = 4.75V) | | | | | |
| SYNC, Data, A0-A15, R/$\overline{W}$, $\phi_1$, $\phi_2$ | | $V_{SS}$ + 2.4 | – | – | |
| Output Low Voltage | $V_{OL}$ | | | | Vdc |
| ($I_{LOAD}$ = 1.6 mAdc, $V_{CC}$ = 4.75V) | | | | | |
| SYNC, Data, A0-A15, R/$\overline{W}$, $\phi_1$, $\phi_2$ | | – | – | $V_{SS}$ + 0.4 | |
| Power Dissipation | $P_D$ | | | | W |
| Commercial temp. versions | | – | 0.25 | 0.575 | |
| Industrial and military temp. versions | | – | 0.50 | 0.700 | |
| Capacitance at 25°C | C | | | | pF |
| ($V_{in}$ = 0, f = 1 MHz) | | | | | |
| Logic | $C_{in}$ | – | – | 10 | |
| Data | | – | – | 15 | |
| A0-A15, R/W, SYNC | $C_{out}$ | – | – | 12 | |
| $\phi_{o(in)}$ | $C_{\phi o(in)}$ | – | – | 15 | |
| $\phi_1$ | $C_{\phi 1}$ | – | 30 | 50 | |
| $\phi_2$ | $C_{\phi 2}$ | – | 50 | 80 | |

Note: $\overline{IRQ}$ and $\overline{NMI}$ require 3K pull-up resistors.

DOCUMENT NO. 29000 D39S1
OCTOBER 1978

PART NUMBER
**R65XXB**

Rockwell

# R6500 Microcomputer System DATA SHEET SUPPLEMENT





## R6500B SERIES (3 MHZ) MICROPROCESSORS

The Rockwell R6500B series is a high-performance addition to the advanced architecture R6500 8-bit microprocessor family. The family includes 10 microprocessor (CPU) devices – six CPUs have on-chip clock oscillators and drivers, four CPUs are driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single-phase inputs, crystal or RC inputs provide the time base. The external clock versions are used in multi-processor system applications. All members of the R6500 family are totally software compatible.

The R6500B series microprocessors operate at a 3 MHz clock rate, providing an instruction cycle of less than 0.7 microseconds. The R6500B microprocessors are available in ceramic and molded plastic packages (order R65XXBC or R65XXBP, respectively) and operate at $0^{\circ}C$ to $+70^{\circ}C$.

The common characteristics for each microprocessor in the R6500 family are contained in the R6500 Microprocessor Data Sheet, Document Number 29000 D39. Specifications unique to the R6500B series are listed in this document.

### FEATURES

- 3 MHz clock rate
- Single +5V supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- 8-bit Bidirectional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input
- Direct Memory Access Capability
- Bus compatible with M6800
- Choice of external or on-chip clocks
- Pipeline architecture
- $0^{\circ}C$ to $+70^{\circ}C$ operation

### R6500 CPU OPTIONS

| | 40-Pin DIP | | 18-Pin DIP | | | | |
|---|---|---|---|---|---|---|---|
| | R6502 | R6512 | R6503<br>R6513 | R6504<br>R6514 | R6505<br>R6515 | R6506 | R6507 |
| Memory Address Space | 65K | 65K | 4K | 8K | 4K | 4K | 8K |
| Interrupts – Maskable<br>– Non-Maskable | Yes<br>Yes | Yes<br>Yes | Yes<br>Yes | Yes<br>No | Yes<br>No | Yes<br>No | No<br>No |
| SYNC – Output indicates op code fetch cycle | Yes | Yes | No | No | No | No | No |
| RDY – Single step and slow memory synchronization | Yes | Yes | No | No | Yes | No | Yes |
| Ø1 Clock Output | Yes | Yes | No | No | No | Yes | No |
| DBE – Extended Data Bus Hold Time | No | Yes | No | No | No | No | No |



Specifications subject to change without notice

## SPECIFICATIONS

### Maximum Ratings

| | |
|---|---|
| $V_{CC}$, Supply Voltage | -0.3 to +7.0 Vdc |
| $V_{IN}$, Input Voltage | -0.3 to +7.0 Vdc |
| $T_A$, Operating Temperature | 0 to +70°C |
| $T_{STG}$, Storage Temperature | -55 to +150°C |

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

### Electrical Characteristics ($V_{CC}$ = 5.0V ±5%, $V_{SS}$ = 0, $T_A$ = 0°C - 70°C) $\phi_1$, $\phi_2$ applies to R6512, 13, 14, 15, $\phi_{0(IN)}$ applies to R6502, 03, 04, 05, 06, and 07

| Symbol | Characteristic | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage<br>Logic, $\phi_{0(IN)}$<br>$\phi_1$, $\phi_2$ | $V_{SS}$ +2.4<br>$V_{CC}$ -0.2 | –<br>– | $V_{CC}$<br>$V_{CC}$ +0.25 | Vdc |
| $V_{IL}$ | Input Low Voltage<br>Logic, $\phi_{0(IN)}$<br>$\phi_1$, $\phi_2$ | $V_{SS}$ -0.3<br>$V_{SS}$ -0.3 | –<br>– | $V_{SS}$ +0.4<br>$V_{SS}$ +0.4 | Vdc |
| $V_{IHT}$ | Input High Threshold Voltage<br>$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O. | $V_{SS}$ +2.0 | – | – | Vdc |
| $V_{ILT}$ | Input Low Threshold Voltage<br>$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O. | – | – | $V_{SS}$ +0.8 | Vdc |
| $I_{IN}$ | Input Leakage Current<br>($V_{IN}$ = 0 to 5.25V, $V_{CC}$ = 0)<br>Logic (Excl. RDY, S.O.)<br>$\phi_1$, $\phi_2$<br>$\phi_{0(IN)}$ | –<br>–<br>– | –<br>–<br>– | 2.5<br>100<br>10.0 | µA<br>µA<br>µA |
| $I_{TSI}$ | Three-State (Off State) Input Current<br>($V_{IN}$ = 0.4 to 2.4V, $V_{CC}$ = 5.25V)<br>Data Lines | – | – | 10 | µA |
| $V_{OH}$ | Output High Voltage<br>($I_{LOAD}$ = -100 µAdc, $V_{CC}$ = 4.75V)<br>SYNC, Data, A0-A15, R/W | $V_{SS}$ +2.4 | – | – | Vdc |
| $V_{OL}$ | Output Low Voltage<br>($I_{LOAD}$ = 1.6 mAdc, $V_{CC}$ = 4.75V)<br>SYNC, Data, A0-A15, R/W | – | – | $V_{SS}$ +0.4 | Vdc |
| $P_D$ | Power Dissipation | – | .50 | .80 | W |
| C<br>$C_{IN}$<br>$C_{OUT}$<br>$C_{\phi 0(IN)}$<br>$C_{\phi 1}$<br>$C_{\phi 2}$ | Capacitance<br>($V_{IN}$ = 0, $T_A$ = 25°C, f = 1 MHz)<br>Logic<br>Data<br>A0-A15, R/W, SYNC<br>$\phi_{0(IN)}$<br>$\phi_1$<br>$\phi_2$ | –<br>–<br>–<br>–<br>–<br>– | –<br>–<br>–<br>–<br>30<br>50 | 10<br>15<br>12<br>15<br>50<br>80 | pF |

NOTE: $\overline{IRQ}$ and $\overline{NMI}$ require 3K pull-up resistors.

**Clock Timing – R6512, 13, 14, 15, 16**

| Symbol | Characteristic | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{CYC}$ | Cycle Time | 333 | – | – | nsec |
| PWH $\phi_1$<br>PWH $\phi_2$ | Clock Pulse Width $\phi_1$ (measured at $V_{CC}$ -0.2V) $\phi_2$ | 150<br>160 | – | – | nsec |
| $T_F$, $T_R$ | Fall Time, Rise Time (measured from 0.2V to $V_{CC}$ -0.2V) | – | – | 15 | nsec |
| $T_D$ | Delay Time between Clocks (measured at 0.2V) | 0 | – | – | nsec |

**Clock Timing – R6502, 03, 04, 05, 06, 07**

| Symbol | Characteristic | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{CYC}$ | Cycle Time | 333 | – | – | ns |
| PWH $\phi_0$ | $\phi_{0(IN)}$ Pulse Width (measured at 1.5V) | 160 | – | 170 | ns |
| TR $\phi_0$, TF $\phi_0$ | $\phi_{0(IN)}$ Rise, Fall Time | – | – | 10 | ns |
| $T_D$ | Delay Time between Clocks (measured at 1.5V) | 5 | – | – | ns |
| PWH $\phi_1$ | $\phi_{1(OUT)}$ Pulse Width (measured at 1.5V) | PWH $\phi_{0L}$ -20 | – | PWH $\phi_{0L}$ | ns |
| PWH $\phi_2$ | $\phi_{2(OUT)}$ Pulse Width (measured at 1.5V) | PWH $\phi_{0H}$ -40 | – | PWH $\phi_{0H}$ -10 | ns |
| $T_R$, $T_F$ | $\phi_{1(OUT)}$, $\phi_{2(OUT)}$ Rise, Fall Time (Load = 30 pF + 1 TTL) (measured at 0.8V to 2.0V) | – | – | 15 | ns |

**Read/Write Timing (Load = 1 TTL + 130 pF)**

| Symbol | Characteristic | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{RWS}$ | Read/Write Setup Time from R6500B | – | 80 | 110 | ns |
| $T_{ADS}$ | Address Setup Time from R6500B | – | 80 | 110 | ns |
| $T_{ACC}$ | Memory Read Access Time | – | – | 170 | ns |
| $T_{DSU}$ | Data Stability Time Period | 50 | – | – | ns |
| $T_{HR}$ | Data Hold Time – Read | 10 | – | – | ns |
| $T_{HW}$ | Data Hold Time – Write | 30 | – | – | ns |
| $T_{MDS}$ | Data Setup Time from R6500B | – | 60 | 75 | ns |
| $T_{RDY}$ | RDY, S.O. Setup Time | 35 | – | – | ns |
| $T_{SYNC}$ | SYNC Setup Time from R6500B | – | – | 100 | ns |
| $T_{HA}$ | Address Hold Time | 15 | 30 | – | ns |
| $T_{HRW}$ | R/W Hold Time | 15 | 30 | – | ns |

DOCUMENT NO. 29000 D51
REVISION 2, OCT. 1978

PART NUMBER
R6500/1

Rockwell

# R6500 Microcomputer System
# DATA SHEET





## R6500/1 ONE-CHIP MICROCOMPUTER

### INTRODUCTION

The Rockwell R6500/1 is a complete, high-performance 8-bit NMOS microcomputer on a single chip, and is totally upward/downward software compatible with all members of the R6500 family.

The R6500/1 consists of an R6502 CPU, an internal clock oscillator, 2048 bytes of Read Only Memory (ROM), 64 bytes of Random Access Memory (RAM) and flexible interface circuitry. The interface circuitry includes a 16-bit programmable counter/latch with four operating modes, 32 bidirectional input/output lines (including two edge-sensitive lines), five interrupts and a counter I/O line.

### PRODUCT SUPPORT

To allow prototype circuit development, Rockwell offers a PROM compatible 64-pin Emulator device. This device provides all R6500/1 interface lines plus routing the address bus, data bus, and associated control lines off the chip to be connected to external memory.

To facilitate system and program development for the R6500/1, Rockwell offers extensive product support. The SYSTEM 65 Microcomputer Development System with the R6500/1 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/1 Personality Module allows total system test and evaluation.

Regularly scheduled designer's courses are offered at regional centers.

The support products available are:

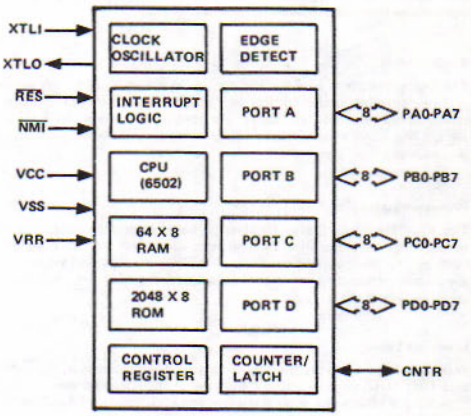
- SYSTEM 65 Microcomputer Development System — P/N S65-101
- 1 MHz R6500/1 Personality Module — P/N M65-081
- 2 MHz R6500/1 Personality Module — P/N M65-082
- 1 MHz R6500/1 Emulator Device — P/N R6500/1EC
- 2 MHz R6500/1 Emulator Device — P/N R6500/1EAC

### ORDERING INFORMATION

| Order Number | Package Type | Frequency Option | Temperature Range |
|---|---|---|---|
| R6500/1P | Plastic | 1 MHz | 0°C to 70°C |
| R6500/1C | Ceramic | 1 MHz | 0°C to 70°C |
| R6500/1AP | Plastic | 2 MHz | 0°C to 70°C |
| R6500/1AC | Ceramic | 2 MHz | 0°C to 70°C |
| R6500/1PE | Plastic | 1 MHz | −40°C to +85°C |
| R6500/1CE | Ceramic | 1 MHz | −40°C to +85°C |
| R6500/1APE | Plastic | 2 MHz | −40°C to +85°C |
| R6500/1ACE | Ceramic | 2 MHz | −40°C to +85°C |

### FEATURES

- R6502 CPU
  - Software upward/downward compatibility
  - Decimal or binary arithmetic modes
  - 13 addressing modes
  - True direct and indirect indexing
  - Memory addressable I/O
- 2048 x 8 mask programmable ROM
- 64 x 8 static RAM
- 32 bi-directional TTL compatible I/O lines (4 ports)
- 1 Counter I/O line
- 16-bit programmable counter/latch with four modes
  - Interval Timer
  - Pulse Generator
  - Event Counter
  - Pulse Width Measurement
- Five Interrupts
  - Reset
  - Non-maskable
  - Two external edge sensitive
  - Counter
- 4 MHz max crystal, clock or RC network external frequency
- 2 MHz or 1 MHz internal clock
- 1 μs minimum instruction execution
- N-channel, silicon gate, depletion load technology
- Single +5V ±10% power supply
- 500 mW operating power
- Separate power pin for RAM
- 40 pin DIP
- 64 pin PROM compatible Emulator device




Interface Diagram



Specifications subject to change without notice

# FUNCTIONAL DESCRIPTION

## CENTRAL PROCESSING UNIT (CPU)

### Clock Oscillator

The Clock Oscillator provides the basic timing signals used by the R6500/1 CPU. The reference frequency is provided by an external source, and can be from a crystal, clock or RC network input. The RC network mode is a mask option. The external frequency can vary from 200 kHz to 4 MHz. The internal Phase 2 ($\phi$ 2) frequency is one-half the external reference frequency.

### Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. Each data transfer which takes place between the registers is caused by decoding the contents of both the Instruction Register and Timing Control Logic.

### Program Counter

The 16-bit Program Counter provides the addresses which step the CPU through sequential instructions in a program. The Program Counter is incremented each time an instruction or data is fetched from memory.

### Instruction Register and Decode

Instructions fetched from memory are gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

### Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter).

### Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

### Index Registers

There are two 8-bit index registers, X and Y. These registers can be used for general purpose storage, or as a displacement to modify the base address and thus obtain a new effective address. Pre- or post-indexing of indirect addresses is possible.

### Stack Pointer

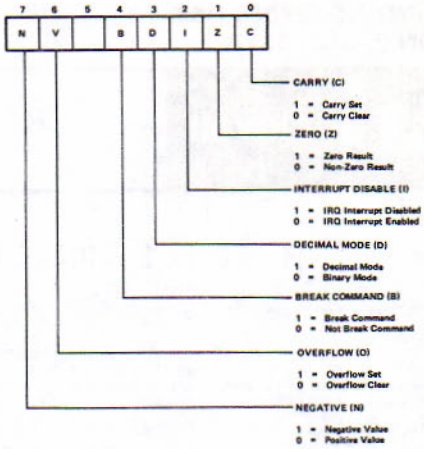
The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the CPU to perform stack manipulation under direction of either the program or interrupts $\overline{NMI}$ and $\overline{IRQ}$. The stack allows simple implementation of nested subroutines and multiple level interrupts.

### Processor Status Register

The 8-bit Processor Status Register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The R6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

### Interrupt Logic

Interrupt logic controls the sequencing of three interrupts; $\overline{RES}$, $\overline{NMI}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of three conditions: Counter Overflow, PA0 Positive Edge Detected, and PA1 Negative Edge Detected.




**Processor Status Register**

## MEMORY

### 2048 x 8 ROM

The 2048 byte Read-Only Memory (ROM) contains the program instructions and other fixed constants. These program instructions and constants are mask programmed into the ROM during fabrication of the R6500/1 device. The R6500/1 ROM is memory mapped from 800 to FFF.

### 64 x 8 RAM

The 64 byte Random Access Memory (RAM) is used for read/write memory during system operation, and contains the stack. This RAM is completely static in operation and requires no clock or dynamic refresh. A standby power pin, VRR, allows RAM memory to be maintained on 10% of the operating power in the event that VCC power is lost.

In order to take advantage of efficient zero page addressing capabilities, the RAM is assigned memory addresses 0 to 03F.

## INPUT/OUTPUT

### Bidirectional I/O Ports

The R6500/1 provides four 8-bit input/output ports (PA, PB, PC, and PD). Associated with the I/O ports are four 8-bit registers located on page zero. See the system memory map for specific addresses. Each I/O line is individually selectable as an input or an output without line grouping or port association restrictions.

An internal active transistor drives each I/O line to the low state. An internal passive resistance pulls the I/O lines to the high state, eliminating the need for external pull-up resistors.

An option is available to delete the internal pull-up resistance on 8-bit port groups at mask time. This option is employed to permanently assign an 8-bit port group to input functions, to interface with CMOS drivers, or to interface with external pull-up devices.

### Inputs

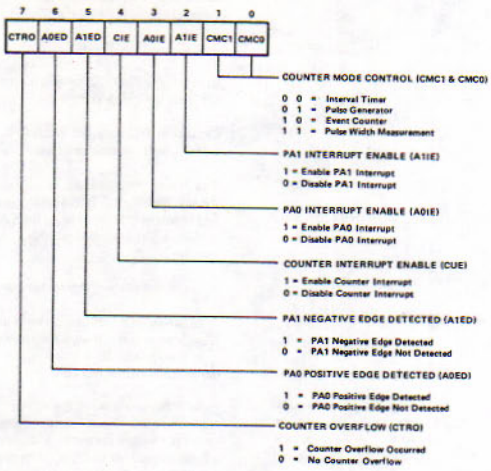
Inputs are enabled by setting the appropriate bit of the I/O port to the high state (Logic 1). A low input signal causes a logic 0 to be read. A high input signal causes a logic 1 to be read. $\overline{RES}$ loads Logic 1 into the I/O ports, thereby initializing all I/O lines as inputs.

### Outputs

Outputs are set by loading the desired bit pattern into the corresponding I/O ports. A Logic 1 selects a high output; a Logic 0 selects a low output.

## CONTROL REGISTER

The Control Register (CR) controls four Counter operating modes and three maskable interrupts. It also reports the status of three interrupt conditions. There are five control bits and three status bits. The control bits are set to Logic 1 or cleared to Logic 0 by writing the desired state into the respective bit positions. The Control Register is cleared to Logic 0 by the occurrence of $\overline{RES}$.




**Control Register**

## EDGE DETECT CAPABILITY

There is an asynchronous edge detect capability on two of the Port A I/O lines. This capability exists in addition to and independently from the normal Port A I/O functions. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. The edge detect logic is continuously active. Each edge detect signal is associated with a maskable interrupt.

### PA0 Positive Edge Detection

A positive (rising) edge is detectable on PA0. When this edge is detected, the PA0 Positive Edge Detected bit – Bit 6 in the Control Register – is set to Logic 1. When both this bit and the PA0 Interrupt Enable Bit – Bit 3 of the Control Register – are set to Logic 1, an $\overline{IRQ}$ interrupt request is generated. The PA0 Positive Edge Detected bit is cleared by writing to address 089.

### PA1 Negative Edge Detection

A negative (falling) edge is detectable on PA1. When this edge is detected, the PA1 Negative Edge Detected bit – Bit 5 of the Control Register – is set to Logic 1. When both this bit and the PA1 Interrupt Enable bit – Bit 2 of the Control Register – are set to Logic 1, an $\overline{IRQ}$ interrupt request is generated. The PA1 Negative Edge Detected bit is cleared by writing to address 08A.

## COUNTER/LATCH

The Counter/Latch consists of a 16-bit decrementing Counter and a 16-bit Latch. The Counter is comprised of two 8-bit registers. Address 086 contains the Upper Count (UC) and address 087 contains the Lower Count (LC). The Counter counts either $\phi 2$ clock periods or occurrences of an external event, depending on the selected counter mode. The UC and LC can be read at any time without affecting counter operation.

The Latch contains the Counter preset value. The Latch consists of two 8-bit registers. Address 084 contains the Upper Latch (UL) and address 085 contains the lower latch (LL). The 16-bit Latch can hold a count from 0 to 65,535. The Latch can be accessed as two write-only memory locations.

The Latch registers can be loaded at any time by storing into UL and LL. The UL can also be loaded by writing into address 088.

The Counter can be preset at any time by writing to address 088. Presetting the Counter in this manner causes the contents of the accumulator to be stored into the UL before the 16-bit value in the Latch (UL and LL) is transferred in the Counter (UC and LC).

The Counter is preset to the Latch value when the Counter overflows. When the counter decrements from 0000, Counter overflow occurs causing the next counter value to be the Latch value, not FFFF.

When the Counter overflows, Counter Overflow bit – Bit 7 of the Control Register – is set to Logic 1. When both this bit and the Counter Interrupt Enable bit – Bit 4 of the Control Register – are set, an $\overline{IRQ}$ interrupt request is generated. The Counter Overflow bit in the Control Register can be examined in an $\overline{IRQ}$ interrupt service routine to determine that the $\overline{IRQ}$ was generated by Counter overflow.

The Counter Overflow bit is cleared when the LC is read or Counter preset is performed by writing into address 088.

## COUNTER MODES

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

| Mode | CMC 1 | CMC 0 |
|---|---|---|
| Interval Timer | 0 | 0 |
| Pulse Generator | 0 | 1 |
| Event Counter | 1 | 0 |
| Pulse Width Measurement | 1 | 1 |

The Interval Timer, Pulse Generator, and Pulse Width Measurement Modes are $\phi 2$ clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line.

### Interval Timer (Mode 0)

In this mode the Counter is free running and decrements at the $\phi 2$ clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

The CNTR line is held in the high state.

### Pulse Generator (Mode 1)

In this mode the Counter is free running and decrements at the $\phi 2$ clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

The CNTR line toggles from one state to the other when Counter overflow occurs. Writing to address 088 will also toggle the CNTR line.

A symmetric or asymmetric output waveform can be generated on the CNTR line in this mode. A one-shot waveform can easily be generated by changing from Mode 1 to Mode 0 after only one occurrence of the output toggle condition.

### Event Counter (Mode 2)

In this mode the CNTR line is used as an event input line. The Counter decrements each time a rising edge is detected on CNTR. The maximum rate at which this edge can be detected is one-half the $\phi 2$ clock rate. Counter overflow sets the Control Register status bit and causes the Counter to be preset to the Latch value.

### Pulse Width Measurement (Mode 3)

This mode allows the accurate measurement of the duration of a low state on the CNTR line. The Counter decrements at the $\phi 2$ clock rate as long as the CNTR line is held in the low state. The Counter is stopped when CNTR is in the high state. If the CNTR pin is left disconnected, this mode may be selected to stop the Counter since the internal pull-up device will cause the CNTR input to be in the high state.

## RESET CONSIDERATIONS

The occurrence of $\overline{RES}$ going from low to high causes initialization of various conditions in the R6500/1. All of the I/O ports (PA, PB, PC, and PD) and CNTR are forced to the high (Logic 1) state. All bits of the Control Register are reset to Logic 0, causing the Interval Timer Mode (Mode 0) to be selected and all interrupt enabled bits to be cleared. Neither the Latch nor the Counter registers are initialized by $\overline{RES}$. The Interrupt Disable bit in the CPU Processor Status Register is set and the program starts execution at the address contained in the Reset Vector location.

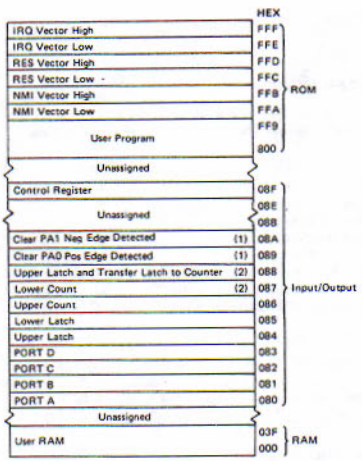
## TEST LOGIC

Special test logic provides a method for thoroughly testing the R6500/1. Applying a +12V signal to the $\overline{RES}$ line places the R6500/1 in the test mode. While in this mode, all memory fetches are made from Port PC. External test equipment can use this feature to test internal CPU logic and I/O. A program can be loaded into RAM allowing the contents of the instruction ROM to be dumped to any port for external verification.

All R6500/1 microcomputers are tested by Rockwell using this feature.

## MEMORY ADDRESSABLE I/O

The I/O ports, registers, and commands are treated as memory and are assigned specific addresses. See the system memory map for the addresses. This I/O technique allows the full set of CPU instructions to be used in the generation and sampling of I/O commands and data. When an instruction is executed with an I/O address and appropriate R/$\overline{W}$ state, the corresponding I/O function is performed.

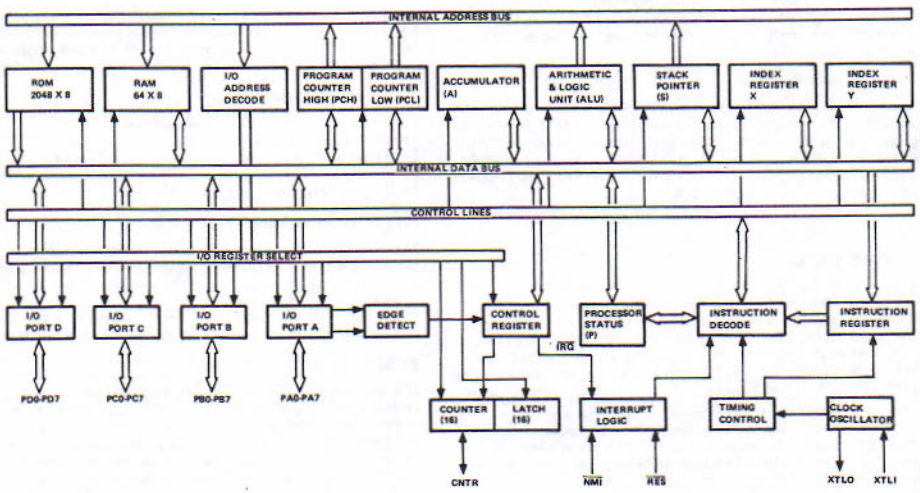



Notes:
(1) I/O command only; i.e., no stored data.
(2) Clears Counter Overflow – Bit 7 in Control Register.

**System Memory Map**

## SIGNAL DESCRIPTIONS

| SIGNAL NAME | PIN NO. | DESCRIPTION |
|---|---|---|
| VCC | 30 | Main power supply +5V ±10% |
| VRR | 1 | Separate power pin for RAM with standby power of +5V. In the event that VCC power is lost, this power retains RAM data. |
| VSS | 12 | Signal ground |
| XTLI | 10 | Crystal clock or RC network input for internal clock oscillator. |
| XTLO | 11 | Crystal or RC network output from internal clock oscillator. |
| $\overline{RES}$ | 39 | The Reset input is used to initialize the R6500/1. This signal must not transition from low to high for at least eight cycles after VCC reaches +5V.<br>+12V input enables the test mode. |
| $\overline{NMI}$ | 40 | A negative going edge on the Non-Maskable Interrupt signal requests that a non-maskable interrupt be generated within the CPU. |
| PA0-PA7<br>PB0-PB7<br>PC0-PC7<br>PD0-PD7 | 38-31<br>29-22<br>20-13<br>9-2 | Four 8-bit ports used for either input/output. Each line consists of an active transistor to VSS and a passive pull-up to +5V. The two lower bits of the PA port (PA0 and PA1) also serve as edge detect inputs with maskable interrupts. |
| CNTR | 21 | This line is used as a Counter input/output line. CNTR is an input in the Event Counter and Pulse Width Measurement modes and is an output in the Interval Timer and Pulse Generator modes. |




**R6500/1 Block Diagram**

## INSTRUCTION SET – ALPHABETIC SEQUENCE

| | |
|---|---|
| ADC | Add Memory to Accumulator with Carry |
| AND | "AND" Memory with Accumulator |
| ASL | Shift left One Bit (Memory or Accumulator) |
| BCC | Branch on Carry Clear |
| BCS | Branch on Carry Set |
| BEQ | Branch on Result Zero |
| BIT | Test Bits in Memory with Accumulator |
| BMI | Branch on Result Minus |
| BNE | Branch on Result not Zero |
| BPL | Branch on Result Plus |
| BRK | Force Break |
| BVC | Branch on Overflow Clear |
| BVS | Branch on Overflow Set |
| CLC | Clear Carry Flag |
| CLD | Clear Decimal Mode |
| CLI | Clear Interrupt Disable Bit |
| CLV | Clear Overflow Flag |
| CMP | Compare Memory and Accumulator |
| CPX | Compare Memory and Index X |
| CPY | Compare Memory and Index Y |
| DEC | Decrement Memory by One |
| DEX | Decrement Index X by One |
| DEY | Decrement Index Y by One |
| EOR | "Exclusive-or" Memory with Accumulator |
| INC | Increment Memory by One |
| INX | Increment Index X by One |
| INY | Increment Index Y by One |
| JMP | Jump to New Location |
| JSR | Jump to New Location Saving Return Address |
| LDA | Load Accumulator with Memory |
| LDX | Load Index X with Memory |
| LDY | Load Index Y with Memory |
| LSR | Shift One Bit Right (Memory or Accumulator) |
| NOP | No operation |
| ORA | "OR" Memory with Accumulator |
| PHA | Push Accumulator on Stack |
| PHP | Push Processor Status on Stack |
| PLA | Pull Accumulator from Stack |
| PLP | Pull Processor Status from Stack |
| ROL | Rotate One Bit Left (Memory or Accumulator) |
| ROR | Rotate One Bit Right (Memory or Accumulator) |
| RTI | Return from Interrupt |
| RTS | Return from Subroutine |
| SBC | Subtract Memory from Accumulator with Borrow |
| SEC | Set Carry Flag |
| SED | Set Decimal Mode |
| SEI | Set Interrupt Disable Status |
| STA | Store Accumulator in Memory |
| STX | Store Index X in Memory |
| STY | Store Index Y in Memory |
| TAX | Transfer Accumulator to Index X |
| TAY | Transfer Accumulator to Index Y |
| TSX | Transfer Stack Pointer to Index X |
| TXA | Transfer Index X to Accumulator |
| TXS | Transfer Index X to Stack Register |
| TYA | Transfer Index Y to Accumulator |



## ADDRESSING MODES

**ACCUMULATOR ADDRESSING** – This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

**IMMEDIATE ADDRESSING** – In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

**ABSOLUTE ADDRESSING** – In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits.

**ZERO PAGE ADDRESSING** – The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

**INDEXED ZERO PAGE ADDRESSING** – (X, Y indexing) – This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

**INDEXED ABSOLUTE ADDRESSING** – (X, Y indexing) – This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X", and "Absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

**IMPLIED ADDRESSING** – In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

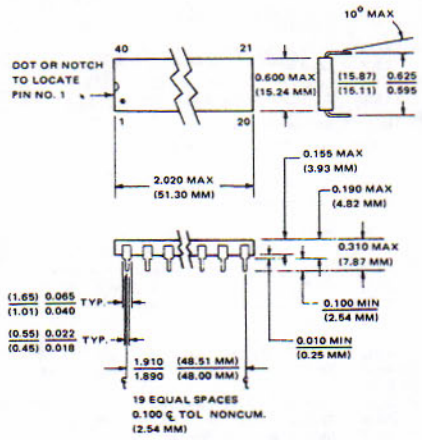
**RELATIVE ADDRESSING** – Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to +127 bytes from the next instruction.

**INDEXED INDIRECT ADDRESSING** – In indexed indirect addressing (referred to as (Indirect, X)), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

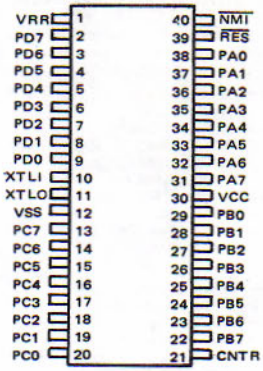
**INDIRECT INDEXED ADDRESSING** – In indirect indexed addressing (referred to as (Indirect), Y), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

**ABSOLUTE INDIRECT** – The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.



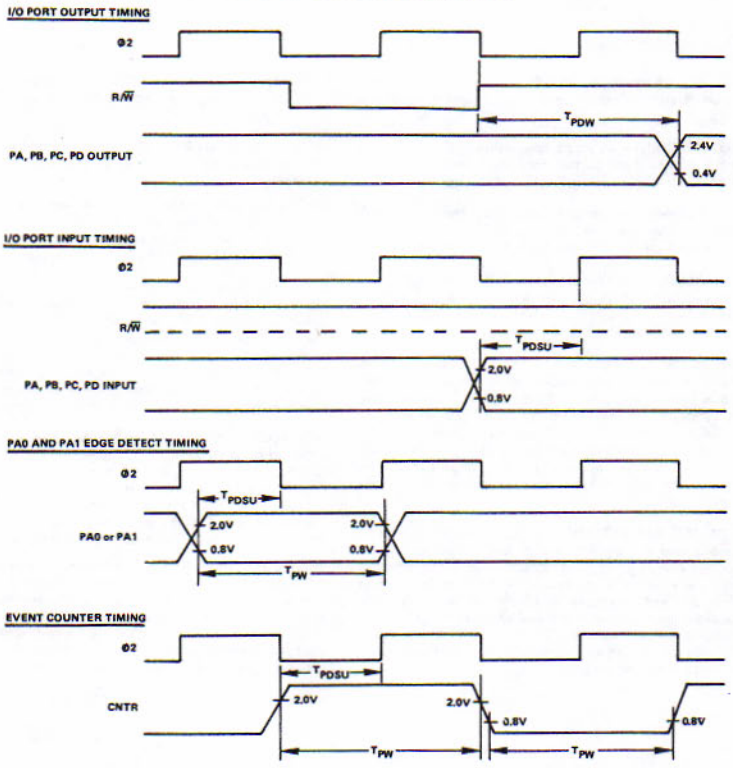

NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

**Packaging Diagram**




**Pin Configuration**

## TIMING CHARACTERISTICS



## SPECIFICATIONS

### Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | -0.3 to +7.0 | Vdc |
| Operating Temperature Range | T | | °C |
| Commercial | | 0 to +70 | |
| Industrial | | -40 to +85 | |
| Storage Temperature Range | $T_{stg}$ | -55 to + 150 | °C |

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

### Static D.C. Characteristics $V_{CC}$ = 5V±10%

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Dissipation (Outputs High) | $P_D$ | – | 500 | – | mW |
| RAM Standby Current | $I_{RR}$ | | 10 | | mAdc |
| Input High Voltage (Normal Operating Levels) | $V_{IH}$ | +2.0 | – | $V_{CC}$ | Vdc |
| Input Low Voltage (Normal Operating Levels) | $V_{IL}$ | -0.3 | – | +0.8 | Vdc |
| Input Threshold Voltage | $V_{IT}$ | 0.8 | – | 2.0 | Vdc |
| Input Leakage Current | $I_{IN}$ | | | | µAdc |
| $V_{in}$ = 0 to 5.0 Vdc $\overline{RES}$, $\overline{NMI}$ | | – | ±1.0 | ±2.5 | |
| Input High Voltage (XTLI) | $V_{IHXT}$ | +2.4 | – | $V_{CC}$ | Vdc |
| Input Low Voltage (XTLI) | $V_{ILXT}$ | -0.3 | – | +0.4 | Vdc |
| Input Low Current | $I_{IL}$ | | | | |
| ($V_{IL}$ = 0.4 Vdc) | | – | -1.0 | -1.6 | mAdc |
| Output High Voltage | $V_{OH}$ | | | | |
| ($V_{CC}$ = min, $I_{Load}$ = -100 µAdc) | | 2.4 | – | – | Vdc |
| Output Low Voltage | $V_{OL}$ | | | | |
| ($V_{CC}$ = min, $I_{Load}$ = 1.6 mAdc) | | – | – | +0.4 | Vdc |
| Output High Current (Sourcing) | $I_{OH}$ | | | | |
| ($V_{OH}$ = 2.4 Vdc) | | -100 | | – | µAdc |
| Output Low Current (Sinking) | $I_{OL}$ | | | | |
| ($V_{OL}$ = 0.4 Vdc) | | 1.6 | – | – | mAdc |
| Input Capacitance | $C_{in}$ | | | | pF |
| ($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | | | | | |
| PA, PB, PC, PD,CNTR | | – | – | 10 | |
| XTLI, XTLO | | – | – | 50 | |
| Output Capacitance | $C_{out}$ | | | | |
| ($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | | – | – | 10 | pF |

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

### AC Characteristics $V_{CC}$ = +5V±10%

| Parameter | Symbol | 1MHz | | 2MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| XTLI Input Clock Cycle Time | $T_{cyc}$ | 0.500 | 5.0 | 0.250 | 5.0 | µsec |
| Internal Write to Peripheral Data Valid | $T_{PDW}$ | 1.0 | | 0.5 | | µsec |
| Peripheral Data Setup Time | $T_{PDSU}$ | 400 | | 200 | | µsec |
| Count and Edge Detect Pulse Width | $T_{PW}$ | 1.0 | | 0.5 | | µsec |

# INSTRUCTION SET

| INSTRUCTIONS | | IMMEDIATE | | | ABSOLUTE | | | ZERO PAGE | | | ACCUM. | | | IMPLIED | | | (IND, X) | | | (IND), Y | | | Z. PAGE, X | | | ABS. X | | | ABS. Y | | | RELATIVE | | | INDIRECT | | | Z. PAGE, Y | | | PROCESSOR STATUS CODES | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MNEMONIC | OPERATION | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | OP | n | # | 7 6 5 4 3 2 1 0<br>N V • B D I Z C | MNEMONIC |
| ADC | A + M + C → A (4) (1) | 69 | 2 | 2 | 6D | 4 | 3 | 65 | 3 | 2 | | | | | | | 61 | 6 | 2 | 71 | 5 | 2 | 75 | 4 | 2 | 7D | 4 | 3 | 79 | 4 | 3 | | | | | | | | | | N V • • • • Z C | ADC |
| AND | A∧M → A (1) | 29 | 2 | 2 | 2D | 4 | 3 | 25 | 3 | 2 | | | | | | | 21 | 6 | 2 | 31 | 5 | 2 | 35 | 4 | 2 | 3D | 4 | 3 | 39 | 4 | 3 | | | | | | | | | | N • • • • • Z • | AND |
| ASL | C ← [7 6 5 4 3 2 1 0] ← 0 | | | | 0E | 6 | 3 | 06 | 5 | 2 | 0A | 2 | 1 | | | | | | | | | | 16 | 6 | 2 | 1E | 7 | 3 | | | | | | | | | | | | | N • • • • • Z C | ASL |
| BCC | BRANCH ON C = 0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 90 | 2 | 2 | | | | | | | | • • • • • • • • | BCC |
| BCS | BRANCH ON C = 1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | B0 | 2 | 2 | | | | | | | | • • • • • • • • | BCS |
| BEQ | BRANCH ON Z = 1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | F0 | 2 | 2 | | | | | | | | • • • • • • • • | BEQ |
| BIT | A∧M | | | | 2C | 4 | 3 | 24 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | $M_7$ $M_6$ • • • • Z • | BIT |
| BMI | BRANCH ON N = 1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 30 | 2 | 2 | | | | | | | | • • • • • • • • | BMI |
| BNE | BRANCH ON Z = 0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | D0 | 2 | 2 | | | | | | | | • • • • • • • • | BNE |
| BPL | BRANCH ON N = 0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 10 | 2 | 2 | | | | | | | | • • • • • • • • | BPL |
| BRK | BREAK | | | | | | | | | | | | | 00 | 7 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • 1 • 1 • • | BRK |
| BVC | BRANCH ON V = 0 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 50 | 2 | 2 | | | | | | | | • • • • • • • • | BVC |
| BVS | BRANCH ON V = 1 (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 70 | 2 | 2 | | | | | | | | • • • • • • • • | BVS |
| CLC | 0 → C | | | | | | | | | | | | | 18 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • 0 | CLC |
| CLD | 0 → D | | | | | | | | | | | | | D8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • 0 • • | CLD |
| CLI | 0 → I | | | | | | | | | | | | | 58 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • 0 • • | CLI |
| CLV | 0 → V | | | | | | | | | | | | | B8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • 0 • • • • • | CLV |
| CMP | A − M | C9 | 2 | 2 | CD | 4 | 3 | C5 | 3 | 2 | | | | | | | C1 | 6 | 2 | D1 | 5 | 2 | D5 | 4 | 2 | DD | 4 | 3 | D9 | 4 | 3 | | | | | | | | | | N • • • • • Z C | CMP |
| CPX | X − M | E0 | 2 | 2 | EC | 4 | 3 | E4 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z C | CPX |
| CPY | Y − M | C0 | 2 | 2 | CC | 4 | 3 | C4 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z C | CPY |
| DEC | M − 1 → M | | | | CE | 6 | 3 | C6 | 5 | 2 | | | | | | | | | | | | | D6 | 6 | 2 | DE | 7 | 3 | | | | | | | | | | | | | N • • • • • Z • | DEC |
| DEX | X − 1 → X | | | | | | | | | | | | | CA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | DEX |
| DEY | Y − 1 → Y | | | | | | | | | | | | | 88 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | DEY |
| EOR | A ∨ M → A (1) | 49 | 2 | 2 | 4D | 4 | 3 | 45 | 3 | 2 | | | | | | | 41 | 6 | 2 | 51 | 5 | 2 | 55 | 4 | 2 | 5D | 4 | 3 | 59 | 4 | 3 | | | | | | | | | | N • • • • • Z • | EOR |
| INC | M + 1 → M | | | | EE | 6 | 3 | E6 | 5 | 2 | | | | | | | | | | | | | F6 | 6 | 2 | FE | 7 | 3 | | | | | | | | | | | | | N • • • • • Z • | INC |
| INX | X + 1 → X | | | | | | | | | | | | | E8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | INX |
| INY | Y + 1 → Y | | | | | | | | | | | | | C8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | INY |
| JMP | JUMP TO NEW LOC | | | | 4C | 3 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 6C | 5 | 3 | | | | • • • • • • • • | JMP |
| JSR | JUMP SUB | | | | 20 | 6 | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | JSR |
| LDA | M → A (1) | A9 | 2 | 2 | AD | 4 | 3 | A5 | 3 | 2 | | | | | | | A1 | 6 | 2 | B1 | 5 | 2 | B5 | 4 | 2 | BD | 4 | 3 | B9 | 4 | 3 | | | | | | | | | | N • • • • • Z • | LDA |
| LDX | M → X (1) | A2 | 2 | 2 | AE | 4 | 3 | A6 | 3 | 2 | | | | | | | | | | | | | | | | | | | BE | 4 | 3 | | | | | | | B6 | 4 | 2 | N • • • • • Z • | LDX |
| LDY | M → Y (1) | A0 | 2 | 2 | AC | 4 | 3 | A4 | 3 | 2 | | | | | | | | | | | | | B4 | 4 | 2 | BC | 4 | 3 | | | | | | | | | | | | | N • • • • • Z • | LDY |
| LSR | 0 → [7 6 5 4 3 2 1 0] → C | | | | 4E | 6 | 3 | 46 | 5 | 2 | 4A | 2 | 1 | | | | | | | | | | 56 | 6 | 2 | 5E | 7 | 3 | | | | | | | | | | | | | 0 • • • • • Z C | LSR |
| NOP | NO OPERATION | | | | | | | | | | | | | EA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | NOP |
| ORA | A ∨ M → A | 09 | 2 | 2 | 0D | 4 | 3 | 05 | 3 | 2 | | | | | | | 01 | 6 | 2 | 11 | 5 | 2 | 15 | 4 | 2 | 1D | 4 | 3 | 19 | 4 | 3 | | | | | | | | | | N • • • • • Z • | ORA |
| PHA | A → Ms S − 1 → S | | | | | | | | | | | | | 48 | 3 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | PHA |
| PHP | P → Ms S − 1 → S | | | | | | | | | | | | | 08 | 3 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | PHP |
| PLA | S + 1 → S Ms → A | | | | | | | | | | | | | 68 | 4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | PLA |
| PLP | S + 1 → S Ms → P | | | | | | | | | | | | | 28 | 4 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | (RESTORED) | PLP |
| ROL | [7 6 5 4 3 2 1 0] ← [C] | | | | 2E | 6 | 3 | 26 | 5 | 2 | 2A | 2 | 1 | | | | | | | | | | 36 | 6 | 2 | 3E | 7 | 3 | | | | | | | | | | | | | N • • • • • Z C | ROL |
| ROR | [C] → [7 6 5 4 3 2 1 0] | | | | 6E | 6 | 3 | 66 | 5 | 2 | 6A | 2 | 1 | | | | | | | | | | 76 | 6 | 2 | 7E | 7 | 3 | | | | | | | | | | | | | N • • • • • Z C | ROR |
| RTI | RTRN INT | | | | | | | | | | | | | 40 | 6 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | (RESTORED) | RTI |
| RTS | RTRN SUB | | | | | | | | | | | | | 60 | 6 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | RTS |
| SBC | A − M − C → A (1) | E9 | 2 | 2 | ED | 4 | 3 | E5 | 3 | 2 | | | | | | | E1 | 6 | 2 | F1 | 5 | 2 | F5 | 4 | 2 | FD | 4 | 3 | F9 | 4 | 3 | | | | | | | | | | N V • • • • Z (3) | SBC |
| SEC | 1 → C | | | | | | | | | | | | | 38 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • 1 | SEC |
| SED | 1 → D | | | | | | | | | | | | | F8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • 1 • • | SED |
| SEI | 1 → I | | | | | | | | | | | | | 78 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • 1 • • | SEI |
| STA | A → M | | | | 8D | 4 | 3 | 85 | 3 | 2 | | | | | | | 81 | 6 | 2 | 91 | 6 | 2 | 95 | 4 | 2 | 9D | 5 | 3 | 99 | 5 | 3 | | | | | | | | | | • • • • • • • • | STA |
| STX | X → M | | | | 8E | 4 | 3 | 86 | 3 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 96 | 4 | 2 | • • • • • • • • | STX |
| STY | Y → M | | | | 8C | 4 | 3 | 84 | 3 | 2 | | | | | | | | | | | | | 94 | 4 | 2 | | | | | | | | | | | | | | | | • • • • • • • • | STY |
| TAX | A → X | | | | | | | | | | | | | AA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | TAX |
| TAY | A → Y | | | | | | | | | | | | | A8 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | TAY |
| TSX | S → X | | | | | | | | | | | | | BA | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | TSX |
| TXA | X → A | | | | | | | | | | | | | 8A | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | TXA |
| TXS | X → S | | | | | | | | | | | | | 9A | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | • • • • • • • • | TXS |
| TYA | Y → A | | | | | | | | | | | | | 98 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | N • • • • • Z • | TYA |

(1) ADD 1 to "N" IF PAGE BOUNDARY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT, = BORROW
(4) IF IN DECIMAL MODE, Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

+ ADD
− SUBTRACT
∧ AND
∨ OR
∨ EXCLUSIVE OR

$M_7$ MEMORY BIT 7
$M_6$ MEMORY BIT 6
n NO. CYCLES
# NO. BYTES

DOCUMENT NO. 29000D51S
REV. 1, APRIL 1979

PART NUMBER
**R6500/1E**

Rockwell

# R6500 Microcomputer System DATA SHEET SUPPLEMENT



# R6500/1E EMULATOR DEVICE

## INTRODUCTION

To aid in designing R6500/1 microcomputer systems, Rockwell has developed a PROM compatible, 64-pin, R6500/1E Emulator device. The architecture of the Emulator device is basically the same as the R6500/1 except that the address, data, and associated control lines are routed off the chip for connection to an external memory.

The functions and operation of the Emulator device are identical to the R6500/1 with only some minor differences, described herein. The R6500/1 data sheet (Document No. 2900D51) contains the description of R6500/1 and R6500/1 common interface signals and functions.

### ORDERING INFORMATION

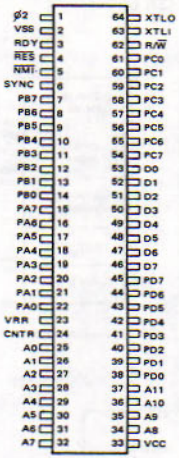
| Order Number | Package Type | Frequency Option | Temperature Range |
|---|---|---|---|
| R6500/1EC | Ceramic | 1 MHz | 0°C to 70°C |
| R6500/1EAC | Ceramic | 2 MHz | 0°C to 70°C |

## SIGNAL DESCRIPTIONS

All R6500/1 interface signals are provided in the Emulator device. While the Emulator pin assignments are different from the R6500/1 in order to accommodate the 64-pin Emulator package, the interface electrical characteristics are identical. The Emulator device provides 24 additional signals to route the address bus (12 lines), the data bus (8 lines), and control signals (4 lines) off the chip for connection to external memory.

## MEMORY MAP

An additional 1024 bytes of memory (400-7FF) are addressable in the Emulator device to support software development.




**R6500/1E Pin Configuration**

## EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock — the RC option is not available in the Emulator device.

## I/O PORT PULLUPS

The R6500/1E has the internal I/O port pullup resistance only.

## R6500/1E DEVICE ADDITIONAL SIGNALS

| Signal Name | Pin No. | Description |
|---|---|---|
| R/$\overline{W}$ | 62 | Read/Write. The Read/Write output controls the direction of data transfer between the R6500/1E Emulator CPU and external memory. This line is high when reading data from memory and low when writing data to memory. |
| RDY | 3 | Ready. The Ready input delays execution of any cycle during which the RDY line is low. This allows the user to halt or single step the CPU on any cycle except a write cycle. A negative transition to the low state during the ϕ2 clock low pulse will halt the CPU with the address lines containing the current address being fetched. If RDY is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent ϕ2 clock pulse in which the RDY line is low. |
| SYNC | 6 | Sync. The Sync signal is provided to identify those cycles in which the CPU is performing an OP CODE fetch. SYNC goes high during ϕ2 clock-low pulse during an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the ϕ2 clock low pulse in which SYNC went high, the CPU will halt in its current state and will remain in that state until the RDY line goes high. Using this technique, the SYNC signal can be used to control RDY to cause single instruction execution. |
| ϕ2 | 1 | Phase 2 (ϕ2) clock pulse. Data transfer can take place only during ϕ2 clock pulse. |
| A0-A11 | 25-32<br>34-37 | Address Bus Lines. The address bus buffers on the R6500/1E are push/pull type drivers capable of driving at least 130 pf and one standard TTL load. The address bus always contains known data. The addressing technique involves putting an address on the address bus which is known to be either in program sequence, on the same page in program memory, or at a known point in memory. The I/O addresses are also placed on these lines. |
| D0-D7 | 53-46 | Data Bus Lines. All transfers of instructions and data between the CPU and external memory take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition. |

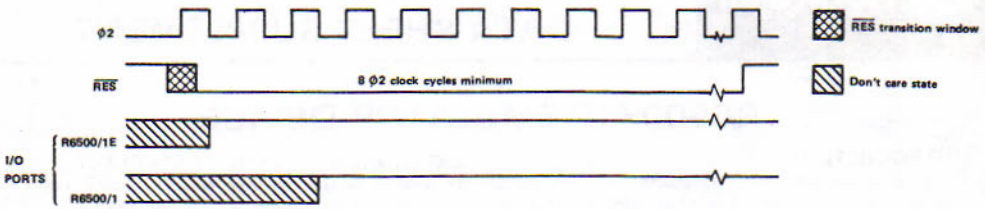




Specifications subject to change without notice

## R6500/1E I/O PORT INITIALIZATION

Ports A, B, C and D and the CNTR line in R6500/1E are initialized to the logic high state two Ø2 clock cycles earlier than in the R6500/1. It is still required, however, that the $\overline{RES}$ line to the R6500/1E be held low for at least eight Ø2 clock cycles after $V_{CC}$ reaches operating range.



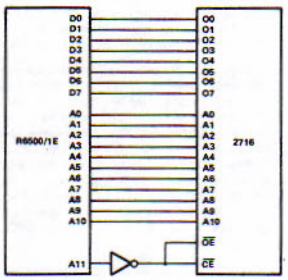

## TYPICAL R6500/1E PROGRAM MEMORY INTERCONNECTIONS

Shown below are two typical connections between the R6500/1E and program memory (in this case, type 2716 and 2708 PROMS). Example 1 shows a connection to a 2K 2716 PROM. Since the R6500/1 has a 2K ROM capacity, the contents of the PROM could be masked directly into the production R6500/1 ROM.

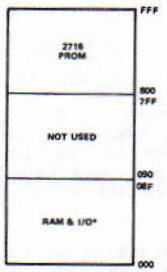
Example 2 shows a connection to 3K of 2708 PROMS. The extra 1K PROM allows expanded or additional programs be used during R6500/1 firmware development. The production program, however, must be reduced to 2K maximum (between addresses 800 and FFF) before committing to R6500/1 ROM.

### EXAMPLE 1: R6500/1E Connected to One 2716 PROM (2K Bytes)

**Connection Diagram**

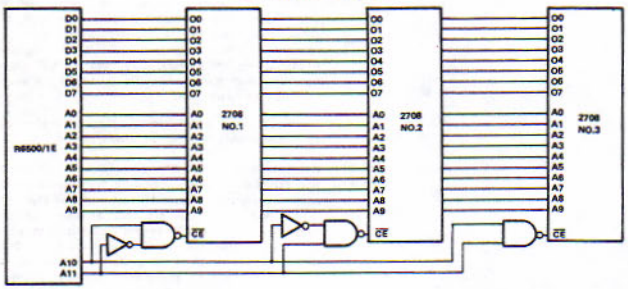



**Memory Map**

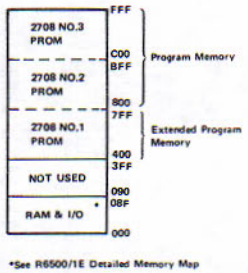



### EXAMPLE 2: R6500/1E Connected to Three PROMS (3K Bytes)

**Connection Diagram**




**Memory Map**




*See R6500/1E Detailed Memory Map

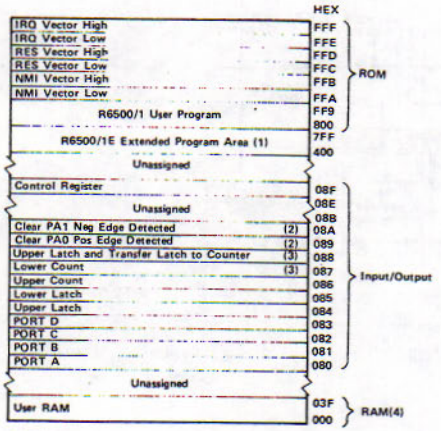
### Truth Table

| Address | | PROM Select | | | |
|---|---|---|---|---|---|
| A11 | A10 | 2708 No. 3 $\overline{CE}$ | 2708 No. 2 $\overline{CE}$ | 2808 No. 1 $\overline{CE}$ | Selected Address Range |
| 0 | 0 | 1 | 1 | 1 | 000-3FF |
| 0 | 1 | 1 | 1 | 0 | 400-7FF |
| 1 | 0 | 1 | 0 | 1 | 800-BFF |
| 1 | 1 | 0 | 1 | 1 | C00-FFF |

## R6500/1 EMULATOR DEVICE TIMING

| Signal | Symbol | 1 MHz | | 2 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| R/$\overline{W}$ setup time from CPU | $T_{RWS}$ | | 300 | | 200 | ns |
| Address setup time from CPU | $T_{ADS}$ | | 300 | | 200 | ns |
| Memory read access time | $T_{ACC}$ | | 525 | | 225 | ns |
| Data stabilization time | $T_{DSU}$ | 150 | | 75 | | ns |
| Data hold time — Read | $T_{HR}$ | 10 | | 10 | | ns |
| Data hold time — Write | $T_{HW}$ | 30 | | 30 | | ns |
| Data delay time from CPU | $T_{MDS}$ | | 200 | | 150 | ns |
| RDY setup time | $T_{RDY}$ | 100 | | 50 | | ns |
| SYNC delay time from CPU | $T_{SYNC}$ | | 350 | | 175 | ns |
| Address hold time | $T_{HA}$ | 30 | | 30 | | ns |
| R/$\overline{W}$ hold time | $T_{HRW}$ | 30 | | 30 | | ns |
| Cycle Time | $T_{CYC}$ | 1.0 | 10.0 | 0.5 | 10.0 | $\mu s$ |

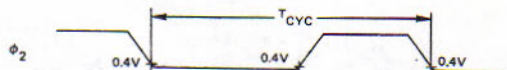
## R6500/1E DETAILED MEMORY MAP



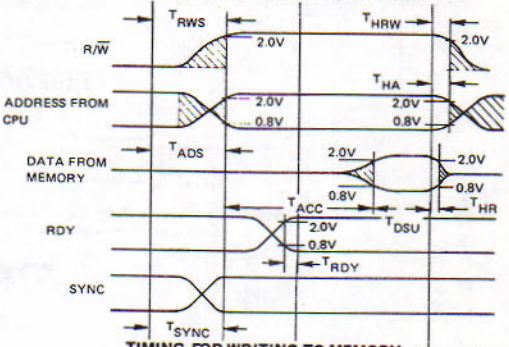

NOTES
(1) Additional 1024 bytes are decoded for external memory addressing by the R6500/1E Emulator Device. This area can be used during debug, but cannot be used in a masked ROM R6500/1.
(2) I/O command only; i.e., no stored data.
(3) Clears Counter Overflow — Bit 7 in Control Register
(4) CAUTION: The R6500/1E allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production R6500/1, however allows RAM mapping only at 000-03F.

## R6500/1E TIMING DIAGRAMS

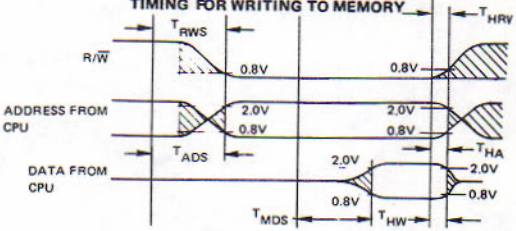
### PHASE 2 ($\phi$2) TIMING REFERENCE




### TIMING FOR READING FROM MEMORY



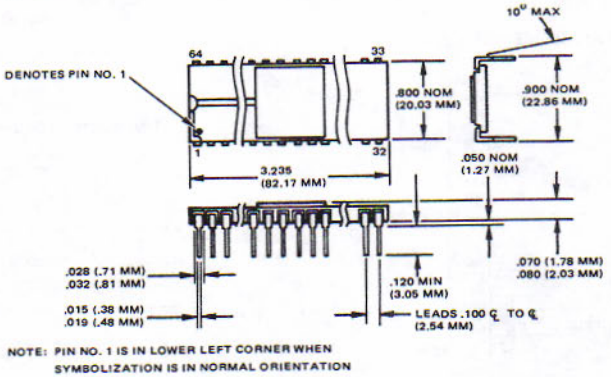

### TIMING FOR WRITING TO MEMORY



## ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 5.0 ± 5%, $V_{SS}$ = 0, $T_A$ = 25°C)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input High Threshold Voltage<br>D0-D7, RDY, | $V_{IHT}$ | $V_{SS}$ + 2.4 | – | – | Vdc |
| Input Low Threshold Voltage<br>D0-D7, RDY, | $V_{ILT}$ | – | – | $V_{SS}$ + 0.8 | Vdc |
| Three-State (Off State) Input Current<br>(V = 0.4 to 2.4V, $V_{CC}$ = 5.25V)<br>D0-D7 | $I_{TSI}$ | – | – | 10 | µA |
| Output High Voltage<br>($I_{LOAD}$ = 100µ Adc, $V_{CC}$ = 4.75V)<br>D0-D7, SYNC, A0-A11, R/$\overline{W}$, $\phi$2 | $V_{OH}$ | $V_{SS}$ + 2.4 | – | – | Vdc |
| Output Low Voltage<br>($I_{LOAD}$ = 1.6 mAdc, $V_{CC}$ = 4.75V)<br>D0-D7, SYNC, A0-A11, R/$\overline{W}$, $\phi$2 | $V_{OL}$ | – | – | $V_{SS}$ + 0.6 | Vdc |
| Power Dissipation | $P_D$ | – | 0.75 | 1.20 | W |
| Capacitance<br>($V_{in}$ = 0, $T_A$ = 25°C, f = 1 MHz)<br>RDY<br>D0-D7<br>A0-A11, R/$\overline{W}$, SYNC<br>$\phi$2 | C<br>$C_{in}$<br><br>$C_{out}$<br>$C_{\phi 2}$ | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>50 | <br>10<br>15<br>12<br>80 | pF |
| I/O Port Pull-up Resistance | $R_L$ | 3.0 | 6.0 | 11.5 | kohm |




NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION

**Packaging Diagram**

DOCUMENT NO. R6500 NO1
REV. 1, JANUARY 1979

Rockwell

# R6500 Microcomputer System
## APPLICATION NOTE





# Low Cost Crystal Oscillator for Clock Input

## PURPOSE

This application note describes a low cost oscillator circuit which will produce the basic input frequency required by the clock generator circuits in the Rockwell R650X series microcomputers. This circuit takes advantage of using either one of two readily available low cost crystals. Both crystals are approximately the same cost depending on source and quantities. The low cost oscillator crystals identified in the table below may be obtained from Electro Dynamics, 5625 Foxridge Drive, Shawnee Mission, Kansas 66201 by ordering Part No. 333R05-001 (3.579 MHz) or 59672 (4.19 MHz).

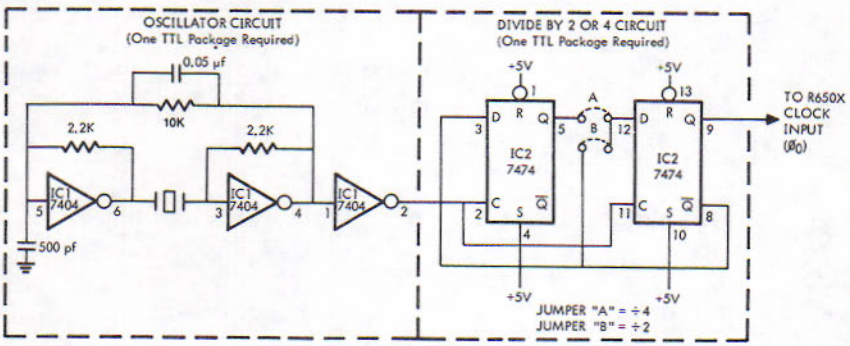
The oscillator output frequency is divided by 2 or by 4 to provide any of the frequency options shown in the table. By trading off the slight deviation in frequency from the standard 1 MHz or 2MHz clock with cost, this approach can reduce the cost of the oscillator circuit to less than $2.00 each in quantity buys.

| CRYSTAL | | OUTPUT FREQUENCY (MHz) | |
|---|---|---|---|
| Primary Use | Frequency | Divided By 2 | Divided By 4 |
| Color TV P/N 333R05-001 | 3.579545 MHz | 1.7897 | 0.894886 |
| Automotive Clock P/N 59672 | 4.194304 MHz | 2.097152 | 1.048576 |

## DESCRIPTION

The clock input frequency generator shown in the schematic consists of an oscillator circuit requiring one IC and a divide by 2 or by 4 circuit which also requires only one IC. The output of this circuit is applied to the ($\emptyset_0$) input of the R650X microcomputer clock generator circuit.

The oscillator circuit uses three of the six drivers in a standard 7404 and a crystal to produce an output. The oscillator output is input to a standard 7474 and the frequency is divided by either 2 or 4 depending on the jumper connections (A or B), as shown in the schematic.




CLOCK INPUT FREQUENCY GENERATOR



Rockwell Microelectronic Devices
P. O. Box 3669
Anaheim, Calif. 92803

DOCUMENT NO. 29000 D40
REVISION 2, OCT. 1978

PART NUMBER
**R6520**

Rockwell

# R6500 Microcomputer System DATA SHEET





## PERIPHERAL INTERFACE ADAPTER (PIA)

### DESCRIPTION

The R6520 Peripheral Interface Adapter is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the R6500 family of microprocessors, the R6520 allows implementation of very complex systems at a minimum overall cost.

Control of peripheral devices is handled primarily through two 8-bit bidirectional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or for "hand-shaking" data between the processor and a peripheral device.

### Ordering Information

**Order Number:** R6520 — — —

Temperature Range:
- No suffix = 0°C to +70°C
- E = -40°C to +85°C (Industrial)
- MT = -55°C to +125°C (Military)
- M = MIL-STD-883, Class B

Package:
- C = Ceramic
- P = Plastic

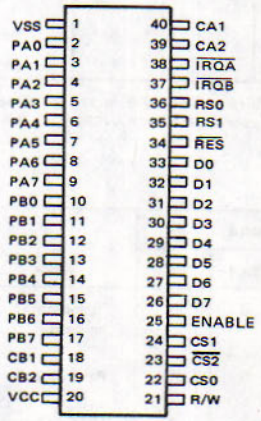
(Not Available for M or MT suffix)

Frequency Range:
- No suffix = 1 MHz
- A = 2MHz

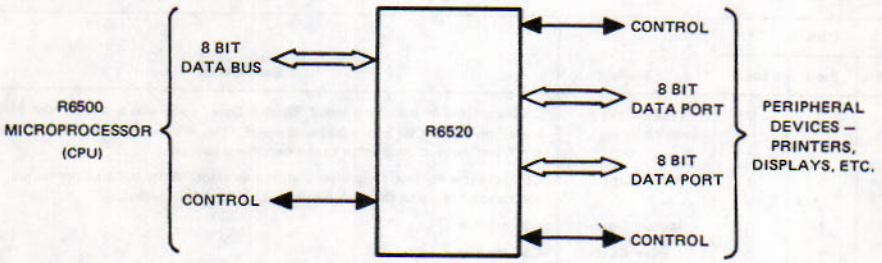
**NOTE:** Contact your local Rockwell Representative concerning availability.

### FEATURES

- High performance replacement for Motorola/AMI/MOSTEK/ Hitachi peripheral adapter.
- N channel, depletion load technology, single +5V supply.
- Completely Static and TTL compatible.
- CMOS compatible peripheral control lines.
- Fully automatic "hand-shake" allows positive control of data transfers between processor and peripheral devices.
- Commercial, industrial and military temperature range versions.




**Pin Configuration**




**Basic R6520 Interface Diagram**

# SUMMARY OF R6520 OPERATION

**See Rockwell Microcomputer Hardware Manual for detailed description of R6520 operation.**

## CA1/CB1 Control

| CRA (CRB) | | Active Transition of Input Signal* | IRQA (IRQB) Interrupt Outputs |
|---|---|---|---|
| Bit 1 | Bit 0 | | |
| 0 | 0 | Negative | Disable — remain high |
| 0 | 1 | Negative | Enable — goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1) |
| 1 | 0 | Positive | Disable — remain high |
| 1 | 1 | Positive | Enable — as explained above |

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

## CA2/CB2 Input Modes

| CRA (CRB) | | | Active Transition of Input Signal* | IRQA (IRQB) Interrupt Output |
|---|---|---|---|---|
| Bit 5 | Bit 4 | Bit 3 | | |
| 0 | 0 | 0 | Negative | Disable — remains high |
| 0 | 0 | 1 | Negative | Enable — goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2) |
| 0 | 1 | 0 | Positive | Disable — remains high |
| 0 | 1 | 1 | Positive | Enable — as explained above |

Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

## CA2 Output Modes

| CRA | | | Mode | Description |
|---|---|---|---|---|
| Bit 5 | Bit 4 | Bit 3 | | |
| 1 | 0 | 0 | "Handshake" on Read | CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor. |
| 1 | 0 | 1 | Pulse Output | CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken. |
| 1 | 1 | 0 | Manual Output | CA2 set low |
| 1 | 1 | 1 | Manual Output | CA2 set high |

## CB2 Output Modes

| CRB | | | Mode | Description |
|---|---|---|---|---|
| Bit 5 | Bit 4 | Bit 3 | | |
| 1 | 0 | 0 | "Handshake" on Write | CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device. |
| 1 | 0 | 1 | Pulse Output | CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available. |
| 1 | 1 | 0 | Manual Output | CB2 set low |
| 1 | 1 | 1 | Manual Output | CB2 set high |

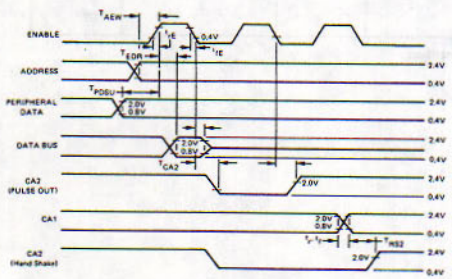
## A.C. CHARACTERISTICS

### Read Timing Characteristics (Loading 130 pF and one TTL load)

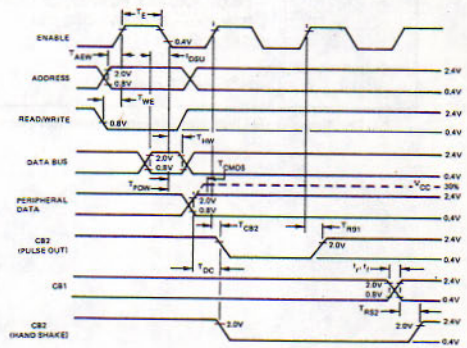
| Characteristics | Symbol | 1 MHz | | 2 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Delay Time, Address valid to Enable positive transition | $T_{AEW}$ | 180 | – | 90 | – | ns |
| Delay Time, Enable positive transition to Data valid on bus | $T_{EDR}$ | – | 395 | – | 190 | ns |
| Peripheral Data Setup Time | $T_{PDSU}$ | 300 | – | 150 | – | ns |
| Data Bus Hold Time | $T_{HR}$ | 10 | – | 10 | – | ns |
| Delay Time, Enable negative transition to CA2 negative transition | $T_{CA2}$ | – | 1.0 | – | 0.5 | µs |
| Delay Time, Enable negative transition to CA2 positive transition | $T_{RS1}$ | – | 1.0 | – | 0.5 | µs |
| Rise and Fall Time for CA1 and CA2 input signals | $t_r$, $t_f$ | – | 1.0 | – | 0.5 | µs |
| Delay Time from CA1 active transition to CA2 positive transition | $T_{RS2}$ | – | 2.0 | – | 1.0 | µs |
| Rise and Fall Time for Enable input | $t_{rE}$, $t_{fE}$ | – | 25 | – | 25 | ns |

### Write Timing Characteristics

| Characteristics | Symbol | 1 MHz | | 2 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Enable Pulse Width | $T_E$ | 0.470 | 25 | 0.235 | 25 | µs |
| Delay Time, Address valid to Enable positive transition | $T_{AEW}$ | 180 | – | 90 | – | ns |
| Delay Time, Data valid to Enable negative transition | $T_{DSU}$ | 300 | – | 150 | – | ns |
| Delay Time, Read/Write negative transition to Enable positive transition | $T_{WE}$ | 130 | – | 65 | – | ns |
| Data Bus Hold Time | $T_{HW}$ | 10 | – | 10 | – | ns |
| Delay Time, Enable negative transition to Peripheral Data valid | $T_{PDW}$ | – | 1.0 | – | 0.5 | µs |
| Delay Time, Enable negative transition to Peripheral Data valid CMOS ($V_{CC}$ - 30%) PA0-PA7, CA2 | $T_{CMOS}$ | – | 2.0 | – | 1.0 | µs |
| Delay Time, Enable positive transition to CB2 negative transition | $T_{CB2}$ | – | 1.0 | – | 0.5 | µs |
| Delay Time, Peripheral Data valid to CB2 negative transition | $T_{DC}$ | 0 | 1.5 | 0 | 0.75 | µs |
| Delay Time, Enable positive transition to CB2 positive transition | $T_{RS1}$ | – | 1.0 | – | 0.5 | µs |
| Rise and Fall Time for CB1 and CB2 input signals | $t_r$, $t_f$ | – | 1.0 | – | 0.5 | µs |
| Delay Time, CB1 active transition to CB2 positive transition | $T_{RS2}$ | – | 2.0 | – | 1.0 | µs |




Read Timing Characteristics




Write Timing Characteristics

## SPECIFICATIONS

### Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | -0.3 to +7.0 | Vdc |
| Operating Temperature Range | T | | °C |
| Commercial | | 0 to +70 | |
| Industrial | | -40 to +85 | |
| Military | | -55 to +125 | |
| Storage Temperature Range | $T_{STG}$ | -55 to + 150 | °C |

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

### Static D.C. Characteristics

($V_{CC}$ = 5.0V ± 5%, $V_{SS}$ = 0, $T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage (Normal Operating Levels) | $V_{IH}$ | +2.0 | – | $V_{CC}$ | Vdc |
| Input Low Voltage (Normal Operating Levels) | $V_{IL}$ | -0.3 | – | +0.8 | Vdc |
| Input Threshold Voltage | $V_{IT}$ | 0.8 | – | 2.0 | Vdc |
| Input Leakage Current | $I_{in}$ | | | | μAdc |
| $V_{in}$ = 0 to 5.0 Vdc R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Φ2 | | – | ±1.0 | ±2.5 | |
| Three-State (Off State Input Current) ($V_{in}$ = 0.4 to 2.4 Vdc, $V_{CC}$ = max) D0-D7, PB0-PB7, CB2 | $I_{TSI}$ | – | ±2.0 | ±10 | μAdc |
| Input High Current ($V_{IH}$ = 2.4 Vdc) PA0-PA7, CA2 | $I_{IH}$ | -100 | -250 | – | μAdc |
| Input Low Current ($V_{IL}$ = 0.4 Vdc) PA0-PA7, CA2 | $I_{IL}$ | – | -1.0 | -1.6 | mAdc |
| Output High Voltage ($V_{CC}$ = min, $I_{Load}$ = -100 μAdc) | $V_{OH}$ | 2.4 | – | – | Vdc |
| Output Low Voltage ($V_{CC}$ = min, $I_{Load}$ = 1.6 mAdc) | $V_{OL}$ | – | – | +0.4 | Vdc |
| Output High Current (Sourcing) ($V_{OH}$ = 2.4 Vdc) | $I_{OH}$ | -100 | -1000 | – | μAdc |
| ($V_O$ = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base) PB0-PB7, CB2 | | -1.0 | -2.5 | – | mAdc |
| Output Low Current (Sinking) ($V_{OL}$ = 0.4 Vdc) | $I_{OL}$ | 1.6 | – | – | mAdc |
| Output Leakage Current (Off State) $\overline{IRQA}$, $\overline{IRQB}$ | $I_{off}$ | – | 1.0 | 10 | μAdc |
| Power Dissipation | $P_D$ | – | 200 | 500 | mW |
| Input Capacitance | $C_{in}$ | | | | pF |
| ($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) D0-D7, PA0-PA7, PB0-PB7, CA2, CB2 | | – | – | 10 | |
| R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, | | – | – | 7.0 | |
| CA1, CB1, Φ2 | | – | – | 20 | |
| Output Capacitance ($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | $C_{out}$ | – | – | 10 | pF |

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

DOCUMENT NO. 29000 D47
REVISION 1, OCT. 1978

PART NUMBER
R6522

Rockwell

# R6500 Microcomputer System

## DATA SHEET

# VERSATILE INTERFACE ADAPTER (VIA)





## SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-channel, silicon-gate, depletion-load technology. Its performance speeds are enhanced by advanced system architecture. Its innovative architecture results in smaller chips – the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices, memory and I/O devices . . . as well as low-cost design aids and documentation.

## DESCRIPTION

The R6522 VIA adds two powerful, flexible Interval Timers, a serial-to-parallel/parallel-to-serial shift register and input latching on the peripheral ports to the capabilities of the R6520 Peripheral Interface Adapter (PIA) device. Handshaking capability is expanded to allow control of bidirectional data transfers between VIAs in multiple processor systems and between peripherals.

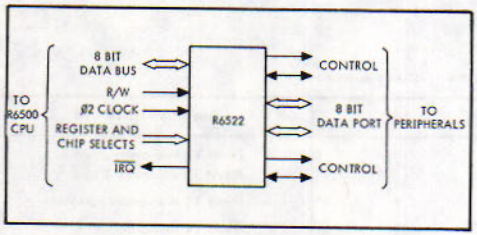
Control of peripherals is primarily through two 8-bit bidirectional ports. Each of these ports can be programmed to act as an input or an output. Peripheral I/O lines can be selectively controlled by the Interval Timers to generate programmable-frequency square waves and/or to count externally generated pulses. Positive control of VIA functions is gained through its internal register organization: Interrupt Flag Register, Interrupt Enable Register, and two Function Control Registers.

## FEATURES

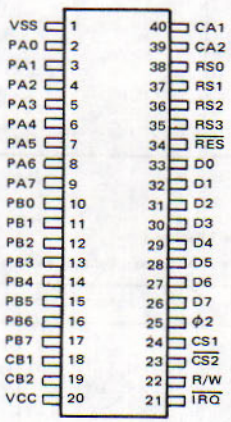
- Organized for simplified software control of many functions
- Compatible with the R650X and R651X family of microprocessors (CPUs)
- Bi-directional, 8-bit data bus for communication with microprocessor
- Two Bi-directional, 8-bit input/output ports for interface with peripheral devices
- CMOS and TTL compatible input/output peripheral ports
- Data Direction Registers allow each peripheral pin to act as either an input or an output
- Interrupt Flag Register allows the microprocessor to readily determine the source of an interrupt and provides convenient control of the interrupts within the chip
- Handshake control logic for input/output peripheral data transfer operations
- Data latching on peripheral input/output ports
- Two fully-programmable interval timers/counters
- Eight-bit Shift Register for serial interface
- Forty-pin plastic or ceramic DIP package.

### Ordering Information

| Order Number | Package Type | Frequency | Temperature Range |
|---|---|---|---|
| R6522P | Plastic | 1 MHz | 0°C to +70°C |
| R6522AP | Plastic | 2 MHz | 0°C to +70°C |
| R6522C | Ceramic | 1 MHz | 0°C to +70°C |
| R6522AC | Ceramic | 2 MHz | 0°C to +70°C |
| R6522PE | Plastic | 1 MHz | -40°C to +85°C |
| R6522APE | Plastic | 2 MHz | -40°C to +85°C |
| R6522CE | Ceramic | 1 MHz | -40°C to +85°C |
| R6522ACE | Ceramic | 2 MHz | -40°C to +85°C |
| R6522CMT | Ceramic | 1 MHz | -55°C to +125°C |




Basic R6522 Interface Diagram




Pin Configuration



Specifications subject to change without notice

## OPERATION SUMMARY

**Register Select Lines (RS0, RS1, RS2, RS3)**

The four Register select lines are normally connected to the processor address bus lines to allow the processor to select the internal R6522 register which is to be accessed. The sixteen possible combinations access the registers as follows:

| RS3 | RS2 | RS1 | RS0 | Register | Remarks |
|---|---|---|---|---|---|
| L | L | L | L | ORB | Controls Handshake |
| L | L | L | H | ORA | |
| L | L | H | L | DDRB | |
| L | L | H | H | DDRA | |
| L | H | L | L | T1L-L | Write Latch |
| | | | | T1C-L | Read Counter |
| L | H | L | H | T1C-H | Trigger T1L-L/T1C-L Transfer |
| L | H | H | L | T1L-L | |
| L | H | H | H | T1L-H | |

| RS3 | RS2 | RS1 | RS0 | Register | Remarks |
|---|---|---|---|---|---|
| H | L | L | L | T2L-L | Write Latch |
| | | | | T2C-L | Read Counter |
| H | L | L | H | T2C-H | Triggers T2L-L/T2C-L Transfer |
| H | L | H | | SR | |
| H | L | H | H | ACR | |
| H | H | L | L | PCR | |
| H | H | L | H | IFR | |
| H | H | H | L | IER | |
| H | H | H | H | ORA | No Effect on Handshake |

Note: L = 0.4V DC, H = 2.4V DC.

**Timer 2 Control**

| RS3 | RS2 | RS1 | RS0 | R/W = L | R/W = H |
|---|---|---|---|---|---|
| H | L | L | L | Write T2L-L | Read T2C-L<br>Clear Interrupt flag |
| H | L | L | H | Write T2C-H<br>Transfer T2L-L to T2C-L<br>Clear Interrupt flag | Read T2C-H |

**Writing the Timer 1 Register**

The operations which take place when writing to each of the four T1 addresses are as follows:

| RS3 | RS2 | RS1 | RS0 | Operation (R/W = L) |
|---|---|---|---|---|
| L | H | L | L | Write into low order latch |
| L | H | L | H | Write into high order latch<br>Write into high order counter<br>Transfer low order latch into low order counter<br>Reset T1 interrupt flag |
| L | H | H | L | Write low order latch |
| X | H | H | H | Write high order latch<br>Reset T1 interrupt flag |

**Reading the Timer 1 Registers**

For reading the Timer 1 registers, the four addresses relate directly to the four registers as follows:

| RS3 | RS2 | RS1 | RS0 | Operation (R/W = H) |
|---|---|---|---|---|
| L | H | L | L | Read T1 low order counter<br>Reset T1 interrupt flag |
| L | H | L | H | Read T1 high order counter |
| L | H | H | L | Read T1 low order latch |
| L | H | H | H | Read T1 high order latch |

**Timer 1 Operating Modes**

Two bits are provided in the Auxiliary Control Register to allow selection of the T1 operating modes. These bits and the four possible modes are as follows:

| ACR7 Output Enable | ACR6 "Free-Run" Enable | Mode |
|---|---|---|
| 0 | 0 | Generate a single time-out interrupt each time T1 is loaded |
| 0 | 1 | Generate continuous interrupts |
| 1 | 0 | Generate a single interrupt and an output pulse on PB7 for each T1 load operation |
| 1 | 1 | Generate continuous interrupts and a square wave output on PB7 |

## FUNCTION CONTROL

Control of the various functions and operating modes within the R6522 is accomplished primarily through two registers, the Peripheral Control Register (PCR), and the Auxiliary Control Register (ACR). The PCR is used primarily to select the operating mode for the four peripheral control pins. The Auxiliary Control Register selects the operating mode for the Interval Timers (T1, T2), and the Serial Port (SR).

**Peripheral Control Register**

The Peripheral Control Register is organized as follows:

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | CB2 Control | | | CB1 Control | CA2 Control | | | CA1 Control |

Typical functions are shown below:

| PCR3 | PCR2 | PCR1 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Input mode – Set CA2 interrupt flag (IFR0) on a negative transition of the input signal. Clear IFR0 on a read or write of the Peripheral A Output Register. |
| 0 | 0 | 1 | Independent interrupt input mode – Set IFR0 on a negative transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag. |
| 0 | 1 | 0 | Input mode – Set CA2 interrupt flag on a positive transition of the CA2 input signal. Clear IFR0 with a read or write of the Peripheral A Output Register. |
| 0 | 1 | 1 | Independent interrupt input mode – Set IFR0 on a positive transition of the CA2 input signal. Reading or writing ORA does not clear the CA2 interrupt flag. |
| 1 | 0 | 0 | Handshake output mode – Set CA2 output low on a read or write of the Peripheral A Output Register. Reset CA2 high with an active transition on CA1. |
| 1 | 0 | 1 | Pulse output mode – CA2 goes low for one cycle following a read or write of the Peripheral A Output Register. . |
| 1 | 1 | 0 | Manual output mode – The CA2 output is held low in this mode. |
| 1 | 1 | 1 | Manual output mode – The CA2 output is held high in this mode. |

### Auxiliary Control Register

Many of the functions in the Auxiliary Control Register have been discussed previously. However, a summary of this register is presented here as a convenient reference for the R6522 user. The Auxiliary Control Register is organized as follows:

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | T1 Control | | T2 Control | Shift Register Control | | | PB Latch Enable | PA Latch Enable |

### Shift Register Control

The Shift Register operating mode is selected as follows:

| ACR4 | ACR3 | ACR2 | Mode |
|---|---|---|---|
| 0 | 0 | 0 | Shift Register Disabled. |
| 0 | 0 | 1 | Shift in under control of Timer 2. |
| 0 | 1 | 0 | Shift in under control of system clock. |
| 0 | 1 | 1 | Shift in under control of external clock pulses. |
| 1 | 0 | 0 | Free-running output at rate determined by Timer 2. |
| 1 | 0 | 1 | Shift out under control of Timer 2. |
| 1 | 1 | 0 | Shift out under control of the system clock. |
| 1 | 1 | 1 | Shift out under control of external clock pulses. |

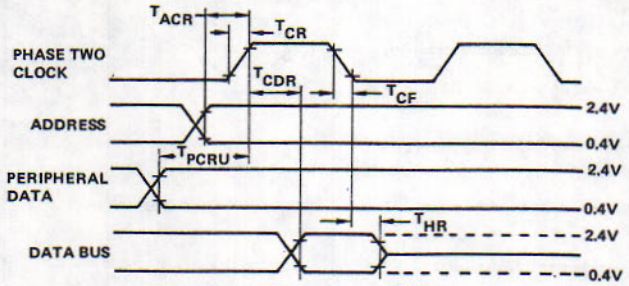
### T2 Control

Timer 2 operates in two modes. If ACR5 = 0, T2 acts as an interval timer in the one-shot mode. If ACR5 = 1, Timer 2 acts to count a predetermined number of pulses on pin PB6.

## TIMING CHARACTERISTICS

### Read Timing Characteristics (loading 130 pF and one TTL load)

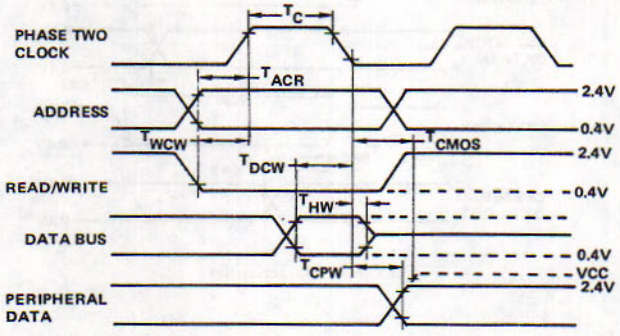
| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Delay time, address valid to clock positive transition | $T_{ACR}$ | 180 | – | – | nS |
| Delay time, clock positive transition to data valid on bus | $T_{CDR}$ | – | – | 395 | nS |
| Peripheral data setup time | $T_{PCR}$ | 300 | – | – | nS |
| Data bus hold time | $T_{HR}$ | 10 | – | – | nS |
| Rise and fall time for clock input | $T_{RC}$ $T_{RF}$ | – | – | 25 | nS |




Read Timing Characteristics

### Write Timing Characteristics

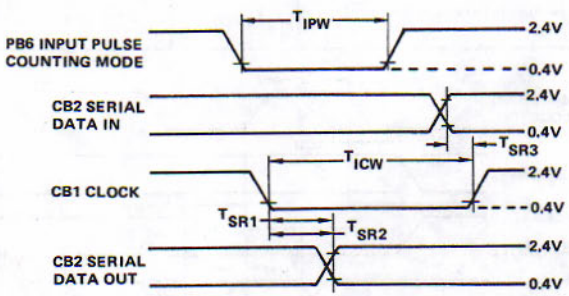
| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Enable pulse width | $T_C$ | 0.47 | – | 25 | μS |
| Delay time, address valid to clock positive transition | $T_{ACW}$ | 180 | – | – | nS |
| Delay time, data valid to clock negative transition | $T_{DCW}$ | 300 | – | – | nS |
| Delay time, read/write negative transition to clock positive transition | $T_{WCW}$ | 180 | – | – | nS |
| Data bus hold time | $T_{HW}$ | 10 | – | – | nS |
| Delay time, Enable negative transition to peripheral data valid | $T_{CPW}$ | – | – | 1.0 | μS |
| Delay time, clock negative transition to peripheral data valid CMOS (VCC - 30%) | $T_{CMOS}$ | – | – | 2.0 | μS |




Write Timing Characteristics

## I/O Timing Characteristics

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Rise and fall time for CA1, CB1, CA2 and CB2 input signals | $T_{RF}$ | – | – | 1.0 | μs |
| Delay time, clock negative transition to CA2 negative transition (read handshake or pulse mode) | $T_{CA2}$ | – | – | 1.0 | μs |
| Delay time, clock negative transition to CA2 positive transition (pulse mode) | $T_{RS1}$ | – | – | 1.0 | μs |
| Delay time, CA1 active transition to CA2 positive transition (handshake mode) | $T_{RS2}$ | – | – | 2.0 | μs |
| Delay time, clock positive transition to CA2 or CB2 negative transition (write handshake) | $T_{WHS}$ | – | – | 1.0 | μs |
| Delay time, peripheral data valid to CB2 negative transition | $T_{DC}$ | 0 | – | 1.5 | μs |
| Delay time, clock positive transition to CA2 or CB2 positive transition (pulse mode) | $T_{RS3}$ | – | – | 1.0 | μs |
| Delay time, CB1 active transition to CA2 or CB2 positive transition (handshake mode) | $T_{RS4}$ | – | – | 2.0 | μs |
| Delay time, peripheral data valid to CA1 or CB1 active transition (input latching) | $T_{IL}$ | 300 | – | – | ns |
| Delay time CB1 negative transition to CB2 data valid (internal SR clock, shift out) | $T_{SR1}$ | – | – | 300 | ns |
| Delay time, negative transition of CB1 input clock to CB2 data valid (external clock, shift out) | $T_{SR2}$ | – | – | 300 | ns |
| Delay time, CB2 data valid to positive transition of CB1 clock (shift in, internal or external clock) | $T_{SR3}$ | – | – | 300 | ns |
| Pulse Width – PB6 Input Pulse | $T_{IPW}$ | 2 | – | – | μs |
| Pulse Width – CB1 Input Clock | $T_{ICW}$ | 2 | – | – | μs |
| Pulse Spacing – PB6 Input Pulse | $I_{IPS}$ | 2 | – | – | μs |
| Pulse Spacing – CB1 Input Pulse | $I_{ICS}$ | 2 | – | – | μs |




I/O Timing Characteristics

## SPECIFICATIONS

### Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +7.0 | Vdc |
| Input Voltage | $V_{IN}$ | -0.3 to +7.0 | Vdc |
| Operating Temperature Range | T | | °C |
| Commercial | | 0 to +70 | |
| Industrial | | -40 to +85 | |
| Military | | -55 to +125 | |
| Storage Temperature Range | $T_{STG}$ | -55 to +150 | °C |

This device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

### Electrical Characteristics

(VCC = 5.0V ±5%, VSS = 0)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input high voltage (normal operation) | $V_{IH}$ | +2.4 | VCC | Vdc |
| Input low voltage (normal operation) | $V_{IL}$ | -0.3 | +0.8 | Vdc |
| Input leakage current — $V_{in}$ = 0 to 5 Vdc<br>R/W, RES, RS0, RS1, RS2, RS3, CS1, CS2, CA1, Ø2 | $I_{IN}$ | — | ±2.5 | μAdc |
| Off-state input current — $V_{in}$ = 0.4 to 2.4V<br>VCC = Max, D0 to D7 | $I_{TSI}$ | — | ±10 | μAdc |
| Input high current — $V_{IH}$ = 2.4V<br>PA0-PA7, CA2, PB0-PB7, CB1, CB2 | $I_{IH}$ | -100 | — | μAdc |
| Input low current — $V_{IL}$ = 0.4 Vdc<br>PA0-PA7, CA2, PB0-PB7, CB1, CB2 | $I_{IL}$ | — | -1.6 | mAdc |
| Output high voltage<br>VCC = min, $I_{load}$ = -100 μAdc<br>PA0-PA7, CA2, PB0-PB7, CB1, CB2 | $V_{OH}$ | 2.4 | — | Vdc |
| Output low voltage<br>VCC = min, $I_{load}$ = 1.6 mAdc | $V_{OL}$ | — | +0.4 | Vdc |
| Output high current (sourcing)<br>$V_{OH}$ = 2.4V<br>$V_{OH}$ = 1.5V, PB0-PB7, CB1, CB2 | $I_{OH}$ | -100<br>-1.0 | —<br>— | μAdc<br>mAdc |
| Output low current (sinking)<br>$V_{OL}$ = 0.4 Vdc | $I_{OL}$ | 1.6 | — | mAdc |
| Output leakage current (off state)<br>IRQ | $I_{off}$ | — | 10 | μAdc |
| Input Capacitance — $T_A$ = 25°C, f = 1 MHz<br>R/W, RES, RE0, RS1, RS2, RS3, CS1, CS2,<br>D0-D7, PA0-PA7, CA2, PB0-PB7,<br>CB1, CB2<br>Ø2 input | $C_{in}$ | —<br>—<br>— | 7.0<br>10<br>20 | pF |
| Output capacitance — $T_A$ = 25°C, f = 1 MHz | $C_{out}$ | — | 10 | pF |
| Power dissipation | $P_d$ | — | 750 | mW |

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**R6541**

Rockwell

# R6500 Microcomputer System
## PRODUCT PREVIEW

# PROGRAMMABLE KEYBOARD/DISPLAY CONTROLLER (PKDC)

## DESCRIPTION

The R6541 Programmable Keyboard/Display Controller (PKDC) is a general purpose keyboard and segmented display interface device designed for use with 8-bit microprocessors. The R6541 adds an advanced keyboard scan and display refresh capability to the established and expanding line of R6500 products. The 8-bit R6500 microcomputer system is produced with N-channel, silicon gate, depletion load technology. The autonomous operation of the R6541 relieves the CPU from performing high demand periodic keyboard/display service functions.

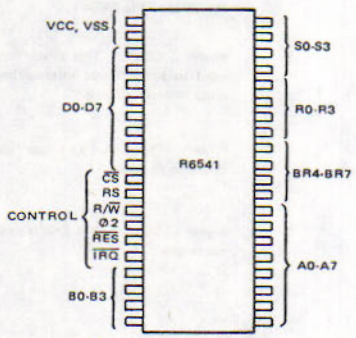
The R6541 has two sections: keyboard and display. The keyboard portion can scan up to 128 matrix type key switches. It can also interface with an array of 64 sensors (static switches) or a strobed interface keyboard. Key depression can be N-key rollover type. Key entries are debounced and stored in an 8-character First In First Out (FIFO)/Sensor RAM. A programmable length interrupt prevents FIFO/Sensor RAM overflow.

The display section provides a buffered scanned display interface with LED, fluorescent, Burroughs SELF-SCAN® display, and other display technologies. Numeric and alphanumeric displays may be directly driven as well as simple indicators. The R6541 has two CPU addressable 16 x 8 display RAM's.

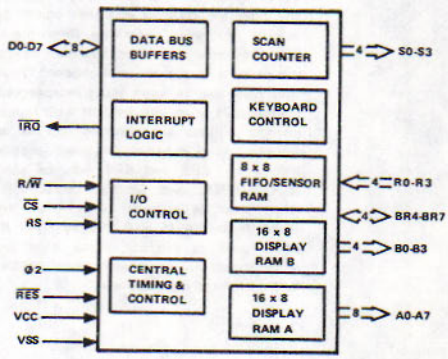
A unique R6541 feature is the 4-line bidirectional BR Display/Return bus. This flexible sensor input or display output capability allows the R6541 to be easily configured to specific applications. When the BR lines are used as outputs, two independent 8 segment, 16-character displays or one 16 segment, 16 character display can be directly driven along with scanning a 64 key encoded keyboard. When the BR lines are used as input, a 12 segment, 16 character display can be directly driven along with scanning a non-encoded 16 x 8 keyboard or sensor matrix. Many other application configurations are possible.

## FEATURES

- Compatible with 8-bit microprocessors
- 8-Character FIFO/Sensor RAM with programmable interrupt
- N-Key rollover
- 12, 16 or dual 8 segment display outputs
- Flexible 16 x 8 keyboard matrix scan modes
- Flexible 8 x 8 sensor matrix scan modes
- Programmable keyboard/sensor mode partitioning
- Strobed output entry mode
- Fully programmable timing
  - Key scan
  - Debounce
  - Display scan
  - Digit and segment
- 2 MHz or 1 MHz operation
- Single +5V ± 10% power supply
- 40-pin plastic or ceramic DIP




R6541 Pin Configuration




R6541 Interface Diagram



Specifications subject to change without notice

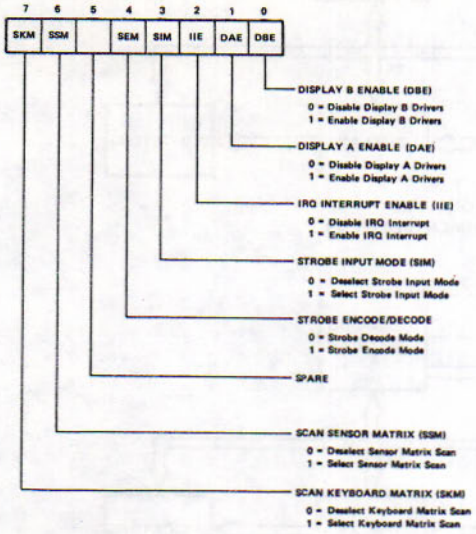
## R6541 INTERFACE SUMMARY

| Pin Name | No. | Description | Type |
|---|---|---|---|
| S0-S3 | 4 | Scan Outputs | Output |
| R0-R3 | 4 | Return Inputs | Input |
| BR4-BR7 | 4 | Display B Outputs/ Return Inputs | Bidirectional |
| B0-B3 | 4 | Display B Outputs | Output |
| A0-A7 | 8 | Display A Outputs | Output |
| D0-D7 | 8 | Data Bus | Bidirectional |
| $\overline{CS}$ | 1 | Chip Select | Input |
| RS | 1 | Register Select | Input |
| R/$\overline{W}$ | 1 | Read/$\overline{Write}$ | Input |
| Ø2 | 1 | Phase 2 Clock | Input |
| $\overline{RES}$ | 1 | Reset | Input |
| $\overline{IRQ}$ | 1 | Interrupt Request | Output |
| VCC, VSS | 2 | Power | Input |

## INTERFACE SIGNAL DESCRIPTION

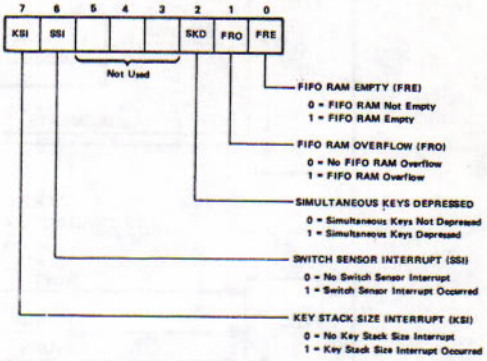
| Pin Name | No. of Lines | Description |
|---|---|---|
| S0-S3 | 4 | Scan Outputs. These lines scan, or strobe, the key switch or sensor matrix and display digits. The lines can be either encoded (1 of 16) or decoded (1 of 4). |
| R0-R3 | 4 | Return Inputs. These lines input the data from matrix type keys, static switches, or a strobed keyboard. The lines can be used as a 4-bit input or as part of an 8-bit input in conjunction with BR4-BR7. Each line has an active pullup resistance to keep it high until a switch closure pulls it low. |
| BR4-BR7 | 4 | Display B Outputs/Return Inputs. These bidirectional lines may be used either as an extension of the Return Inputs or as an extension of the Display B outputs. The lines are assigned as either inputs or outputs at system definition time; therefore, they may not be used as both inputs and outputs in a given application. These lines may also be used as an independent 4-bit output or an independent 4-bit input. Internal pullups are provided for use as inputs. In a scanned keyboard matrix application, BR6 and BR7 may be used as CONTROL and SHIFT, respectively. When used as outputs, these lines are driven from the 16 x 8 Display RAM B. When used as outputs, these lines are synchronized to the scan-outputs (S0-S3) for multiplexed digit displays. |
| B0-B3 | 4 | Display B Outputs. These lines are outputs from the 16 x 8 Display RAM B. The lines may be used as a 4-bit output port or may be considered as part of an 8-bit output port in conjunction with BR4-BR7. When used as outputs, these lines are synchronized to the scan outputs (S0-S3) for multiplexed digit displays. |
| A0-A7 | 8 | Display A Outputs. These lines are the outputs from the 16 x 8 Display RAM A. The lines may be used as an 8-bit output or two 4-bit outputs. When used as an output, these lines are synchronized to the scan outputs (S0-S3) for multiplexed digit displays. |
| D0-D7 | 8 | Data Bus. Eight bidirectional tri-state lines used to transfer all the data between the CPU and the R6541. |
| $\overline{IRQ}$ | 1 | Interrupt Request. This Interrupt Request output is used in the Keyboard or Strobe Input Modes to interrupt the CPU when driven to the low state. An external pullup resistor is required. |
| $\overline{RES}$ | 1 | Reset. This high impedance input line resets the R6541 to the power-on initialization condition when driven to the low state. |
| $\overline{CS}$ | 1 | Chip Select. This high impedance input line selects the R6541 when in the low state. |
| RS | 1 | Register Select. This high impedance input line is used to select specific R6541 registers. When low, the address Pointer can be written and the Status Register read. When high, the Address Pointer identifies the specific register to be used for data transfer. |
| R/$\overline{W}$ | 1 | Read/$\overline{Write}$. This high impedance line controls the transfer of data between the CPU and the R6541. When high (read), data is transferred from the R6541 to the CPU. When low (write), data is transferred from the CPU to the R6541. |
| Ø2 | 1 | Phase 2 Clock. This clock input signal is used to synchronize internal logic and generate internal timing. |
| VCC | 1 | Power. This input line supplies +5V ± 10% operating power. |
| VSS | 1 | Signal Ground. This line is power and signal return. |

The Control Register allows the CPU to select display and keyboard functions.

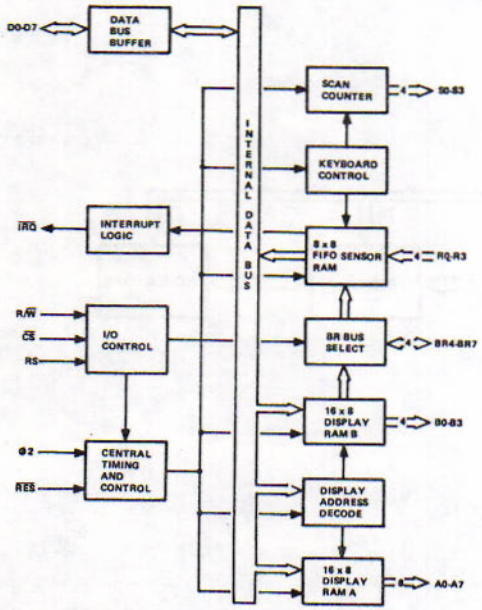



R6541 Control Register

The Status Register reports the status of various conditions and interrupts.




R6541 Status Register

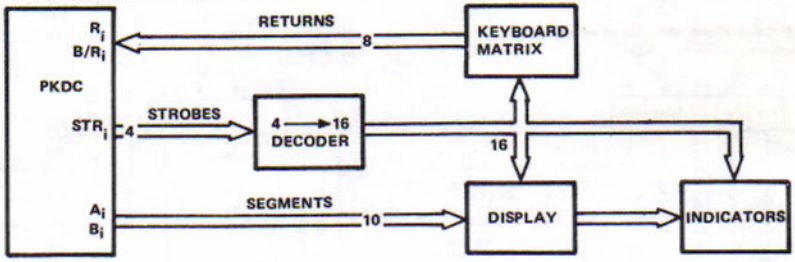



R6541 Block Diagram

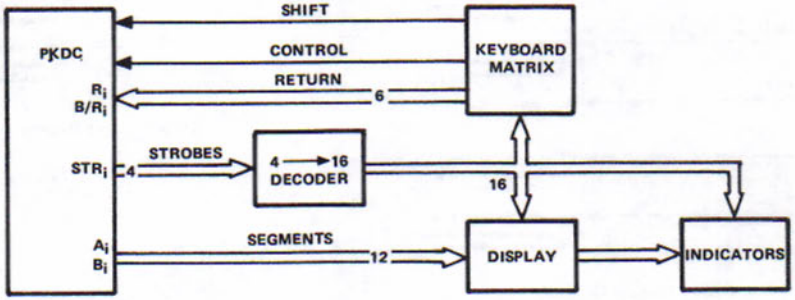
| Address Pointer |
|---|
| Status Register |
| RAM A0 Display |
| ↓ |
| RAM A15 Display |
| RAM B0 Display |
| ↓ |
| RAM B15 Display |
| FIFO/SENSOR RAM |
| FIFO SENSOR Address Pointer |
| FIFO/SENSOR Key Stack Size |
| Internal Clock |
| Keyboard Scan Time |
| Keyboard Debounce Time |
| Key Scan Time |
| Display Scan Time |
| Digit "On" Time |
| Segment "On" Time |
| Control Register |

R6541 Register Organization

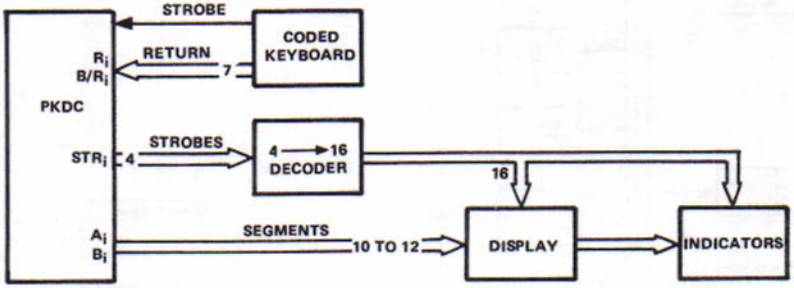
## APPLICATION EXAMPLES




128 KEY POSITIONS AND
16 CHARACTER (10 SEGMENT) DISPLAY




96 KEY POSITIONS WITH SHIFT, CONTROL AND
16 CHARACTER (12 SEGMENT) DISPLAY



DOCUMENT NO. 29000 P55
AUGUST 1978

PART NUMBER
**R6545**

Rockwell

# R6500 Microcomputer System

## PRODUCT PREVIEW

# CRT CONTROLLER (CRTC)





## DESCRIPTION

The R6545 CRT Controller (CRTC) is designed to interface an 8-bit microprocessor to CRT raster scan video displays. The R6545 adds an advanced CRT controller to the established and expanding line of R6500 products. The R6500 microcomputer system is produced with N-channel, silicon gate, depletion load technology.

Programmable internal registers generate video timing and display blanking signals.

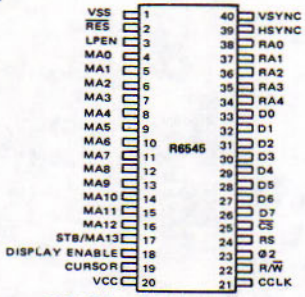
The R6545 provides refresh memory addresses and character generator row addresses which allow up to 16K characters with 32 scan lines per character to be addressed. A major advantage of the R6545 is that the refresh memory may be addressed in either straight binary or by row/column. Another feature is that the refresh memory may be configured as part of the microprocessor memory map or independently slaved to the R6545. This latter mode eliminates the need for address multiplexing and memory contention circuits by allowing the microprocessor to address any character location by loading the update register. By setting the address register to a special location and entering characters, the update address is automatically incremented to allow block loading. The flexibility of these operating modes allows the R6545 user to optimize hardware/software choices concerning character addressing and memory configuration.

Other functions in the R6545 include an internal cursor register which generates a cursor output when its contents are equal to the current refresh address. Programmable cursor start and end registers allow a cursor of up to the full character scan in height to be placed on any scan lines of the character. Variable cursor display blink rates are provided. A light pen strobe input allows capture of the current refresh address in an internal light pen register.

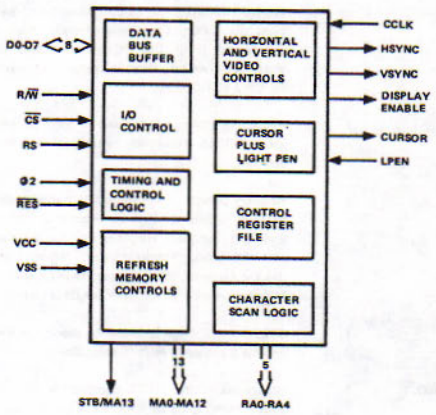
All timing for the video refresh memory signals is derived from the character clock input. Shift register, latch, and multiplex control signals (when needed) are provided by external high-speed timing. The mode control register allows interlaced, non-interlaced and interlaced plus video display modes at 50 or 60 Hz refresh rate. The internal status register may be used to monitor the R6545 operation.

## FEATURES

- Compatible with 8-bit microprocessors
- Refresh RAM may be configured in row/column or straight binary addressing
- Refresh RAM may be configured as part of microprocessor memory map or independently slaved to R6545
- Memory contention circuitry not required
- Output strobe pin to simplify refresh RAM read/update
- Alphanumeric and graphic capability
- Up and down scrolling by page, line, or character
- Fully programmable display (rows, columns, character matrix)
- Fully programmable scanning interlaced or non-interlaced at 50/60 Hz
- Fully programmable cursor
- Light pen register
- Addresses refresh RAM to 16K characters
- No external DMA required
- Internal status register
- 2 MHz or 1 MHz operation
- 40-Pin ceramic or plastic DIP
- Single +5 ±10% Volt Power Supply




R6545 Pin Configuration




R6545 Interface Diagram



Specifications subject to change without notice

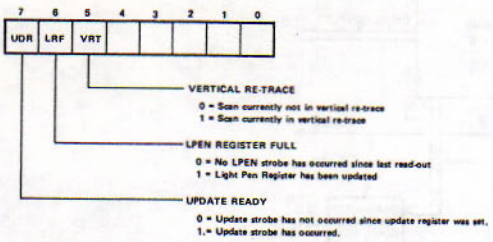
## R6545 INTERFACE SUMMARY

| Pin Name | No. | Description | Type |
|---|---|---|---|
| VSYNC | 1 | Vertical Sync | Output |
| HSYNC | 1 | Horizontal Sync | Output |
| DISPLAY ENABLE | 1 | Display Enable | Output |
| MA0-MA12 | 13 | Refresh Memory Address | Output |
| STB/MA13 | 1 | RAM Update Strobe/ Refresh Memory Address | Output |
| RA0-RA4 | 5 | Character Raster Address | Output |
| CCLK | 1 | Character Clock | Input |
| CURSOR | 1 | Cursor Character Position | Output |
| LPEN | 1 | Light Pen Strobe | Input |
| D0-D7 | 8 | Data Bus | Bidirectional |
| $\overline{CS}$ | 1 | Chip Select | Input |
| RS | 1 | Register Select | Input |
| Ø2 | 1 | Phase 2 Clock | Input |
| R/$\overline{W}$ | 1 | Read/$\overline{Write}$ | Input |
| $\overline{RES}$ | 1 | Reset | Input |
| VCC, VSS | 2 | Power | Input |

## INTERFACE SIGNAL DESCRIPTION

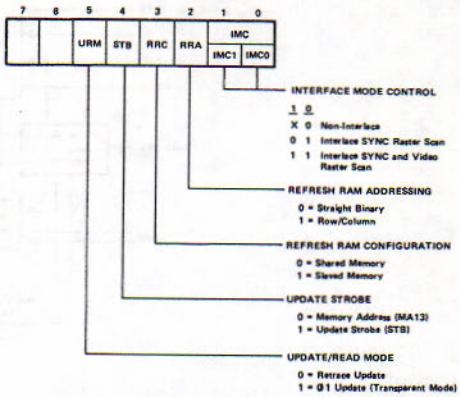
| Pin Name | No. of Lines | Description |
|---|---|---|
| D0-D7 | 8 | Data Bus. Eight-bit bidirectional data bus interface used to transfer control, data, and status information to and from the CPU. |
| Ø2 | 1 | Phase 2 Clock. High-impedance Phase 2 clock input. |
| R/$\overline{W}$ | 1 | Read/Write. High-impedance line used to control the direction of data transfer to and from the CPU. When high (read), data is transferred from the R6545 to the CPU. When low (write), data is transferred from the CPU to R6545. |
| $\overline{RES}$ | 1 | Reset. High-impedance input used to perform R6545 power-on initialization when driven to the low state. |
| RS | 1 | Register Select. High-impedance input used to gain access to R6545 registers. When low, the Address Register can be written and the Status Register read. When high, the contents of the Address Register identifies the register to be used for data transfer. |
| $\overline{CS}$ | 1 | Chip Select. High-impedance input. A low on this pin causes R6545 selection. |
| HSYNC | 1 | Horizontal Sync. TTL-compatible output, active high, used to determine the horizontal position of the displayed data. |
| VSYNC | 1 | Vertical Sync. TTL-compatible output, active high, used to determine the vertical position of the displayed data. |
| DISPLAY ENABLE | 1 | Display Enable. TTL-compatible output, active high, indicates that the R6545 is generating active display information. |
| CURSOR | 1 | Cursor Character Position. TTL-compatible output, active high, indicates that the current refresh address is equal to the cursor position. |
| CCLK | 1 | Character Clock. High-impedance input used to drive the R6545. This clock runs at the character rate and is normally derived from the dot clock generator. The active transition is the high-to-low edge of the signal. |
| LPEN | 1 | Light Pen Strobe. High-impedance strobe input used to latch the current character scan address (refresh RAM) into the internal Light-Pen register. Latching occurs on the high-to-low CCLK edge immediately after LPEN goes low. |
| MA0-MA13 STB/MA13 | 14 | Refresh Memory Address. TTL-compatible outputs used to address the refresh RAM (character storage). If the address organization selected is row/column, then MA0-MA7 becomes character column and MA8-MA13 becomes character row. The high order address pin (STB/MA13) functions as a strobe output pin when the R6545 is operating in the slaved memory mode. In this case the strobe (active high) is true at the time the refresh RAM update address is gated on to the address lines. In this way, updates and readouts of the refresh RAM can be made under control of the R6545 with minimal external circuitry. |
| RA0-RA4 | 5 | Character Raster Address. TTL-compatible outputs used to address the character ROM. These lines represent the row of the character currently being scanned in the display. |

The Status Register is used to monitor the status of the R6545.

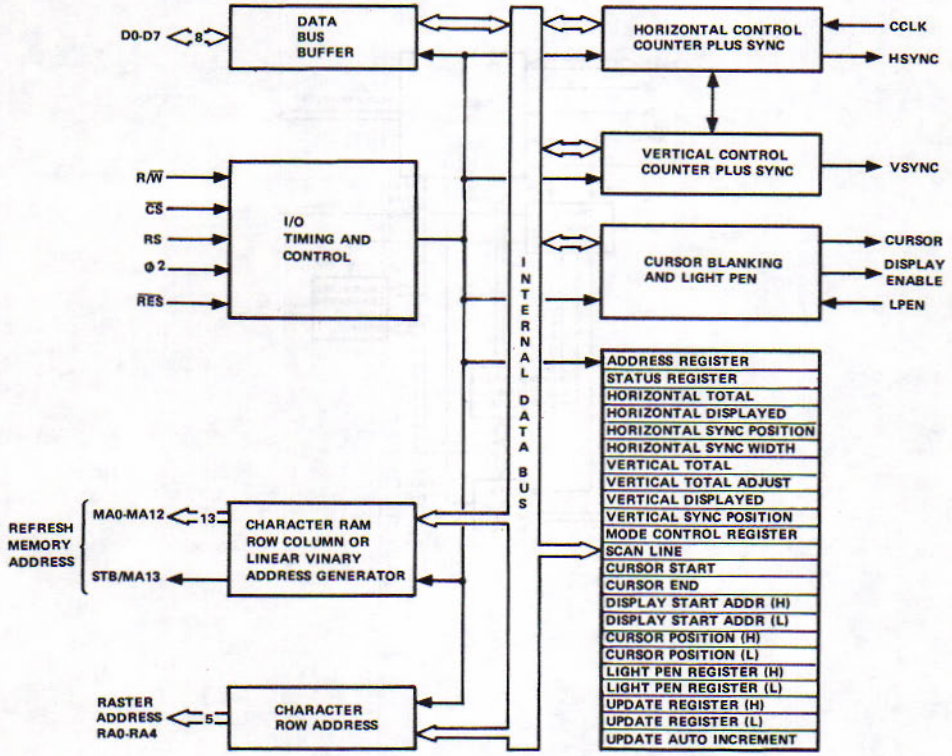



R6545 Status Register

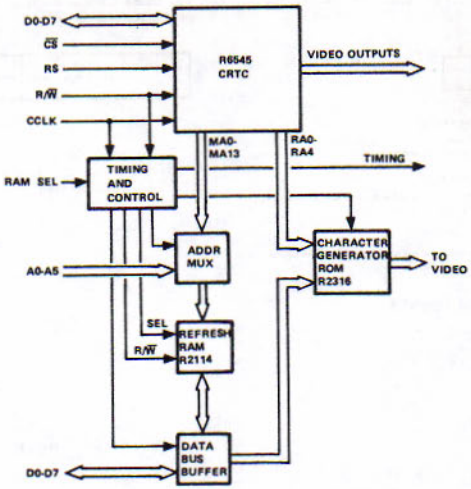
The Mode Control Register is used to select the operating modes of the R6545



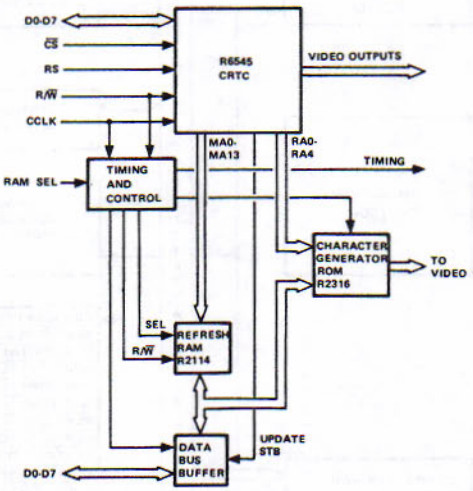

R6545 Mode Control Register




R6545 Block Diagram




Shared Memory Technique



Rockwell

# R6500 Microcomputer System
# DATA SHEET



## Asynchronous Communication Interface Adapter (ACIA)

The R6551 Asynchronous Communication Interface Adapter (ACIA) provides the interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

With its on-chip baud rate generator, the R6551 is capable of transmitting at 15 different program-selectable rates between 50 baud and 19,200 baud, and receiving at either the transmit rate or at 16 times an external clock rate. The R6551 has programmable word lengths of 5, 6, 7 or 8 bits; even, odd or no parity; 1, 1-1/2 or 2 start bits.

With the R6551, a crystal is the only required external support component — eliminating the multiple-component support that is typically needed.

In addition, the R6551 is designed for maximum programmed control from the CPU, to simplify hardware implementation. A control register and a separate command register permit the CPU to easily select the R6551's operating modes and data checks.

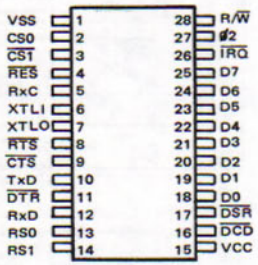
### FEATURES

- Compatible with 8-bit microprocessors
- Full duplex operation with buffered receiver and transmitter
- 15 Programmable Baud Rates (50 to 19,200)
- Receiver data rate may be identical to baud rate or may be 16 times the external clock input
- Data set/modem control functions
- Programmable word lengths, number of bit stops, and parity bit generation and detection
- Programmable interrupt control
- Selectable serial echo mode
- Two chip selects
- 2 MHz or 1 MHz clock rate
- Single +5V ±10% power supply
- 28-pin plastic or ceramic DIP
- Full TTL compatibility

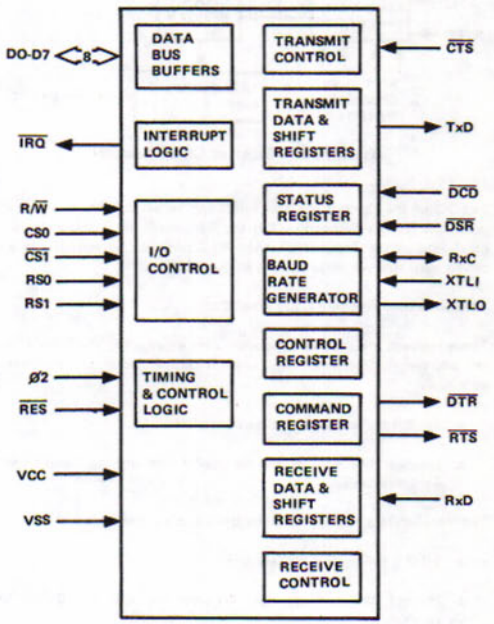
### Ordering Information

**Order Number:** R6551

- Temperature Range:
  - No suffix = 0°C to +70°C
  - E = -40°C to +85°C (Industrial)
- Package:
  - C = Ceramic
  - P = Plastic
- Frequency Range:
  - No suffix = 1 MHz
  - A = 2 MHz




R6551 Pin Configuration



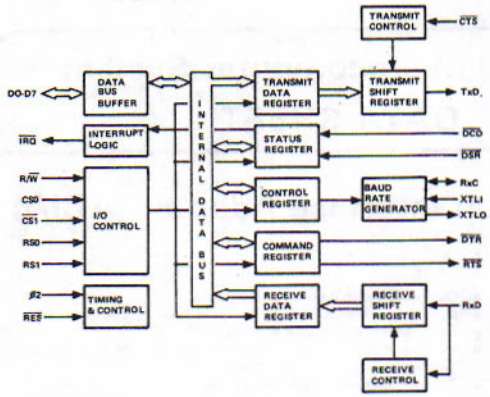

R6551 Interface Diagram





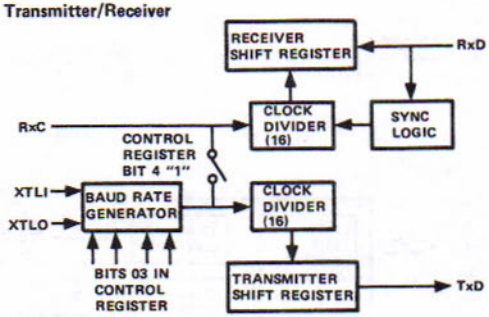
Specifications subject to change without notice

## INTERNAL ORGANIZATION




R6551 Block Diagram

### Transmitter/Receiver




Transmitter/Receiver Clock Circuits

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the R6551.

### Transmit and Receive Data Registers

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

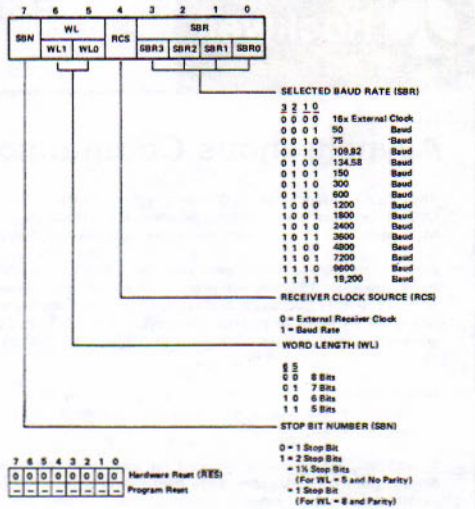
- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0"

### Control Register

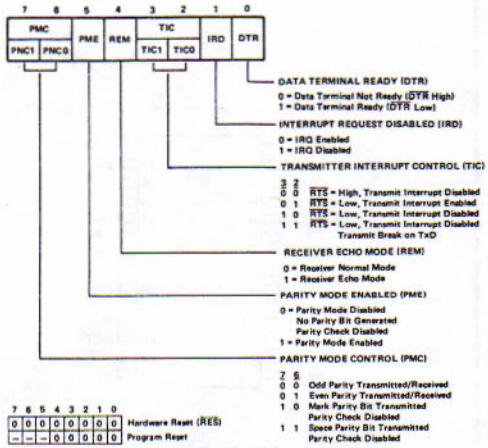
The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.




R6551 Control Register

### Command Register

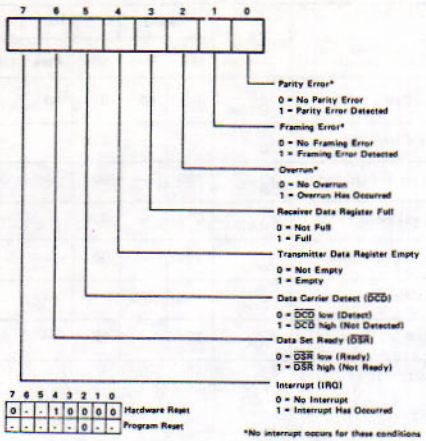
The Command Register controls specific modes and functions.




R6551 Command Register

### Status Register

The Status Register reports the status of various R6551 functions




**R6551 Status Register**

## INTERFACE SIGNAL DESCRIPTION

**$\overline{RES}$ (Reset)**

During system initialization a low on the $\overline{RES}$ input will cause internal registers to be cleared.

**Ø2 (Input Clock)**

The input clock is the system Ø2 clock and is used to trigger all data transfers between the system microprocessor and the R6551.

**R/$\overline{W}$ (Read/Write)**

The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the R6551. A low on the R/$\overline{W}$ pin allows a write to the R6551.

**$\overline{IRQ}$ (Interrupt Request)**

The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

**D0-D7 (Data Bus)**

The D0-D7 pins are the eight data lines used for transfer of data between the processor and the R6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

**CS0, $\overline{CS1}$ (Chip Selects)**

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The R6551 is selected when CS0 is high and $\overline{CS1}$ is low.

**RS0, RS1 (Register Selects)**

The two register select lines are normally connected to the processor address lines to allow the processor to select the various R6551 internal registers. The following table indicates the internal register select coding:

| RS1 | RS0 | Write | Read |
|---|---|---|---|
| 0 | 0 | Transmit Data Register | Receiver Data Register |
| 0 | 1 | Programmed Reset (Data is "Don't Care") | Status Register |
| 1 | 0 | Command Register | |
| 1 | 1 | Control Register | |

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the R6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$); these differences are described in the individual register definitions.

### ACIA/Modem Interface Signal Description

**XTLI, XTLO (Crystal Pins)**

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTLI pin, in which case the XTLO pin must float. XTLI is the input pin for the transmit clock.

**TxD (Transmit Data)**

The TxD output line is used to transfer serial NRZ (nonreturn-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

**RxD (Receive Data)**

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

**RxC (Receive Clock)**

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

**$\overline{RTS}$ (Request to Send)**

The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

**$\overline{CTS}$ (Clear to Send)**

The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

**$\overline{DTR}$ (Data Terminal Ready)**

This output pin is used to indicate the status of the R6551 to the modem. A low on $\overline{DTR}$ indicates the R6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

**$\overline{DSR}$ (Data Set Ready)**

The $\overline{DSR}$ input pin is used to indicate to the R6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready".

**$\overline{DCD}$ (Data Carrier Detect)**

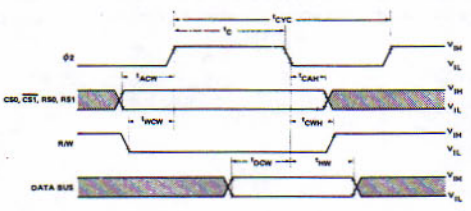
The $\overline{DCD}$ input pin is used to indicate to the R6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not.

## Write Cycle

($V_{CC}$ = 5.0V ±5%, $T_A$ = 0 to 70°C, unless otherwise noted)

| Characteristic | Symbol | 1 MHz | | 2 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Cycle Time | $t_{CYC}$ | 1.0 | 40 | 0.5 | 40 | µs |
| Ø2 Pulse Width | $t_C$ | 470 | — | 235 | — | ns |
| Address Set-Up Time | $t_{ACW}$ | 180 | — | 90 | — | ns |
| Address Hold Time | $t_{CAH}$ | 0 | — | 0 | — | ns |
| R/$\overline{W}$ Set-Up Time | $t_{WCW}$ | 180 | — | 90 | — | ns |
| R/$\overline{W}$ Hold Time | $t_{CWH}$ | 0 | — | 0 | — | ns |
| Data Bus Set-Up Time | $t_{DCW}$ | 300 | — | 150 | — | ns |
| Data Bus Hold Time | $t_{HW}$ | 10 | — | 10 | — | ns |

($t_r$ and $t_f$ = 10 to 30 ns)



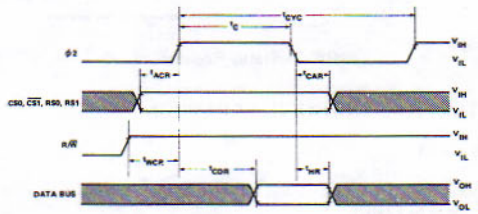

**Write Timing Characteristics**

## Read Cycle

($V_{CC}$ = 5.0V ±5%, $T_A$ = 0 to 70°C, unless otherwise noted)

| Characteristic | Symbol | 1 MHz | | 2 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Cycle Time | $t_{CYC}$ | 1.0 | 40 | 0.5 | 40 | µs |
| Pulse Width (Ø2) | $t_C$ | 470 | — | 235 | — | ns |
| Address Set-Up Time | $t_{ACR}$ | 180 | — | 90 | — | ns |
| Address Hold Time | $t_{CAR}$ | 0 | — | 0 | — | ns |
| R/$\overline{W}$ Set-Up Time | $t_{WCR}$ | 180 | — | 90 | — | ns |
| Read Access Time | $t_{CDR}$ | — | 395 | — | 200 | ns |
| Read Hold Time | $t_{HR}$ | 10 | — | 10 | — | ns |

($t_r$ and $t_f$ = 10 to 30 ns)



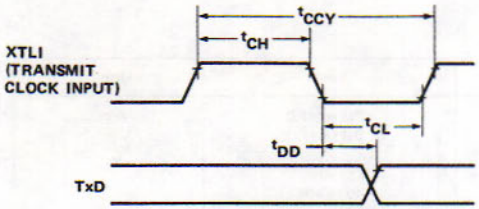

**Read Timing Characteristics**

## Transmit/Receive Characteristics

| Characteristic | Symbol | 1 MHz | | 2 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Transmit/Receive Clock Rate | $t_{CCY}$ | 0.5* | — | 0.5* | — | µs |
| Transmit/Receive Clock High Time | $t_{CH}$ | 235 | — | 235 | — | ns |
| Transmit/Receive Clock Low Time | $t_{CL}$ | 235 | — | 235 | — | ns |
| XTLI to TxD Propagation Delay | $t_{DD}$ | — | 500 | — | 500 | ns |
| $\overline{RTS}$ Propagation Delay | $t_{RTS}$ | — | 500 | — | 500 | ns |
| $\overline{IRQ}$ Propagation Delay (Clear) | $t_{IRQ}$ | — | 500 | — | 500 | ns |

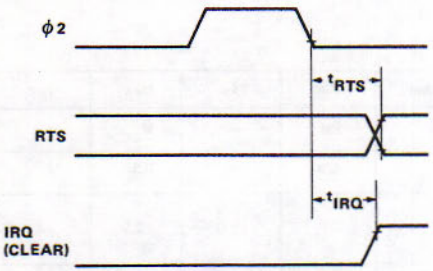
($t_r$, $t_f$ = 10 to 30 ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

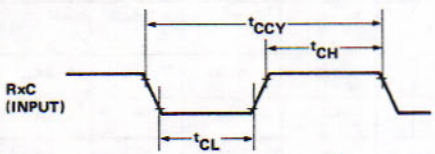



NOTE: TxD rate is 1/16 TxC rate

Transmit Timing with External Clock




Interrupt and RTS Timing

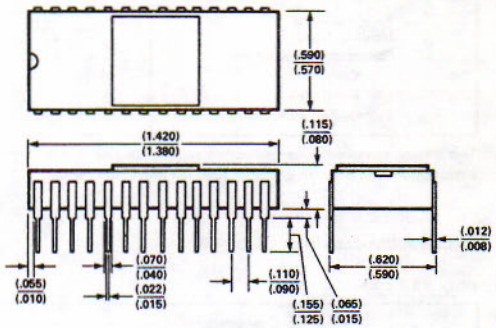



NOTE: RxD rate is 1/16 RxC rate

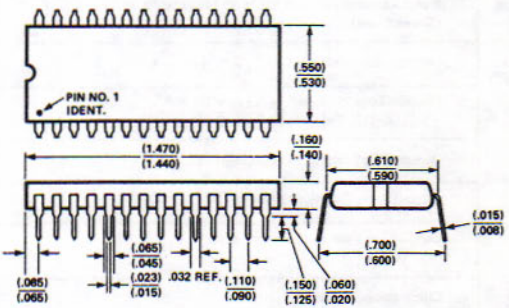
Receive External Clock Timing

## PACKAGE OUTLINES

### 28 LEAD CERAMIC




### 28 LEAD PLASTIC



## SPECIFICATIONS

### Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | -0.3 to +7.0 | Vdc |
| Operating Temperature | $T_A$ | | °C |
| Commercial | | 0 to +70 | |
| Industrial | | -40 to +85 | |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C |

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

### Electrical Characteristics

($V_{CC}$ = 5.0 ± 5%, $V_{SS}$ = 0)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 2.0 | – | $V_{CC}$ | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | – | 0.8 | V |
| Input Leakage Current: $V_{IN}$ = 0 to 5V. (Ø2, R/$\overline{W}$, $\overline{RES}$, CS0, $\overline{CS1}$, RS0, RS1, $\overline{CTS}$, RxD, $\overline{DCD}$, $\overline{DSR}$) | $I_{IN}$ | – | ±1.0 | ±2.5 | μA |
| Input Leakage Current for High Impedance State (Three State) | $I_{TSI}$ | – | ±2.0 | ±10.0 | μA |
| Output High Voltage: $I_{LOAD}$ = -100 μA | $V_{OH}$ | 2.4 | – | – | V |
| Output Low Voltage: $I_{LOAD}$ = 1.6 mA (D0-D7, TxD, RxC, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$) | $V_{OL}$ | – | – | 0.4 | V |
| Output High Current (Sourcing): $V_{OH}$ = 2.4V | $I_{OH}$ | -100 | -1000 | – | μA |
| Output Low Current (Sinking): $V_{OL}$ = 0.4V | $I_{OL}$ | 1.6 | – | – | mA |
| Output Leakage Current (off state): $V_{OUT}$ = 5V ($\overline{IRQ}$) | $I_{OFF}$ | – | 1.0 | 10.0 | μA |
| Clock Capacitance (Ø2) | $C_{CLK}$ | – | – | 20 | pF |
| Input Capacitance (except XTLI and XTLO) | $C_{IN}$ | – | – | 10 | pF |
| Output Capacitance | $C_{OUT}$ | – | – | 10 | pF |
| Power Dissipation | $P_D$ | – | 350 | 500 | mw |

# R6500

Memory-I/O
Combination Devices

DOCUMENT NO. 29000 D41
REV. 4, FEBRUARY 1979

PART NUMBER
**R6530**

Rockwell

# R6500 Microcomputer System DATA SHEET





## ROM-RAM-I/O-INTERVAL TIMER DEVICE (RRIOT)

### SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-channel, Silicon-Gate technology. Its performance speeds are enhanced by advanced system architecture. Its innovative architecture results in smaller chips – the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices. Rockwell also provides memory and I/O devices that further enhance the cost-effectivity of the R6500 microcomputer system . . . as well as low-cost design aids and documentation.

### FEATURES

- 8 bit bidirectional Data Bus for direct communication with the microprocessor
- 1024 x 8 ROM
- 64 x 8 static RAM
- Two 8 bit bidirectional data ports for interface to peripherals
- Two programmable Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Bus
- Allows up to 7K contiguous bytes of ROM with no external decoding

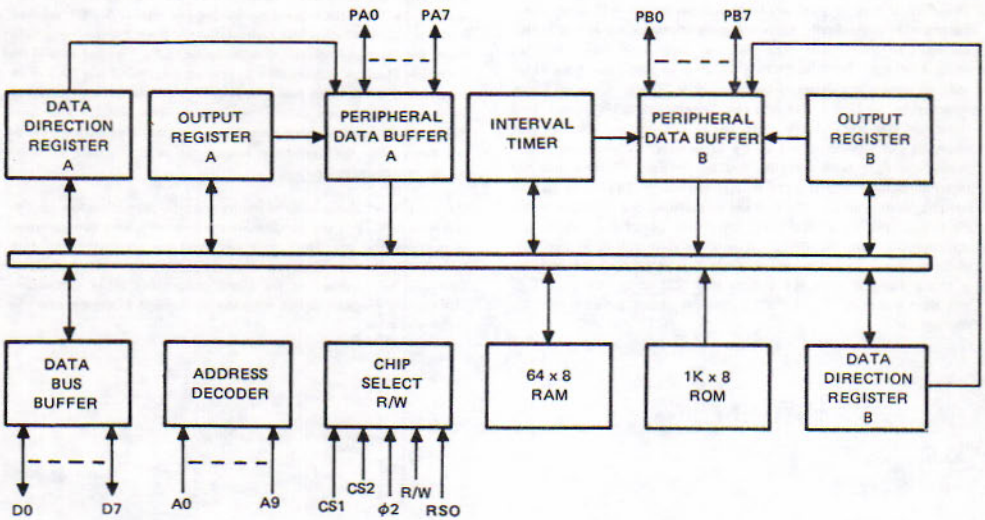
### DESCRIPTION

The R6530 is designed to operate in conjunction with the R6500 Microprocessor Family. It is comprised of a mask programmable 1024 x 8 ROM, a 64 x 8 static RAM, two software controlled 8 bit bidirectional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, and a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods.

**Ordering Information**

| Order Number | Package Type | Temperature Range |
|---|---|---|
| R6530P | Plastic | 0°C to +70°C |
| R6530C | Ceramic | 0°C to +70°C |

A custom number will be assigned by Rockwell.




R6530 Block Diagram



Specifications subject to change without notice

## INTERFACE SIGNAL DESCRIPTION

**Reset ($\overline{RES}$)**

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an off state during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

**Read/Write (R/W)**

The R/W signal is supplied by the microprocessor and is used to control the transfer of data to and from the microprocessor and the R6530. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the R6530. A low on the R/W pin allows a write (with proper addressing) to the R6530.

**Interrupt Request ($\overline{IRQ}$)**

The $\overline{IRQ}$ pin is an interrupt pin from the interval timer. This same pin, if not used as an interrupt, can be used as a peripheral I/O pin (PB7). When used as an interrupt, the pin should be set up as an input by the Data Direction Register. The pin will be normally high with a low indicating an interrupt from the R6530. An external pull-up device is not required; however, if collector-OR'd with other devices, the internal pullup may be omitted with a mask option.

**Data Bus (D0-D7)**

The R6530 has eight bidirectional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor. The output buffers remain in the off state except when selected for a Read operation.

**Peripheral Data Ports**

The R6530 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into two 8-bit ports, PA0-PA7 and PB0-PB7. PB5, PB6 and PB7 also have other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the Data Direction Register. A "1" into the Data Direction Register will cause its corresponding bit to be an output. When in the input mode, the Peripheral Data Buffers are in the "1" state and the internal pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the R6530 it receives data stored in the Output Register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts (for a "1") or less than 0.8 volts (for a "0") as the peripheral pins are all TTL compatible.

**Address Lines (A0-A9)**

There are 10 address pins (A0-A9). In addition, there is the ROM Select pin (RSO). Further, pins PB5 and PB6 are mask programmable, and can be used either individually or together as chip selects. When used as peripheral data pins they cannot be used as chip selects.

## INTERNAL ORGANIZATION

The R6530 is divided into four basic sections: RAM, ROM, I/O and Timer. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an Output Register.

**ROM 1K Byte (8K Bits)**

The 8K ROM is in a 1024 x 8 configuration. Address lines A0-A9, as well as RS0 are needed to address the entire ROM. With the addition of CS1 and CS2, seven R6530's may be addressed, giving 7168 x 8 bits of contiguous ROM.

**RAM – 64 Bytes (512 Bits)**

A 64 x 8 static RAM is contained on the R6530. It is addressed by A0-A5 (Byte Select), RS0, A6, A7, A8, A9 and, depending on the number of chips in the system, CS1 and CS2.

**Internal Peripheral Registers**

There are four internal registers, two data direction registers and two output registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral buffer pin as an output. Therefore, anything then written into the Output Register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data from the Output Register. For example, a "1" loaded into Data Direction Register A, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and remain in the high state. The two Data Output Registers are used to latch data from the Data Bus during a Write operation until the peripheral device can read the data supplied by the microprocessor.

During a Read operation the microprocessor is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the Output Register. The only way the Output Register data can be changed is by a microprocessor Write operation. The Output Register is not affected by a Read of the data on the peripheral pins.

### Interval Timer

The Timer section of the R6530 contains three basic parts: prescale divide down register, programmable 8-bit register and interrupt logic.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Timer Register.

At the same time that data is being written to the Interval Timer, the counting interval (1, 8, 64 or 1024T) is decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., $A_3$ = 1 enables IRQ on PB7, $A_3$ = 0 disables IRQ on PB7. When PB7 is to be used as an interrupt flag with the interval timer it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs PB7 will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

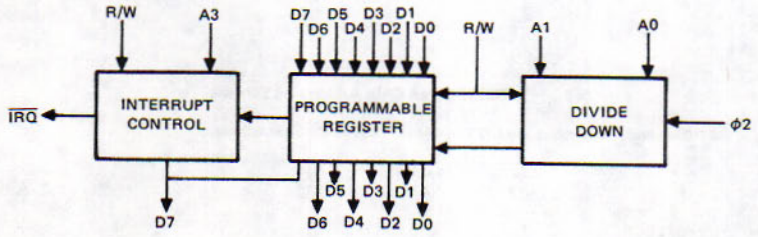
When the timer has counted down to 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the Timer Register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in one's complement.

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1 = 27

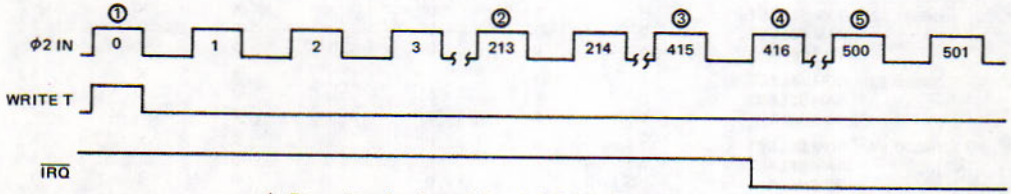
Thus, to arrive at the total elapsed time, merely do a one's complement and add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 417T + 27T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flag is read on DB7 all other DB outputs (DB0 thru DB6) go to "0".

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.




**Basic Elements of Interval Timer**




1. Data written into interval timer is 0 0 1 1 0 1 0 0 = $52_{10}$
2. Data in Interval timer is 0 0 0 1 1 0 0 1 = $25_{10}$
   $52 - \frac{213}{8} - 1 = 52-26-1 = 25$
3. Data in Interval timer is 0 0 0 0 0 0 0 0 = $0_{10}$
   $52 - \frac{415}{8} - 1 = 52-51-1 = 0$
4. Interrupt has occurred at Ø2 pulse #416
   Data in Interval timer = 1 1 1 1 1 1 1 1
5. Data in Interval timer is 1 0 1 0 1 1 0 0
   two's complement is 0 1 0 1 0 0 1 1 = $83_{10}$
   $83 + (52 \times 8) + 1 = 500_{10}$

## ADDRESSING

Addressing of the R6530 offers many variations to the user for greater flexibility. The user may configure his system with RAM in lower memory, ROM in higher memory, and I/O registers with interval timers between the extremes. There are 10 address lines (A0-A9). In addition, there is the possibility of 3 additional address lines to be used as chip-selects and to distinguish between ROM, RAM, I/O and interval timer. Two of the additional lines are chip-selects 1 and 2 (CS1 and CS2). The chip-select pins can also be PB5 and PB6. Whether the pins are used as chip-selects or peripheral I/O pins is a mask option and must be specified when ordering the part. Both pins act independently of each other in that either or both pins may be designated as a chip-select. The third additional address line is RSO. The R6502 and R6530 in a 2-chip system would use RSO to distinguish between ROM and non-ROM sections of the R6530. With the addressing pins available, a total of 7K contiguous ROM may be addressed with no external decode. Below is an example of a 1-chip and a 7-chip R6530 Addressing Scheme.

### One-Chip Addressing

A 1-chip system decode for the R6530 is illustrated on the top of the following page.

### Seven-Chip Addressing

In the 7-chip system the objective would be to have 7K of contiguous ROM, with RAM in low order memory. The 7K of ROM could be placed between addresses 65,535 and 1024. For this case, assume A13, A14 and A15 are all 1 when addressing ROM, and 0 when addressing RAM or I/O. This would place the 7K ROM between addresses 65,535 and 58,367. The 2 pins designated as chip-select or I/O would be masked programmed as chip-select pins. Pin RSO would be connected to address line A10. Pins CS1 and CS2 would be connected to address lines A11 and A12 respectively. See illustration below.

The two examples shown would allow addressing of the ROM and RAM; however, once the I/O or timer has been addressed, further decoding is necessary to select which of the I/O registers are desired, as well as the coding of the interval timer.

### I/O Register — Timer Addressing

Addressing Decode for I/O Register and Timer illustrates the address decoding for the internal elements and timer programming. Address lines A2 distinguishes I/O registers from the timer. When A2 is high and I/O timer select is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

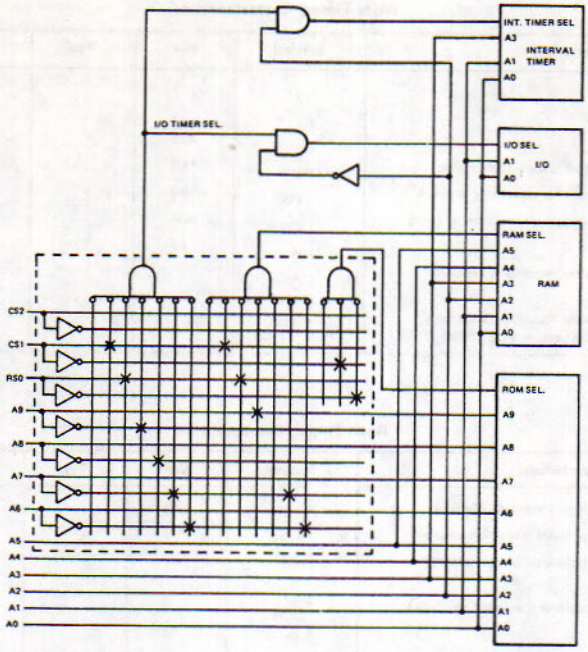
When the timer is selected A1 and A0 decode the divide by matrix. In addition, Address A3 is used to enable the interrupt flag to PB7.

### R6530 Seven Chip Addressing Scheme

The addressing of the ROM select, RAM select and I/O Timer select lines would be as follows:

| | | CS2 A12 | CS1 A11 | RSO A10 | A9 | A8 | A7 | A6 |
|---|---|---|---|---|---|---|---|---|
| R6530 #1, | ROM SELECT | 0 | 0 | 1 | X | X | X | X |
| | RAM SELECT | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | I/O TIMER | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| R6530 #2, | ROM SELECT | 0 | 1 | 0 | X | X | X | X |
| | RAM SELECT | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | I/O TIMER | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| R6530 #3, | ROM SELECT | 0 | 1 | 1 | X | X | X | X |
| | RAM SELECT | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | I/O TIMER | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| R6530 #4, | ROM SELECT | 1 | 0 | 0 | X | X | X | X |
| | RAM SELECT | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| | I/O TIMER | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| R6530 #5, | ROM SELECT | 1 | 0 | 1 | X | X | X | X |
| | RAM SELECT | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| | I/O TIMER | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| R6530 #6, | ROM SELECT | 1 | 1 | 0 | X | X | X | X |
| | RAM SELECT | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| | I/O TIMER | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| R6530 #7, | ROM SELECT | 1 | 1 | 1 | X | X | X | X |
| | RAM SELECT | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| | I/O TIMER | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

*RAM select for R6530 #5 would read = $\overline{A12} \bullet A11 \bullet \overline{A10} \bullet \overline{A9} \bullet A8 \bullet \overline{A7} \bullet \overline{A6}$




A. X indicates mask programming
i.e. ROM select = $\overline{CS1} \cdot RS0$
RAM select = $CS1 \cdot \overline{RS0} \cdot \overline{A9} \cdot A7 \cdot A6$
I/O TIMER SELECT = $CS1 \cdot \overline{RS0} \cdot A9 \cdot A8 \cdot A7 \cdot A6$

B. Notice that A8 is a don't care for RAM select

C. CS2 can be used as PB5 in this example.

**R6530 One Chip Address Encoding Diagram**

## Addressing Decode for I/O Register and Timer

| | Addressing Decode | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **ROM Select** | **RAM Select** | **I/O Timer Select** | **R/W** | **A3** | **A2** | **A1** | **A0** |
| Read ROM | 1 | 0 | 0 | 1 | X | X | X | X |
| Write RAM | 0 | 1 | 0 | 0 | X | X | X | X |
| Read RAM | 0 | 1 | 0 | 1 | X | X | X | X |
| Write DDRA | 0 | 0 | 1 | 0 | X | 0 | 0 | 1 |
| Read DDRA | 0 | 0 | 1 | 1 | X | 0 | 0 | 1 |
| Write DDRB | 0 | 0 | 1 | 0 | X | 0 | 1 | 1 |
| Read DDRB | 0 | 0 | 1 | 1 | X | 0 | 1 | 1 |
| Write Per. Reg. A | 0 | 0 | 1 | 0 | X | 0 | 0 | 0 |
| Read Per. Reg. A | 0 | 0 | 1 | 1 | X | 0 | 0 | 0 |
| Write Per. Reg. B | 0 | 0 | 1 | 0 | X | 0 | 1 | 0 |
| Read Per. Reg. B | 0 | 0 | 1 | 1 | X | 0 | 1 | 0 |
| Write Timer | | | | | | | | |
| ÷1T | 0 | 0 | 1 | 0 | * | 1 | 0 | 0 |
| ÷8T | 0 | 0 | 1 | 0 | * | 1 | 0 | 1 |
| ÷64T | 0 | 0 | 1 | 0 | * | 1 | 1 | 0 |
| ÷1024T | 0 | 0 | 1 | 0 | * | 1 | 1 | 1 |
| Read Timer | 0 | 0 | 1 | 1 | * | 1 | X | 0 |
| Read Interrupt Flag | 0 | 0 | 1 | 1 | X | 1 | X | 1 |

*$A_3$ = 1 Enables IRQ to PB7
$A_3$ = 0 Disables IRQ to PB7

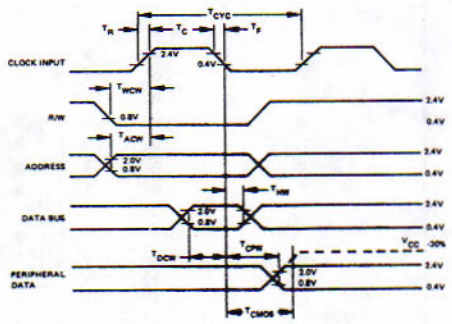
### Write Timing Characteristics

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Clock Period | $T_{CYC}$ | 1 | | 10 | μS |
| Rise & Fall Times | $T_R, T_F$ | | | 25 | ns |
| Clock Pulse Width | $T_C$ | 470 | | | ns |
| R/W valid before positive transition of clock | $T_{WCW}$ | 180 | | | ns |
| Address valid before positive transition of clock | $T_{ACW}$ | 180 | | | ns |
| Data Bus valid before negative transition of clock | $T_{DCW}$ | 300 | | | ns |
| Data Bus Hold Time | $T_{HW}$ | 10 | | | ns |
| Peripheral data valid after negative transition of clock | $T_{CPW}$ | | | 1 | μS |
| Peripheral data valid after negative transition of clock driving CMOS (Level = VCC - 30%) | $T_{CMOS}$ | | | 2 | μS |

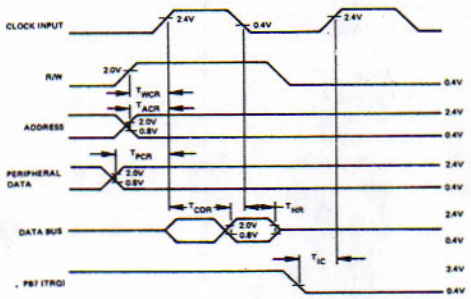
### Read Timing Characteristics

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R/W valid before positive transition of clock | $T_{WCR}$ | 180 | | | ns |
| Address valid before positive transition of clock | $T_{ACR}$ | 180 | | | ns |
| Peripheral data valid before positive transition of clock | $T_{PCR}$ | 300 | | | ns |
| Data Bus valid after positive transition of clock | $T_{CDR}$ | | | 395 | ns |
| Data Bus Hold Time | $T_{HR}$ | 10 | | | ns |
| IRQ (Interval Timer Interrupt) valid before positive transition of clock | $T_{IC}$ | 200 | | | ns |

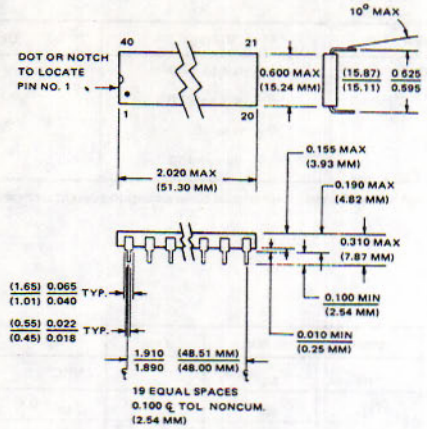
Loading = 30 pF + 1 TTL load for PA0-PA7, PB0-PB7
= 130 pF + 1 TTL load for D0-D7




Write Timing Characteristics

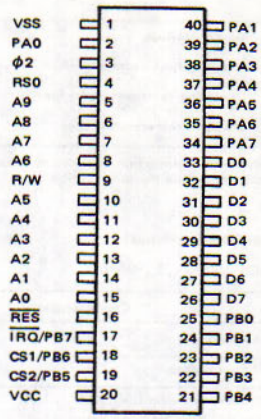



Read Timing Characteristics




NOTE: - Pin No. 1 is in lower left corner when symbolization is in normal orientation

**Packaging Diagram**




**Pin Configuration**

## SPECIFICATIONS

### Maximum Ratings

| Rating | Symbol | Voltage | Unit |
|---|---|---|---|
| Supply Voltage | VCC | -0.3 to +7.0 | V |
| Input/Output Voltage | $V_{IN}$ | -0.3 to +7.0 | V |
| Operating Temperature Range | $T_{OP}$ | 0 to 70 | °C |
| Storage Temperature Range | $T_{STG}$ | -55 to +150 | °C |

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

### Electrical Characteristics

(VCC=5.0%, VSS=0V, $T_A$=25°C)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | $V_{SS}$ + 2.4 | | VCC | V |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$ - 0.3 | | $V_{SS}$ + 0.4 | V |
| Input Leakage Current; $V_{IN}$ = $V_{SS}$ + 5V<br>A0-A9, RS, R/W, $\overline{RES}$, 02, PB6*, PB5* | $I_{IN}$ | | 1.0 | 2.5 | μA |
| Input Leakage Current for High Impedance State<br>(Three State); $V_{IN}$ = 0.4V to 2.4V; D0-D7 | $I_{TSI}$ | | ±1.0 | ±10.0 | μA |
| Input High Current; $V_{IN}$ = 2.4V<br>PA0-PA7, PB0-PB7 | $I_{IH}$ | -100. | -300. | | μA |
| Input Low Current; $V_{IN}$ = 0.4V<br>PA0-PA7, PB0-PB7 | $I_{IL}$ | | -1.0 | -1.6 | MA |
| Output High Voltage<br>VCC = MIN, $I_{LOAD}$ ≤ -100 μA (PA0-PA7, PB0-PB7, D0-D7)<br>$I_{LOAD}$ ≤ -3 MA (PA0-PB0) | $V_{OH}$ | <br>VSS + 2.4<br>VSS + 1.5 | | | V |
| Output Low Voltage<br>VCC = MIN, $I_{LOAD}$ ≤ 1.6 MA | $V_{OL}$ | | | VSS + 0.4 | V |
| Output High Current (Sourcing);<br>VOH ≥ 2.4V (PA0-PA7, PB0-PB7, D0-D7)<br>≥ 1.5V Available for other than TTL<br>(Darlingtons) (PB0, PB7) | $I_{OH}$ | <br>-100<br>-3.0 | <br>-1000<br>-5.0 | | <br>μA<br>MA |
| Output Low Current (Sinking); VOL ≤ 0.4V (PA0-PA7)<br>(PB0-PB7) | $I_{OL}$ | 1.6 | | | MA |
| Clock Input Capacitance | $C_{Clk}$ | | | 30 | pF |
| Input Capacitance | $C_{IN}$ | | | 10 | pF |
| Output Capacitance | $C_{OUT}$ | | | 10 | pF |
| Power Dissipation | $P_D$ | | 500 | 1000 | MW |

*When programmed as address pins
All values are D.C. readings

DOCUMENT NO. 29000D52
REV. 2, FEBRUARY 1979

PART NUMBER
R6531

Rockwell

# R6500 Microcomputer System
# DATA SHEET





## ROM-RAM-I/O-COUNTER (RRIOC)

### SYSTEM ABSTRACT

The ROM-RAM-I/O Counter (RRIOC), Part Number R6531, further enhances the cost-effectivity of the R6500 NMOS 8-bit microcomputer system by providing a powerful, flexible two-chip minimum system option. Produced with N-channel depletion load, silicon gate technology, the R6500 system employs advanced architecture, including 13 instruction addressing modes to achieve third generation performance speeds and smaller chips, the threshold to lower hardware and design costs. Included in the R6500 system are 10 software-compatible microprocessor (CPU) options, a growing number of memory and I/O devices, a very efficient, low-cost SYSTEM 65 development aid and complete documentation.

### DESCRIPTION

The R6531 is primarily designed to provide innovative Equipment Designers with a wide span of two-chip minimum systems in combination with the R6500 family of 10 CPUs. It can also be combined in a variety of multi-chip system configurations with other R6531's, ROMs, RAMs and other I/O devices.

There are two R6531 versions: a 40-pin dual-in-line package; another with expanded I/O in a compact 52-pin quad-in-line package — see Table 1. Both versions contain a 2048 x 8 mask-programmable ROM, a 128 x 8 static RAM, a software programmable multi-mode counter, an 8-bit serial data channel, and 15 bidirectional data lines (two ports) with a handshake control mode and four interrupt inputs. The 52-pin version has an 8-bit output port and a 4-bit input port for a total of 27 I/O lines. Several mask options are available to provide a RAM standby power pin and chip selects for multi-chip systems — see Figure 1.

Prototyping circuits are available in both the 40- and 52-pin packages, and in 1- and 2-MHz versions. They are offered as part numbers R6531-098 and R6531-098A for the 40-pin part, and as part numbers R6531-099 and R6531-099A for the 52-pin part.

### FEATURES

- 2048 x 8 mask programmable ROM
- 128 x 8 static RAM
- 16-bit multi-mode counter/latch
  - interval timer (one shot or free running)
  - pulse generator (one shot or free running)
  - event counter
  - external trigger
- 8-bit serial channel
- TTL compatible I/O, drive one TTL load
- 15 bidirectional I/O lines (2 ports — 40 pin package)
- Expansion 8-bit output port and 4-bit input port (52 pin package)
- I/O handshake control
- Four edge sensitive interrupt inputs
- 2 MHz or 1 MHz operation
- Single +5V power supply

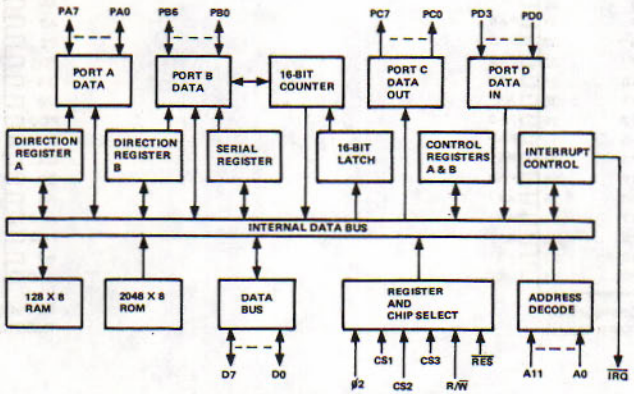
**Table 1 Ordering Information**

Order Number: R6531

Temperature Range:
- No suffix = 0°C to +70°C
- E = −40°C to +85°C (Industrial)

Package:
- C = 40-Pin DIP, Ceramic
- P = 40-Pin DIP, Plastic
- Q = 52-Pin QUIP, Plastic

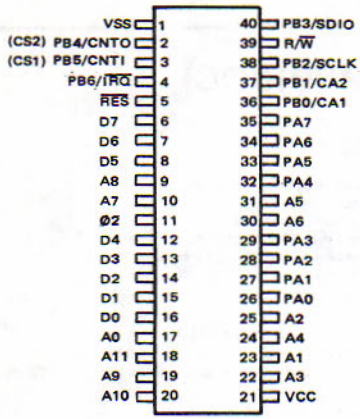
Frequency Range:
- No suffix = 1 MHz
- A = 2 MHz



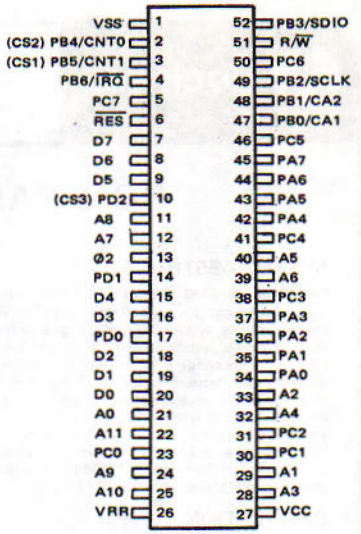

R6531 Block Diagram



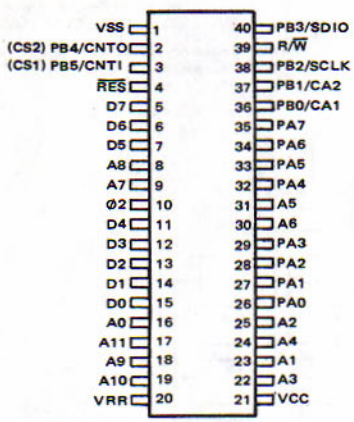
Specifications subject to change without notice



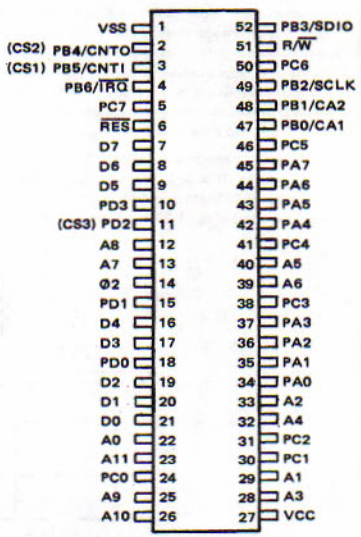

**40- Pin Configuration**
**R6531, PB6 Option**




**52-Pin Configuration**
**R6531Q, VRR Option**




**40-Pin Configuration**
**R6531, VRR Option**




**52-Pin Configuration**
**R6531Q, PD3 Option**

**Figure 1. R6531 Pin Configuration Options**

## INTERFACE SIGNALS

### RESET ($\overline{RES}$)

This active, low signal is used to initialize the R6531. It clears all internal registers (except the counter and serial registers) to logic zero. This action places all bidirectional I/O lines in the input state and the Port C outputs in the high state. The timer, shift register, and interrupts are disabled. The $\overline{RES}$ signal must be low for at least four clock periods when reset is required.

### ADDRESS BUS (A0-A11) AND CHIP SELECTS (CS1-CS3)

Memory and register selection is accomplished using the 12 address lines and in multiple device systems also using one or more of the three Chip Select mask options. When PB4, PB5, or PD2 are chosen as chip selects, they cannot be used as peripheral I/O pins.

### DATA BUS (D0-D7)

The R6531 has eight data bus lines. These lines connect to the microcomputers data bus and allow transfer of data to or from the microprocessor. The output buffers remain in the off-state except when the R6531 is selected for a read operation.

### READ/WRITE (R/$\overline{W}$)

The R/$\overline{W}$ signal is supplied by the microprocessor and is used to control the transfer of data to and from the microprocessor and the R6531. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the data supplied by the R6531. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the R6531.

### PERIPHERAL DATA PORTS (PA0-PA7, PB0-PB6, PC0-PC7, PD0-PD3)

Both versions of the R6531 have 15 pins available for peripheral I/O operations. Each pin is software programmable to act as an input or an output. The pins are grouped into an 8-bit port, PA0-PA7, and a 7-bit port, PB0-PB6. The lines of the PB port may serve other functions. Ports PA and PB have associated data direction registers.

The expanded I/O of the 52-pin version provides an 8-bit output only port, PC0-PC7, and a 4-bit input only port, PD0-PD3. PD2 and PD3 may be assigned other functions as described herein.

The outputs are push/pull type drivers capable of driving a single TTL load. When inputs are selected the lines float. If PB6 is programmed as the $\overline{IRQ}$ request output, the line is driven low and requires an external pull-up, thus allowing the wire OR-ing of $\overline{IRQ}$ from other devices.

### RAM RETENTION VOLTAGE (VRR)

A separate pin for a power supply for the read/write memory is available as a mask option. This allows the retention of RAM data by using a battery back-up for the RAM only. Pin PB6 in the 40-pin version or PD3 in the 52-pin version is mask programmable as the VRR pin. Address line A10 must be held in the logic state which deselects RAM (user-defined) in order to protect the RAM data when VCC falls below the specified level or is turned off.

## INTERNAL ORGANIZATION

The R6531 is divided into three basic functions: ROM, RAM, and I/O. The selection of any one of these three is accomplished by issuing the appropriate address information on the address bus when the chip is selected.

### ADDRESSING

Addressing of the R6531 offers many variations to the user for system configuration flexibility. Combination with other R6531's, ROMs, RAMs or I/O devices is possible without need for external address decoding. Each of the three basic functions on the device has its own decode mask for unique selection.

The specific address ranges and chip selects are defined by the user and are dependent on the number of chips in the system. The programmed options to be fixed by masking are:

| R6531 Function | Chip Selects | | | Address Inputs (A0-A11) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CS3 | CS2 | CS1 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ROM | X | X | X | X | 2K ROM Decode | | | | | | | | | | |
| RAM | Y | Y | Y | Y | Y | Y | Y | Y | 128 RAM Decode | | | | | | |
| I/O | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | I/O Decode | | |

The X, Y, and Z bits may be selected as high, low or no effect.

The chip select pins are also discrete I/O pins PB5, PB4, and PD2. The pins are independent of each other in that any one may be used as a chip select. The user specifies as mask options which pins are to be used as I/O and which as chip selects.

### ROM – 2K BYTES (16K BITS)

The 16K ROM is a 2048 x 8 bit configuration. An address on lines A0-A10 uniquely selects one byte of ROM. Additionally, address line A11 and the chip selects are required to select the ROM function on a given chip. In a system with multiple R6531's, the CS1, CS2, and CS3 mask options allow up to seven devices with 14K bytes of ROM without the need for external decoding.

### RAM – 128 BYTES (1024 BITS)

The 128 x 8 static RAM of a given R6531 is addressed by lines A0-A6. Additionally, address lines A7-A11 and chip selects CS1, CS2, and CS3 provide selection of the RAM section of the device as well as the device itself when additional RAM devices or R6531's are in the system.

### R6531 40 PIN PROTOTYPING CIRCUIT

Prototyping circuits R6531-098 (1 MHz) and R6531-098A (2 MHz) are packaged in a 40-pin dual in-line package, and has the same pin-outs as the 40-pin R6531 with PB6 option. In this prototyping circuit, the ROM is disabled and there is no VRR option.

Access codes for this prototyping circuit are shown in the table below.

| R6531-098 Function | Chip Selects | | Address Inputs (A0 - A11) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CS2 | CS1 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RAM | N | N | L | L | L | N | L | 128 RAM Decode | | | | | | |
| I/O | N | N | L | H | H | H | L | L | L | L | L | I/O Decode | | |

In the above table, N means No Effect; H means High (2.4 volts or greater) and L means Low (0.4 volt or less).

### R6531 52-PIN PROTOTYPING CIRCUIT

Prototyping circuits R6531-099 (1 MHz) and R6531-099A (2 MHz) are packaged in the 52-pin quad in-line package, with VRR option. PD2 is used as a chip select (CS3), and PB4 and PB5 are available as I/O lines.

Access codes for the prototyping circuit are shown in the table below.

| R6531-099 Function | Chip Selects | | | Address Inputs (A0-A11) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CS3 | CS2 | CS1 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ROM | H | N | N | H | 2K ROM Decode | | | | | | | | | | |
| RAM | L | N | N | L | L | L | N | L | 128 RAM Decode | | | | | | |
| I/O | L | N | N | L | H | H | H | L | L | L | L | I/O Decode | | | |

The 128 words of RAM have been mapped into the first half of both Page 0 and Page 1, to accomodate zero page addressing and stack operations. The full I/O capabilities described for the R6531 are available in the prototyping circuit, except that I/O lines PD2 and PD3 are dedicated to the VRR and CS3 mask options.

## INPUT/OUTPUT

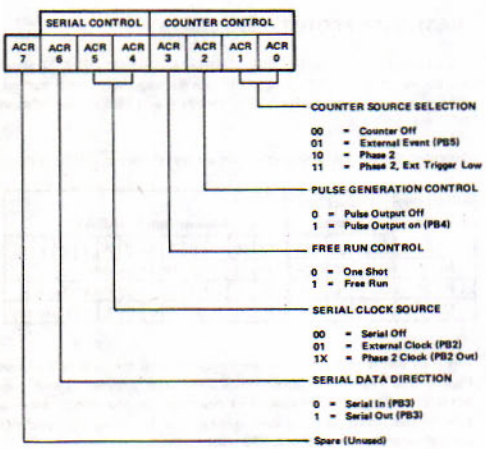
The input/output section is comprised of the data ports, direction registers, counter and associated latches, control registers, and interrupt registers. These I/O functions are all accessible by the R6502 CPU's instruction set using address bits A0-A3 for the specific function of the device. Address bits A4-A11 and CS1, CS2, and CS3 additionally may be decoded to select a given R6531 device in a multichip system. The addresses of the 15 internal peripheral registers are:

| A3 | A2 | A1 | A0 | Register |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Port A |
| 0 | 0 | 0 | 1 | Port B |
| 0 | 0 | 1 | 0 | Port C (write only) |
| 0 | 0 | 1 | 1 | Port D (read only) |
| 0 | 1 | 0 | 0 | Read Lower Counter/Write Lower Latch |
| 0 | 1 | 0 | 1 | Read Upper Counter/Write Upper Latch and Download |
| 0 | 1 | 1 | 0 | Write Lower Latch |
| 0 | 1 | 1 | 1 | Write Upper Latch |
| 1 | 0 | 0 | 0 | Serial Data Register |
| 1 | 0 | 0 | 1 | Interrupt Flag Register |
| 1 | 0 | 1 | 0 | Interrupt Enable Register |
| 1 | 0 | 1 | 1 | Auxiliary Control Register |
| 1 | 1 | 0 | 0 | Peripheral Control Register |
| 1 | 1 | 0 | 1 | *Data Direction Register – Port A |
| 1 | 1 | 1 | 0 | *Data Direction Register – Port B |

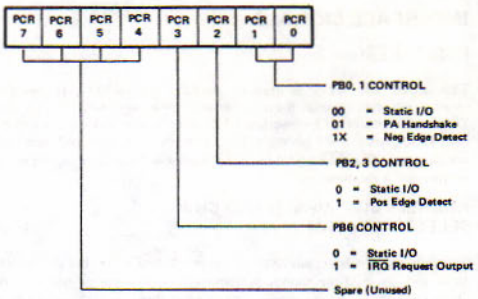
* Write Only

## CONTROL REGISTERS

Two control registers, Peripheral Control and Auxiliary Control, are provided for software selection of various I/O functions. The Peripheral Control Register is primarily associated with Port B functions and the Auxiliary Control Register is associated with the counter and serial data functions which also affect Port B. The register bit assignments are:




Auxiliary Control Register (ACR)




Peripheral Control Register (PCR)

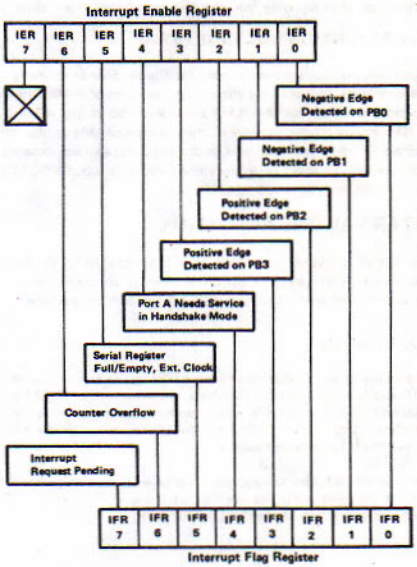
## INTERRUPT ENABLE AND FLAG REGISTERS

Two registers are provided for interrupt control. Corresponding bits in the enable and flag registers are logically ANDed to set the Interrupt Request Pending flag. If the pending flag is set and PB6 is selected as an $\overline{\text{IRQ}}$ Request Output, then PB6 will be set low to request the R6502 CPU to service $\overline{\text{IRQ}}$.

The interrupt enable bits are set or reset by writing into the Interrupt Enable Register. The interrupt flag bits IFR0-IFR6 can be cleared directly by writing a byte to the flag register which has 1's in those bit positions to be cleared.

IFR4 and IFR5 may also be cleared by reading or writing the Port A or Serial Data Registers respectively. IFR6 may also be cleared by reading the lower counter with I/O address hex 4 or writing the upper latch with I/O addresses hex 5 or 7.

These registers and their bit assignments are:



## PERIPHERAL DATA PORTS

Each line of the 8-bit data Port A may be individually selected as an input or output. Associated with the port is Data Direction Register – Port A (DDRA). Each line of the 7-bit date Port B may be individually selected as an input or an output. This port also has a Data Direction Register (DDRB). The two data direction registers (A and B) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral pin as an output. Therefore, anything written into the data register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data from the data register. For example, a "1" loaded into DDRA, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and would be in a float state.

Note that when lines in the PB port are used alternately as control lines for other on-chip functions, Direction Register B must also be loaded to set up the proper direction – the Control Registers have no effect on data direction.

The 8-bit data Port C is an output only port. The 4-bit data Port D is an input only port.

For those lines being used as outputs, the data registers are used to latch data from the Data Bus during a Write operation so the peripheral device can read the data supplied by the microprocessor.

For the lines being used as inputs, the microprocessor is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the Output data.

## EDGE DETECT LOGIC

Operating in parallel with the I/O operation of PB0-PB3 is edge detect logic that is enabled by Peripheral Control Register bits 1 and 2. PCR1 enables logic that upon detection of a negative edge on PB0 or PB1 will set a corresponding flag in the Interrupt Flag Register. PCR2 enables logic that upon detection of a positive edge on PB2 or PB3 will set corresponding flags in the Interrupt Flag Register. If corresponding bits are set in the Interrupt Enable Register, then the Interrupt Request Pending flag will be set.

## MULTI-MODE COUNTER/LATCH

The R6531 contains a 16-bit counter with an associated 16-bit latch whose modes are software selectable by setting appropriate bits in the Auxiliary Control Register. The latch holds the counter preset value and all 16 bits download to the counter simultaneously upon command (I/O address hex 5) of the software or automatically in free run modes upon overflow of the counter. The counter is a decrementing counter and causes the setting of a flag in the Interrupt Flag Register when it overflows. This interrupt flag, bit 6, is logically ANDed with a corresponding counter overflow interrupt enabled bit to set the Interrupt Request Pending flag. The Auxiliary Control Register is used to set four basic modes which specify the source of the count information, and to select two mode modifiers that apply equally to the three active modes.

Mode 0 – Counter Off

Mode 1 – Event Counter – counts external event inputs (negative transitions) at PB5

Mode 2 – Interval Timer – counts Ø2 system clock pulses.

Mode 3 – External Trigger – counts Ø2 system clock pulses starting with a negative transition on PB5.

Mode Modifier A – Pulse Generation Control – causes the output level on PB4 to switch low each time the counter is loaded using I/O address hex. 5. At counter overflow, PB4 switches high. If in the free run mode, PB4 continues to toggle at each subsequent counter overflow; otherwise there are no further transitions until the counter is reactivated by the software.

Mode Modifier B – Free Run Control – causes the full 16-bit latch to be downloaded to the counter, continues to count, and sets the counter overflow flag bit every time the counter overflows. Otherwise the counter is a one shot mode in which the counter overflow flag is set one time only until the counter is reactivated by the software.

## SERIAL DATA CHANNEL

The R6531 has an 8-bit serial channel. PB2 and PB3 are software selectable as the serial clock (SCLK) and serial data (SDIO) lines respectively.

The software sets Auxiliary Control Register bits 4 and 5 to enable the serial channel and to specify the source of the shift clock. Selection of the internal clock will shift data at one half the system Ø2 clock rate. If the external clock is used, data may be shifted at any rate up to one half the system Ø2 clock rate. In the external clock mode, the counter may be operated in the free run pulse generator mode using the CNTO line externally connected to the SCLK line to provide the desired shift rate.

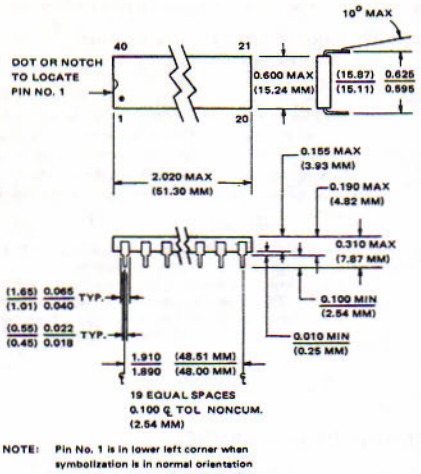
Auxiliary Control Register bit 6 sets the serial data direction. Data are shifted in or out with the most significant bit first under control of the shift clock.

In the external clock mode, the completion of eight shifts of the serial register will set bit 5 of the interrupt flag register. If the corresponding bit of the Interrupt Enable Register is also set an Interrupt Request Pending flag will be set.

## HANDSHAKE OPERATIONS

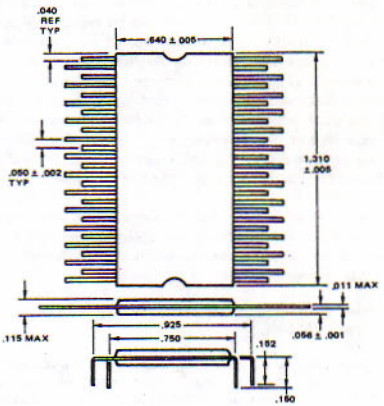
PB0 and PB1 may be used as handshake control lines for date transmissions over Port PA; see PCR definition. PB0 is a control input, PB1 is a control output. PB1 switches low on a read or write to Port PA, and switches high in response to a negative transition on PB0.

IFR4 in the Flag Register is set by a negative transition on PB0, and cleared by a Read or Write to Port PA; see Handshake Timing Diagram for timing details.

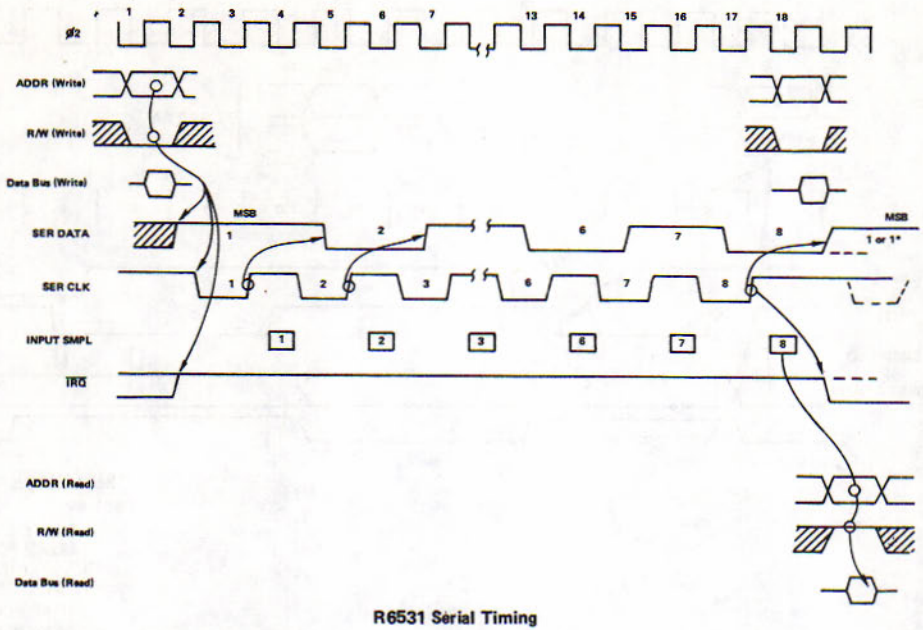



NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

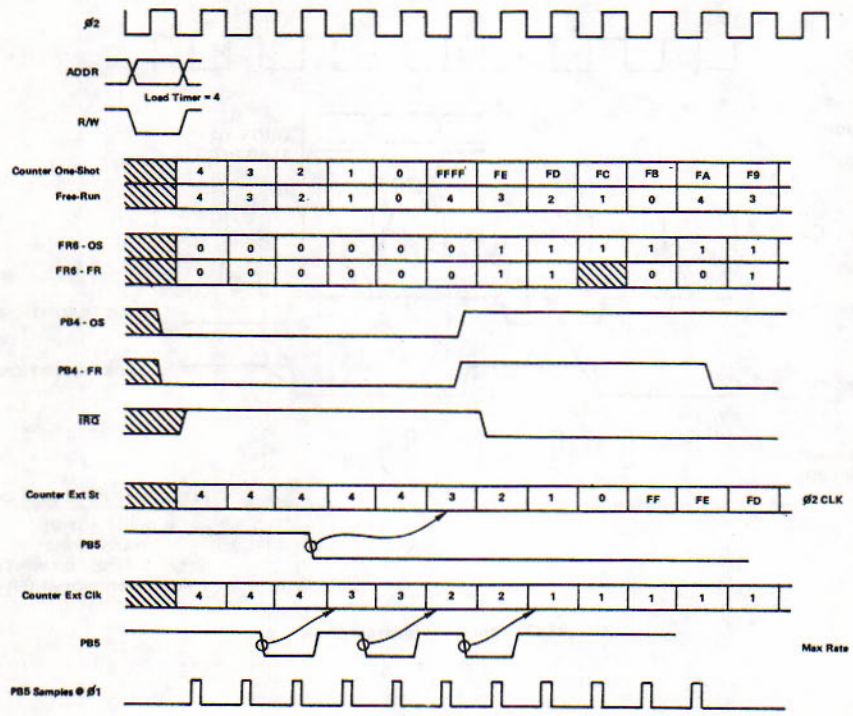
**40-Pin Packaging Diagram**



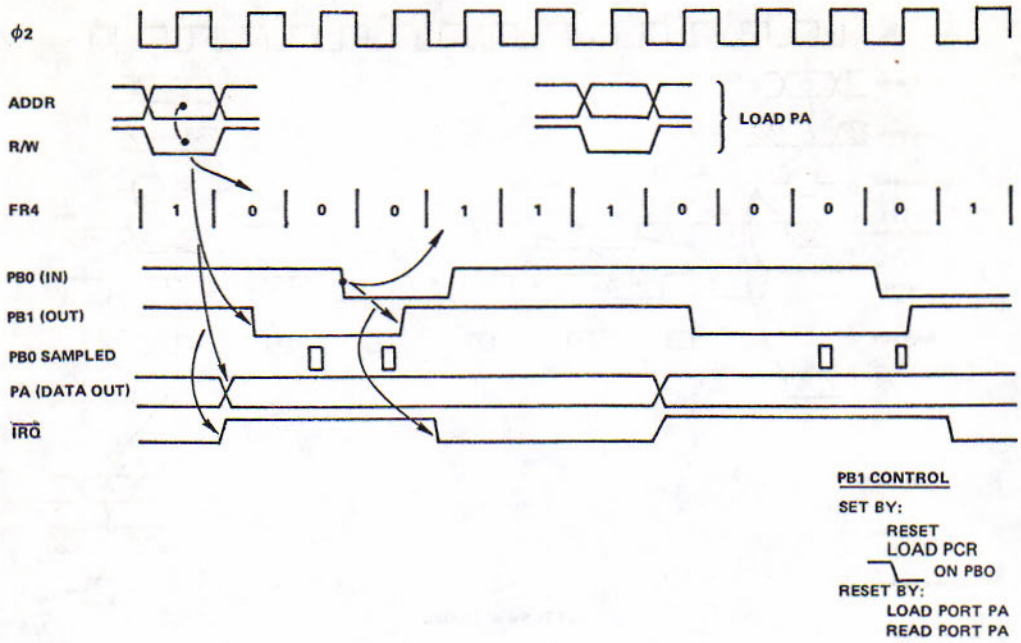

**52-Pin Packaging Diagram**



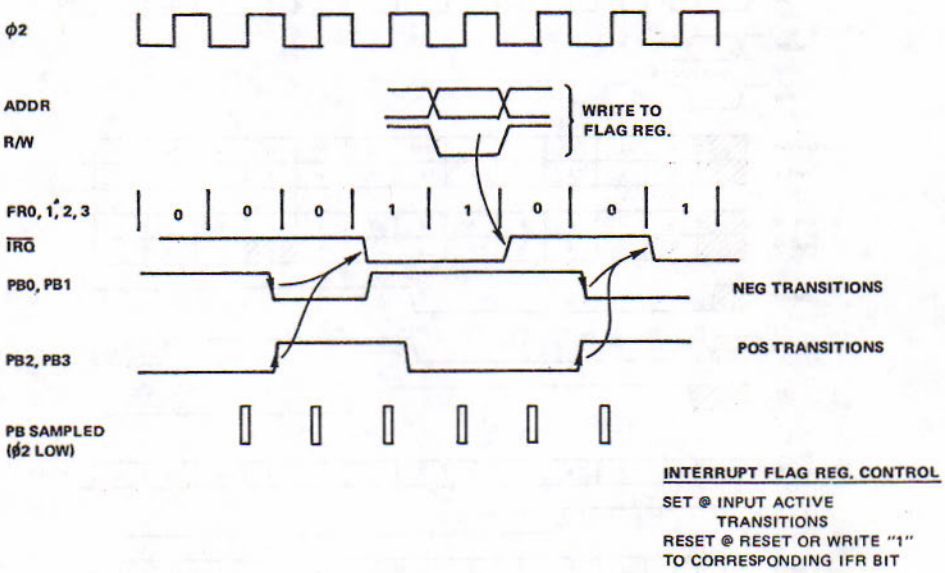

R6531 Serial Timing




R6531 Counter/Timer Timing




R6531 Timing for Handshake Mode




R6531 Timing for Interrupt Mode

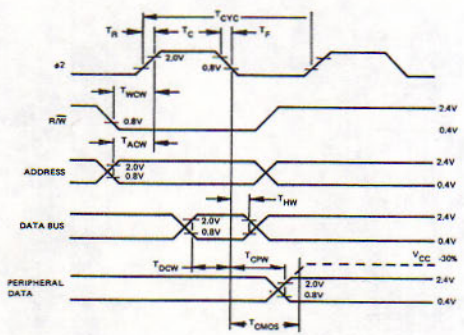
## Write Timing Characteristics

| Characteristic | Symbol | 1 MHz | | 2 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Clock Period | $T_{CYC}$ | 1 | 10 | 0.5 | 10 | μs |
| Rise & Fall Times | $T_R$, $T_F$ | | 25 | | 15 | ns |
| Clock Pulse Width | $T_C$ | 470 | | 235 | | ns |
| R/$\overline{W}$ valid before positive transition of clock | $T_{WCW}$ | 180 | | 120 | | ns |
| Address valid before positive transition of clock | $T_{ACW}$ | 180 | | 120 | | ns |
| Data Bus valid before negative transition of clock | $T_{DCW}$ | 270 | | 135 | | ns |
| Data Bus Hold Time | $T_{HW}$ | 10 | | 10 | | ns |
| Peripheral data valid after negative transition of clock | $T_{CPW}$ | | 900 | | 450 | ns |

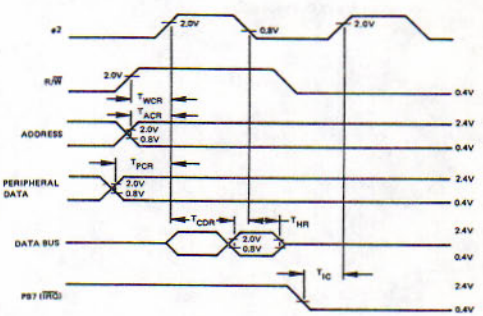
## Read Timing Characteristics

| Characteristic | Symbol | 1 MHz | | 2 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| R/$\overline{W}$ valid before positive transition of clock | $T_{WCR}$ | 180 | | 120 | | ns |
| Address valid before positive transition of clock | $T_{ACR}$ | 180 | | 120 | | ns |
| Peripheral data valid before positive transition of clock | $T_{PCR}$ | 270 | | 135 | | ns |
| Data Bus valid after positive transition of clock | $T_{CDR}$ | | 350 | | 180 | ns |
| Data Bus Hold Time | $T_{HR}$ | 10 | | 10 | | ns |
| IRQ valid after negative transition of clock | $T_{IC}$ | | 900 | | 450 | ns |

Loading = 100 pF + 1 TTL load for PA0-PA7, PB0-PB6, PCO-PC7
= 100 pF + 1 TTL load for D0-D7 (R6531A)
= 130 pF + 1 TTL load for D0-D7 (R6531)




Write Timing Characteristics




Read Timing Characteristics

## SPECIFICATIONS

### Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | -0.3 to +7.0 | Vdc |
| Operating Temperature Range | $T$ | | °C |
| Commercial | | 0 to +70 | |
| Industrial | | -40 to +85 | |
| Storage Temperature Range | $T_{stg}$ | -55 to +150 | °C |

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

### Electrical Characteristics

(VCC = 5V ± 10% for R6531, VCC = 5V ± 5% for R6531A)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 2.0 | VCC | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | +0.8 | V |
| Input Leakage Current; $V_{IN} = V_{SS} + 5V$, $V_{CC} = +5V$ A0-A11, CS, R/$\overline{W}$, $\overline{RES}$, $\phi 2$, PD0-PD3 | $I_{IN}$ | | 2.5 | μA |
| Leakage Current for High Impedance State, $V_{CC} = +5V$ (Three State); $V_{IN} = 0.4V$ to 2.4V; D0-D7, PA0-PA7, PB0-PB6 | $I_{TSI}$ | | ±10.0 | μA |
| Output High Voltage VCC = MIN, $I_{LOAD} \leq -200$ μA (PA0-PA7, PB-PB6, D0-D7) | $V_{OH}$ | VSS + 2.4 | | V |
| Output Low Voltage VCC = MIN, $I_{LOAD} \leq 2.1$ mA | $V_{OL}$ | | VSS + 0.4 | V |
| Output High Current (Sourcing); VOH ≥ 2.4V (PA0-PA7, PB0-PB6, PC0-PC7, PD0-PD3, D0-D7) | $I_{OH}$ | -200 | | μA |
| Output Low Current (Sinking); $V_{OL} \leq 0.4V$ (PA0-PA7) (PB0-PB6) (PC0-PC7) | $I_{OL}$ | 2.1 | | mA |
| Clock Input Capacitance, $V_{CC} = 5V$ | $C_{Clk}$ | | 20 | pF |
| Input Capacitance, $V_{CC} = 5V$ | $C_{IN}$ | | 10 | pF |
| Output Capacitance, $V_{CC} = 5V$, chip deselected | $C_{OUT}$ | | 10 | pF |
| Power Dissipation | $P_D$ | | 1.0 | W |

*When programmed as address pins

All values are D.C. readings

DOCUMENT NO. 29000 D42
REV. 2, FEBRUARY 1978

PART NUMBER
**R6532**

Rockwell

# R6500 Microcomputer System DATA SHEET





# RAM, I/O, INTERVAL TIMER DEVICE (RIOT)

## SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-Channel, Silicon-Gate technology. Its performance speeds are enhanced by advanced system architecture which enables multiple addressing. Its innovative architecture results in smaller chips — the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of 10 software-compatible microprocessor (CPU) devices. Rockwell also provides memory and I/O devices that further enhance the cost-effectivity of the R6500 microcomputer system . . . as well as low-cost design aids and documentation.

## DESCRIPTION

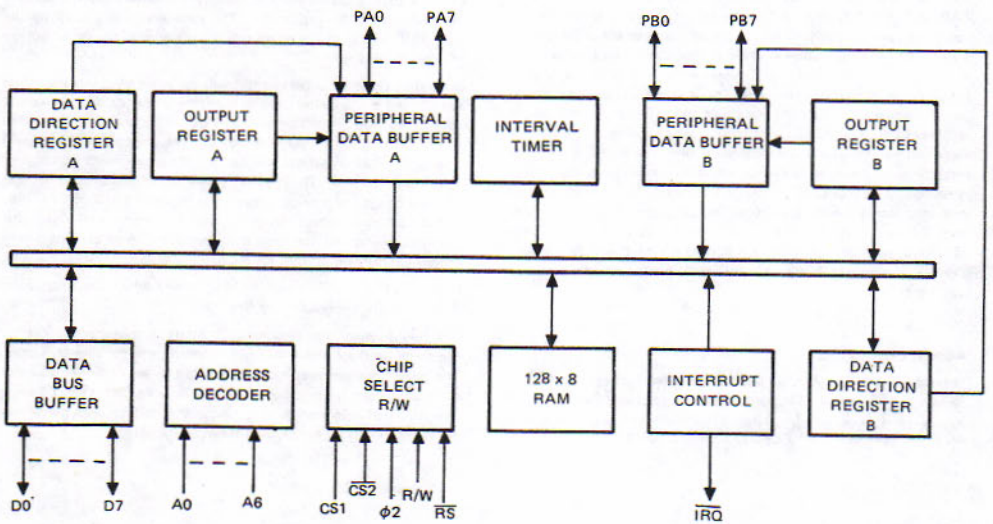
The R6532 is designed to operate in conjunction with the R6500 Microprocessor Family. It is comprised of a 128 x 8 static RAM, two software controlled 8 bit bidirectional data ports allowing direct interfacing between the microcomputer and peripheral devices, a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods, and a programmable edge detect circuit.

## FEATURES

- 8 bit bidirectional Data Bus for direct communication with the microprocessor
- 128 x 8 static RAM
- Two 8 bit bidirectional data ports for interface to peripherals
- Two programmable Data Direction Registers
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Bus
- Programmable edge-sensitive interrupt

### Ordering Information

| Order Number | Package Type | Temperature Range |
|---|---|---|
| R6532P | Plastic | 0°C to +70°C |
| R6532C | Ceramic | 0°C to +70°C |




R6532 Block Diagram



Specifications subject to change without notice

## INTERFACE SIGNAL DESCRIPTION

**Reset ($\overline{RES}$)**

During system initialization a logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least two clock periods when reset is required.

**Read/Write (R/W)**

The R/W signal is supplied by the microprocessor and is used to control the transfer of data to and from the microprocessor and the R6532. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the R6532. A low on the R/W pin allows a write (with proper addressing) to the R6532.

**Interrupt Request ($\overline{IRQ}$)**

The $\overline{IRQ}$ pin is an interrupt pin from the interrupt control logic. The pin will be normally high with a low indicating an interrupt from the R6532. An external 3K pull-up resistor is required. The $\overline{IRQ}$ pin may be activated by a transition on PA7 or timeout of the interval timer.

**Data Bus (D0-D7)**

The R6532 has eight bidirectional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor array. The output buffers remain in the off state except when the R6532 is selected for a Read operation.

**Peripheral Data Ports (PA0-PA7, PB0-PB7)**

The R6532 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into 2 8-bit ports, PA0-PA7 and PB0-PB7. PA7 also has other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and the internal pull-up device acts as less than one TTL load to the peripheral data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the R6532 it receives data stored in the output register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volt for a "0" as the peripheral pins are all TTL compatible. Pins PB0-PB7 are also capable of sourcing 3 ma at 1.5V, thus making them capable of Darlington drive.

**Address Lines (A0-A6)**

There are 7 address pins. In addition to these 7, there is the $\overline{RAM\ SELECT}$ ($\overline{RS}$) pin. The pins A0-A6 and $\overline{RAM\ SELECT}$ are always used as addressing pins. There are two additional pins which are used as CHIP SELECTS. They are pins CS1 and $\overline{CS2}$.

## INTERNAL ORGANIZATION

The R6532 is divided into four basic sections, RAM, I/O, TIMER, and Interrupt Control. The RAM interfaces directly with the microprocessor through the system data bus and address lines. The I/O section consists of two 8-bit halves. Each half contains a Data Direction Register (DDR) and an Output Register.

**RAM – 128 Bytes (1024 Bits)**

The 128 x 8 Read/Write memory acts as a conventional static RAM. Data can be written into the RAM from the microprocessor by selecting the chip (CS1=1, $\overline{CS2}$ = 0) and by setting $\overline{RS}$ to a logic 0 (0.4V). Address lines A0 through A6 are then used to select the desired byte of storage.

**Internal Peripheral Registers**

The Peripheral A I/O port consists of eight lines which can be individually programmed to act as either an input or an output. A logic zero in a bit of the Data Direction Register (DDRA) causes the corresponding line of the PA port to act as an input. A logic one causes the corresponding PA line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Output Register (ORA).

Data is read directly from the PA pins during any read operation. For any output pin, the data transferred into the processor will be the same as that contained in the Output Register if the voltage on the pin is allowed to go to 2.4V for a logic one. Note that for input lines, the processor can write into the corresponding bit of the Output Register. This will not affect the polarity on the pin until the corresponding bit of DDRA is set to a logic one to allow the peripheral pin to act as an output.

In addition to acting as a peripheral I/O line, the PA7 line can be used as an edge-detecting input. In this mode, an active transition will set the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag will cause $\overline{IRQ}$ output to go low if the PA7 interrupt has been enabled.

Control of the PA7 edge detecting mode is accomplished by writing to one of four addresses. In this operation, A0 controls the polarity of the active transition and A1 acts to enable or disable interrupting of the processor. The data which is placed on the Data Bus during this operation is discarded and has no effect on the control of PA7.

Setting of the PA7 interrupt flag will occur on an active transition even if the pin is being used as a normal input or as a peripheral control output. The flag will also be set by an active transition if interrupting from PA7 is disabled. The reset signal ($\overline{RES}$) will disable the PA7 interrupt and will set the active transition to negative (high to low). During the system initialization routine, it is possible to set the interrupt flag by a negative transition. It may also be set by changing the polarity of the active interrupt. It is therefore recommended that the interrupt flag be cleared before enabling interrupting from PA7.

Clearing of the PA7 Interrupt Flag occurs when the micorprocessor reads the Interrupt Flag Register.

The operation of the Peripheral B Input/Output port is exactly the same as the normal I/O operation of the Peripheral A port. The eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin is controlled by the Output Register (ORB).

The primary difference between the PA and the PB ports is in the operation of the output buffers which drive these pins. The PB output buffers are push-pull devices which are capable of sourcing 3 ma at 1.5V. This allows these pins to directly drive transistor switches. To assure that the microprocessor will read proper data on a "Read PB" operation, sufficient logic is provided in the chip to allow the microprocessor to read the Output Register instead of reading the peripheral pin as on the PA port.

**Interval Timer**

The Timer section of the R6532 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic.

The interval timer can be programmed to count up to 255 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1". After the interrupt flag is set the internal clock begins counting down to a maximum of -255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8-bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., A3 = 1 enables $\overline{IRQ}$, A3 = 0 disables $\overline{IRQ}$. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

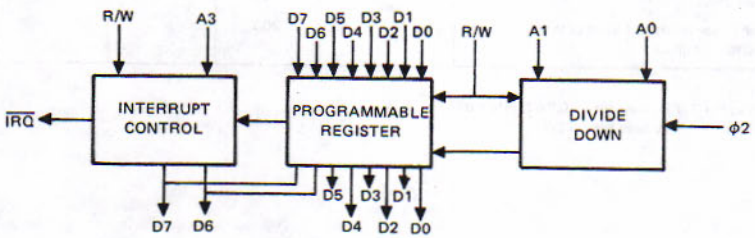
When the timer has counted thru 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 27T. The value read is in two's complement, but remember that interrupt occurred on count number one. Therefore, we must subtract 1.

| | | |
|---|---|---|
| Value read | = | 1 1 1 0 0 1 0 0 |
| Complement | = | 0 0 0 1 1 0 1 1 |
| ADD 1 | = | 0 0 0 1 1 1 0 0 = 28 Equals two's complement of register |
| SUB 1 | = | 0 0 0 1 1 0 1 1 = 27 |

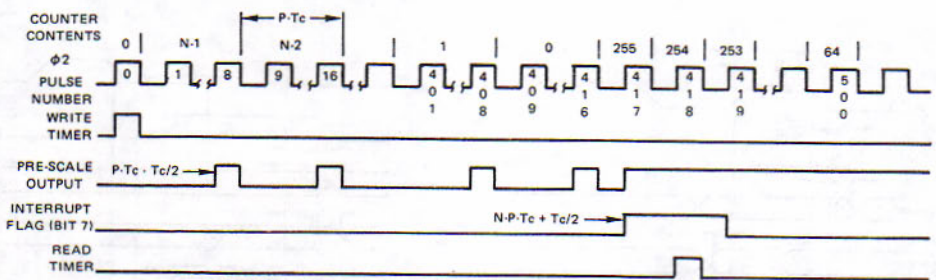
Thus, to arrive at the total elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divide by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 27T = 443T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flags are read (D7 for the timer, D6 for the edge detect) data bus lines D0-D5 go to 0.

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.




**Basic Elements of Interval Timer**




ASSUME 52 LOADED INTO TIMER WITH A DIVIDE BY 8.
THE COUNTER CONTENTS AND THE CLOCK PULSE NUMBERS WILL COINCIDE.
Prescale, P = 8
Cycle Time, Tc = 1 μsec (for 1 MHz)
Count, N = 52

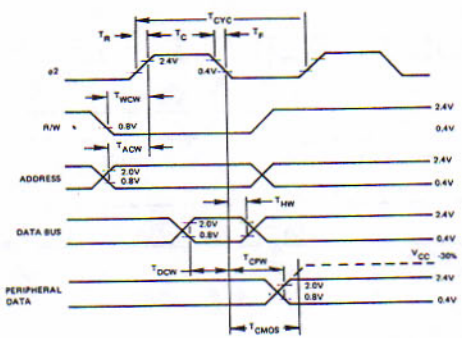
## Write Timing Characteristics

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Clock Period | $T_{CYC}$ | 1 | | 10 | μS |
| Rise & Fall Times | $T_R$, $T_F$ | | | 25 | ns |
| Clock Pulse Width | $T_C$ | 470 | | | ns |
| R/W valid before positive transition of clock | $T_{WCW}$ | 180 | | | ns |
| Address valid before positive transition of clock | $T_{ACW}$ | 180 | | | ns |
| Data Bus valid before negative transition of clock | $T_{DCW}$ | 300 | | | ns |
| Data Bus Hold Time | $T_{HW}$ | 10 | | | ns |
| Peripheral data valid after negative transition of clock | $T_{CPW}$ | | | 1 | μS |
| Peripheral data valid after negative transition of clock driving CMOS (Level = VCC - 30%) | $T_{CMOS}$ | | | 2 | μS |

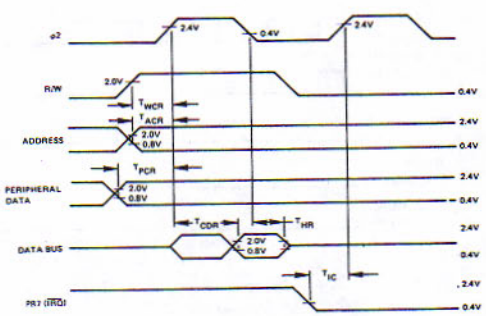
## Read Timing Characteristics

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R/W valid before positive transition of clock | $T_{WCR}$ | 180 | | | ns |
| Address valid before positive transition of clock | $T_{ACR}$ | 180 | | | ns |
| Peripheral data valid before positive transition of clock | $T_{PCR}$ | 300 | | | ns |
| Data Bus valid after positive transition of clock | $T_{CDR}$ | | | 395 | ns |
| Data Bus Hold Time | $T_{HR}$ | 10 | | | ns |
| IRQ (Interval Timer Interrupt) valid before positive transition of clock | $T_{IC}$ | 200 | | | ns |

Loading = 30 pF + 1 TTL load for PA0-PA7, PB0-PB7
= 130 pF + 1 TTL load for D0-D7




Write Timing Characteristics




Read Timing Characteristics

**RAM Addressing**

$\overline{RS}$ = 0
A0-A6 select RAM address

**I/O Addressing**

$\overline{RS}$ = 1 A2 = 0
R/W = 1 to read, 0 to write

| | A1 | A0 |
|---|---|---|
| PA data | 0 | 0 |
| PA data direction | 0 | 1 |
| PB data | 1 | 0 |
| PB data direction | 1 | 1 |

**Write Edge Detect Control**

$\overline{RS}$, A2 = 1 R/W, A4 = 0

A1 = 1, enable interrupt from PA7
A1 = 0, disable interrupt from PA7
A0 = 1, positive edge detect (PA7)
A0 = 0, negative edge detect (PA7)

**Read and Clear Interrupt Flag**

$\overline{RS}$, R/W, A2, A0 = 1
Bit 7 = Timer Flag
Bit 6 = PA7 Flag

**Read Interval Timer**

$\overline{RS}$, A4, A2, R/W, A0 = 1

**Read Interval Timer Overflow**

$\overline{RS}$, A4, A2, R/W = 1, A0 = 0

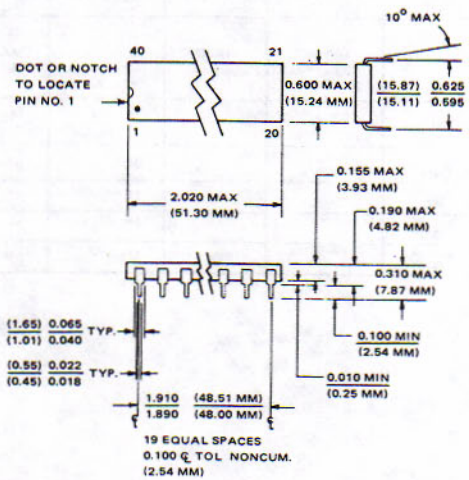
**Write Count to Interval Timer**

$\overline{RS}$, A4, A2 = 1, R/W = 0

| | A1 | A0 |
|---|---|---|
| ÷1 | 0 | 0 |
| ÷8 | 0 | 1 |
| ÷64 | 1 | 0 |
| ÷1024 | 1 | 1 |

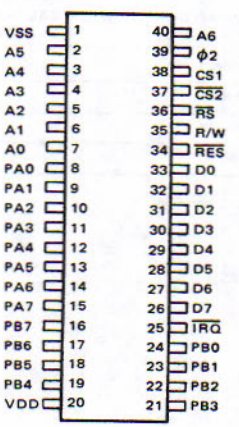
A3 = 1, enable timer interrupt
A3 = 0, disable timer interrupt

NOTE: For all operations CS1 = 1, $\overline{CS2}$ = 0.




NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

**Packaging Diagram**




**Pin Configuration**

## SPECIFICATIONS

### Maximum Ratings

| Rating | Symbol | Voltage | Unit |
|---|---|---|---|
| Supply Voltage | VCC | -0.3 to +7.0 | V |
| Input/Output Voltage | $V_{IN}$ | -0.3 to +7.0 | V |
| Operating Temperature Range | $T_{OP}$ | 0 to 70 | °C |
| Storage Temperature Range | $T_{STG}$ | -55 to +150 | °C |

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

### Electrical Characteristics

(VCC=5.0%, VSS=0V, $T_A$=25°C)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | $V_{SS}$ + 2.4 | | VCC | V |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$ - 0.3 | | $V_{SS}$ + 0.4 | V |
| Input Leakage Current; $V_{IN}$ = $V_{SS}$ + 5V<br>A0-A6, RS, R/W, $\overline{RES}$, $\phi$2, CS1, $\overline{CS2}$ | $I_{IN}$ | | 1.0 | 2.5 | μA |
| Input Leakage Current for High Impedance State<br>(Three State); $V_{IN}$ = 0.4V to 2.4V; D0-D7 | $I_{TSI}$ | | ±1.0 | ±10.0 | μA |
| Input High Current; $V_{IN}$ = 2.4V<br>PA0-PA7, PB0-PB7 | $I_{IH}$ | -100. | -300. | | μA |
| Input Low Current; $V_{IN}$ = 0.4V<br>PA0-PA7, PB0-PB7 | $I_{IL}$ | | -1.0 | -1.6 | MA |
| Output High Voltage<br>VCC = MIN, $I_{LOAD}$ ≤ -100 μA (PA0-PA7, PB0-PB7, D0-D7)<br>$I_{LOAD}$ ≤ -3 MA (PB0-PB7) | $V_{OH}$ | <br>VSS + 2.4<br>VSS + 1.5 | | | V |
| Output Low Voltage<br>VCC = MIN, $I_{LOAD}$ ≤ 1.6 MA (D0-D7) | $V_{OL}$ | | | VSS + 0.4 | V |
| Output High Current (Sourcing);<br>VOH ≥ 2.4V (PA0-PA7, PB0-PB7, D0-D7)<br>≥ 1.5V Available for other than TTL (Darlingtons) (PB0-PB7) | $I_{OH}$ | <br>-100<br>-3.0 | <br>-1000<br>-5.0 | | <br>μA<br>MA |
| Output Low Current (Sinking); VOL ≤ 0.4V (PA0-PA7)<br>(PB0-PB7) | $I_{OL}$ | 1.6 | | | MA |
| Clock Input Capacitance | $C_{Clk}$ | | | 30 | pF |
| Input Capacitance | $C_{IN}$ | | | 10 | pF |
| Output Capacitance | $C_{OUT}$ | | | 10 | pF |
| Power Dissipation | $P_D$ | | 500 | 1000 | mW |

All values are D.C. readings

DOCUMENT NO. 29000 D56
SEPTEMBER 1978

PART NUMBER
R6534

Rockwell

# R6500 Microcomputer System
# DATA SHEET





## ROM-I/O-COUNTER (RIOC)

### SYSTEM ABSTRACT

The ROM-I/O-Counter (RIOC), Part Number R6534, further enhances the cost-effectivity of the R6500 NMOS 8-bit microcomputer system by providing a powerful, flexible two-chip minimum system option. Produced with N-channel depletion load, silicon gate technology, the R6500 system employs advanced architecture, including 13 instruction addressing modes to achieve third generation performance speeds and smaller chips, the threshold to lower hardware and design costs. Included in the R6500 system are 10 software-compatible microprocessor (CPU) options, a growing number of memory and I/O devices, a very efficient, low-cost SYSTEM 65 development aid and complete documentation.

### DESCRIPTION

The R6534 is primarily designed to provide innovative Equipment Designers with a wide span of two-chip minimum systems in combination with the R6500 family of 10 CPUs. It can also be combined in a variety of multi-chip system configurations with other R6534's, ROMs, RAMs and other I/O devices.

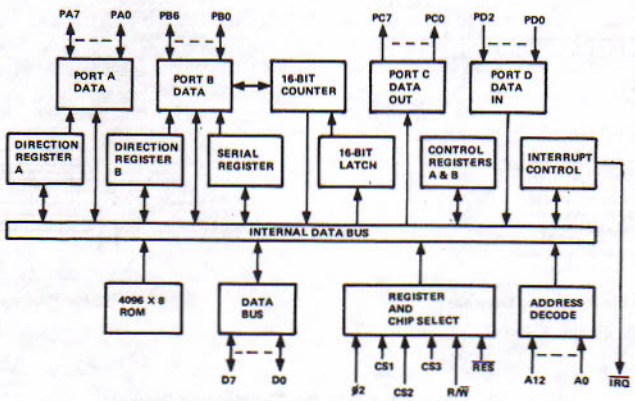
There are two R6534 versions: a 40-pin dual-in-line package; another with expanded I/O in a compact 52-pin quad-in-line package — see Table 1. Both versions contain a 4096 x 8 mask-programmable ROM, a software programmable multi-mode counter, an 8-bit serial data channel, and 14 bidirectional data lines (two ports) with a handshake control mode and four interrupts inputs. The 52-pin version has an additional 8-bit output port and a 3-bit input port and one additional I/O line for a total of 26 I/O lines.

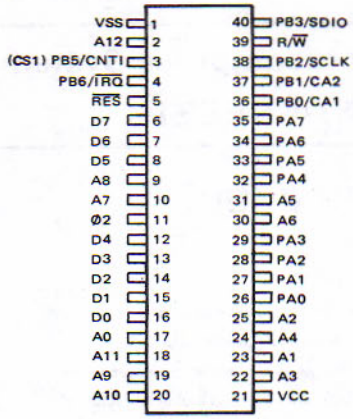
### FEATURES

- 4096 x 8 mask programmable ROM
- 16-bit multi-mode counter/latch
  - interval timer (one shot or free running)
  - pulse generator (one shot or free running)
  - event counter
- 8-bit serial channel
- TTL compatible I/O, drive one TTL load
- 26 I/O lines (52-pin package)
- I/O handshake control
- Four edge sensitive interrupt inputs
- 1 MHz operation
- Single +5V power supply

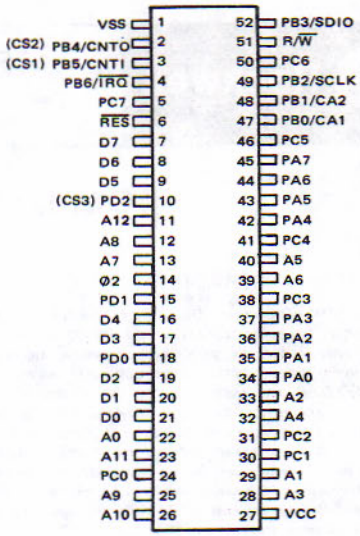
**Table 1 Ordering Information**

| Order Number | Package Type | Frequency Option | Temperature Range |
|---|---|---|---|
| R6534P | 40-Pin DIP Plastic | 1 MHz | $0^{o}C$ to $+70^{o}C$ |
| R6534C | 40-Pin DIP Ceramic | 1 MHz | $0^{o}C$ to $+70^{o}C$ |
| R6534Q | 52-Pin QIP Plastic | 1 MHz | $0^{o}C$ to $+70^{o}C$ |

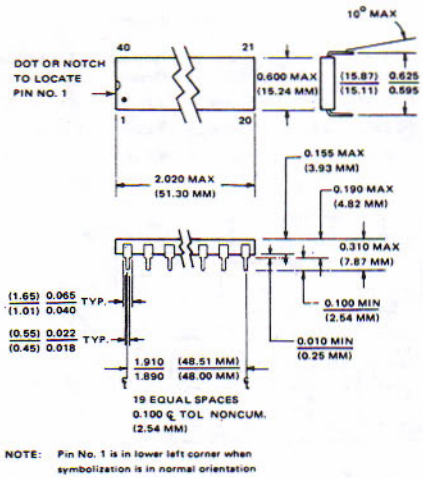





40- Pin Configuration

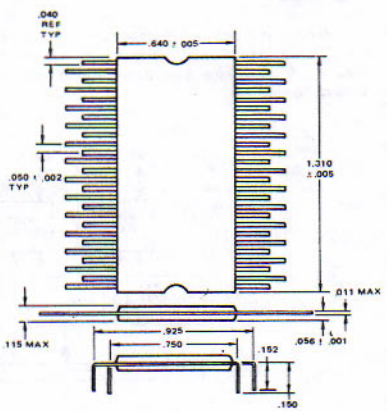



52-Pin Configuration




NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

40-Pin Packaging Diagram




52-Pin Packaging Diagram

Figure 1. R6534 Pin Configuration Options

## INTERFACE SIGNALS

### RESET ($\overline{RES}$)

This active, low signal is used to initialize the R6534. It initializes all internal registers except the counter and serial registers. This action places all bidirectional I/O lines in the input state and the Port C outputs in the high state. The timer, shift register, and interrupts are disabled. The $\overline{RES}$ signal must be low for at least four clock periods when reset is required.

### ADDRESS BUS (A0-A12) AND CHIP SELECTS (CS1-CS3)

Memory and register selection is accomplished using the 12 address lines and in multiple device systems also using one or more of the three Chip Select mask options. When PB4, PB5, or PD2 are chosen as chip selects, they cannot be used as peripheral I/O pins.

### DATA BUS (D0-D7)

The R6534 has eight data bus lines. These lines connect to the microcomputers data bus and allow transfer of data to or from the microprocessor. The output buffers remain in the off-state except when the R6534 is selected for a read operation.

### READ/WRITE (R/W)

The R/W signal is supplied by the microprocessor and is used to control the transfer of data to and from the microprocessor and the R6534. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the R6534. A low on the R/W pin allows a write (with proper addressing) to the R6534.

### PERIPHERAL DATA PORTS (PA0-PA7, PB0-PB6, PC0-PC7, PD0-PD2)

The 40-pin version of the R6534 has 14 pins available for peripheral I/O operations. Each pin is software programmable to act as an input or an output. The pins are grouped into an 8-bit port, PA0-PA7, and a 6-bit port, PB0-PB3, PB5 and PB6. The lines of the PB port may serve other functions. Port PA and PB have associated data direction registers.

The expanded I/O of the 52-pin version provides one additional PB bit (PB5), an 8-bit output only port (PC0-PC7) and a 3-bit input only port (PD0-PD2). PB5, PB6 and PD2 may be assigned other functions, as described herein.

The outputs are push/pull type drivers capable of driving a single TTL load. When inputs are selected the lines float. If PB6 is programmed as the $\overline{IRQ}$ request output, the line is driven low and requires an external pull-up, thus allowing the wire OR-ing of $\overline{IRQ}$ from other devices.

## INTERNAL ORGANIZATION

The R6534 is divided into two basic functions: ROM and I/O — see table below. The selection is accomplished by issuing the appropriate address information on the address bus when the chip is selected.

### ADDRESSING

Addressing of the R6534 offers many variations to the user for system configuration flexibility. Combination with other R6534's, ROMs, RAMs or I/O devices is possible without need for external address decoding. Each of the basic functions on the device has its own decode mask for unique selection.

The specific address ranges and chip selects are defined by the user and are dependent on the number of chips in the system. The programmed options to be fixed by masking are:

**R6534 Address Table**

| | Chip Selects | | | Address Inputs (A0-A12) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | CS3 | CS2 | CS1 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ROM | X | X | X | X | 4K ROM Decode | | | | | | | | | | | |
| I/O | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | I/O Decode | | | |

The X and Z bits may be selected as high, low or no effect.

The chip select pins are also discrete I/O pins PB5, PB4, and PD2. The pins are independent of each other in that any one may be used as a chip select. The user specifies as mask options which pins are to be used as I/O and which as chip selects.

### ROM — 4K BYTES (32K BITS)

The 32K ROM is a 4096 x 8 bit configuration. An address on lines A0-A11 uniquely selects one byte of ROM. Additionally, address line A12 and the chip selects are required to select the ROM function on a given chip. In a system with multiple R6534's, the CS1, CS2, and CS3 mask options allow up to seven devices with 28K bytes of ROM without the need for external decoding.

## INPUT/OUTPUT

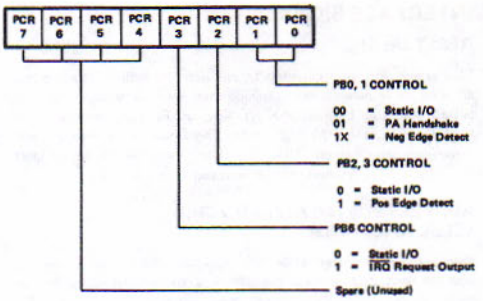
The input/output section is comprised of the data ports, direction registers, counter and associated latches, control registers, and interrupt registers. These I/O functions are all accessible by the R6502 CPU's instruction set using address bits A0-A3 for the specific function of the device. Address bits A4-A12 and CS1, CS2, and CS3 additionally may be decoded to select a given R6534 device in a multichip system. The addresses of the 15 internal peripheral registers are:

| A3 | A2 | A1 | A0 | Register |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Port A |
| 0 | 0 | 0 | 1 | Port B |
| 0 | 0 | 1 | 0 | Port C (write only) |
| 0 | 0 | 1 | 1 | Port D (read only) |
| 0 | 1 | 0 | 0 | Read Lower Counter/Write Lower Latch |
| 0 | 1 | 0 | 1 | Read Upper Counter/Write Upper Latch and Download |
| 0 | 1 | 1 | 0 | Write Lower Latch |
| 0 | 1 | 1 | 1 | Write Upper Latch |
| 1 | 0 | 0 | 0 | Serial Data Register |
| 1 | 0 | 0 | 1 | Interrupt Flag Register |
| 1 | 0 | 1 | 0 | Interrupt Enable Register |
| 1 | 0 | 1 | 1 | Auxiliary Control Register |
| 1 | 1 | 0 | 0 | Peripheral Control Register |
| 1 | 1 | 0 | 1 | *Data Direction Register – Port A |
| 1 | 1 | 1 | 0 | *Data Direction Register – Port B |

* Write Only

## CONTROL REGISTERS

Two control registers, peripheral control and auxiliary control, are provided for software selection of various I/O functions. The Peripheral Control Register is primarily associated with Port B functions and the Auxiliary Control Register is associated with the counter and serial data functions which also affect Port B. The register bit assignments are:




**Peripheral Control Register (PCR)**

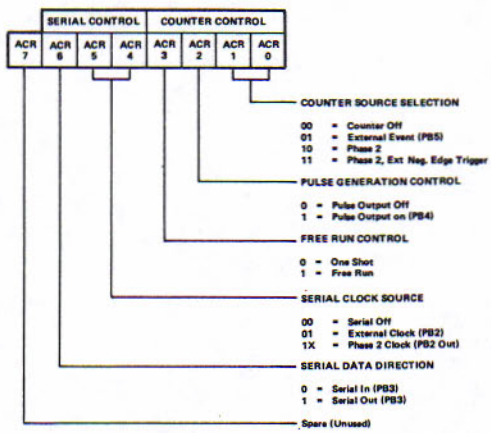
## INTERRUPT ENABLE AND FLAG REGISTERS

Two registers are provided for interrupt control. Corresponding bits in the enable and flag registers are logically ANDed to set the Interrupt Request Pending flag. If the pending flag is set and PB6 is selected as an $\overline{IRQ}$ Request Output, then PB6 will be set low to request the R6502 CPU to service $\overline{IRQ}$.

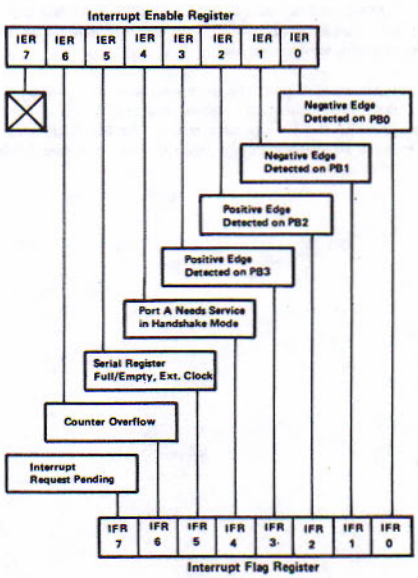
The interrupt enable bits are set or reset by writing into the Interrupt Enable Register. The interrupt flag bits IFR0-IFR6 can be cleared directly by writing a byte to the flag register which has 1's in those bit positions to be cleared.

IFR4 and IFR5 may also be cleared by reading or writing the Port A or Serial Data Registers respectively. IFR6 may also be cleared by reading the lower counter with I/O address hex 4 or writing the upper latch with I/O addresses hex 5 or 7.

These registers and their bit assignments are:




**Auxiliary Control Register (ACR)**



## PERIPHERAL DATA PORTS

Each line of the 8-bit data Port A may be individually selected as an input or output. Associated with the port is Data Direction Register – Port A (DDRA). Each line of the 7-bit data Port B may be individually selected as an input or an output. This port also has a Data Direction Register (DDRB). The two data direction registers (A and B) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral pin as an output. Therefore, anything written into the data register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data from the data register. For example, a "1" loaded into DDRA, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and would be in a float state.

Note that when lines in the PB port are used alternately as control lines for other on-chip functions, Direction Register B must also be loaded to set up the proper direction – the Control Registers have no effect on data direction.

The 8-bit data Port C is an output only port. The 3-bit data Port D is an input only port.

For those lines being used as outputs, the data registers are used to latch data from the Data Bus during a Write operation.

For the lines being used as inputs, the microprocessor is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the Output data.

## EDGE DETECT LOGIC

Operating in parallel with the I/O operation of PB0-PB3 is edge detect logic that is enabled by Peripheral Control Register bits 1 and 2. PCR1 enables logic that upon detection of a negative edge on PB0 or PB1 will set a corresponding flag in the Interrupt Flag Register. PCR2 enables logic that upon detection of a positive edge on PB2 or PB3 will set corresponding flags in the Interrupt Flag Register. If corresponding bits are set in the Interrupt Enable Register, then the Interrupt Request Pending flag will be set.

## MULTI-MODE COUNTER/LATCH

The R6534 contains a 16-bit counter with an associated 16-bit latch whose modes are software selectable by setting appropriate bits in the Auxiliary Control Register. The latch holds the counter preset value and all 16 bits download to the counter simultaneously upon command (I/O address hex 5) of the software or automatically in free run modes upon overflow of the counter. The counter is a decrementing counter and causes the setting of a flag in the Interrupt Flag Register when it overflows. This interrupt flag, bit 6, is logically ANDed with a corresponding counter overflow interrupt enabled bit to set the Interrupt Request Pending flag. The Auxiliary Control Register is used to set four basic modes which specify the source of the count information, and to select two mode modifiers that apply equally to the three active modes.

Mode 0 – Counter Off

Mode 1* – Event Counter. – counts external event inputs (negative transitions) at PB5

Mode 2 – Interval Timer – counts O2 system clock pulses.

Mode 3* – External Trigger – counts Ø2 system clock pulses starting with a negative transition.

Mode Modifier A* – Pulse Generation Control – causes the output level on PB4 to switch low each time counter is loaded using I/O address hex. 5. At the counter overflow, PB4 switches high. If in the free run mode, PB4 continues to toggle at each subsequent counter overflow; otherwise there are no further transitions until the counter is reactivated by the software.

Mode Modifier B – Free Run Control – causes the full 16-bit latch to be downloaded to the counter, continues to count, and sets the counter overflow flag bit every time the counter overflows. Otherwise the counter is a one shot mode in which the counter overflow flag is set one time only until the counter is reactivated by the software.

*52-pin version only.

## SERIAL DATA CHANNEL

The R6534 has an 8-bit serial channel. PB2 and PB3 are software selectable as the serial clock (SCLK) and serial data (SDIO) lines respectively.

The software sets Auxiliary Control Register bits 4 and 5 to enable the serial channel and to specify the source of the shift clock. Selection of the internal clock will shift data at one half the system O2 clock rate. If the external clock is used, data may be shifted at any rate up to one half the system O2 clock rate. In the external clock mode, the counter may be operated in the free run pulse generator mode using the CNTO line externally connected to the SCLK line to provide the desired shift rate.

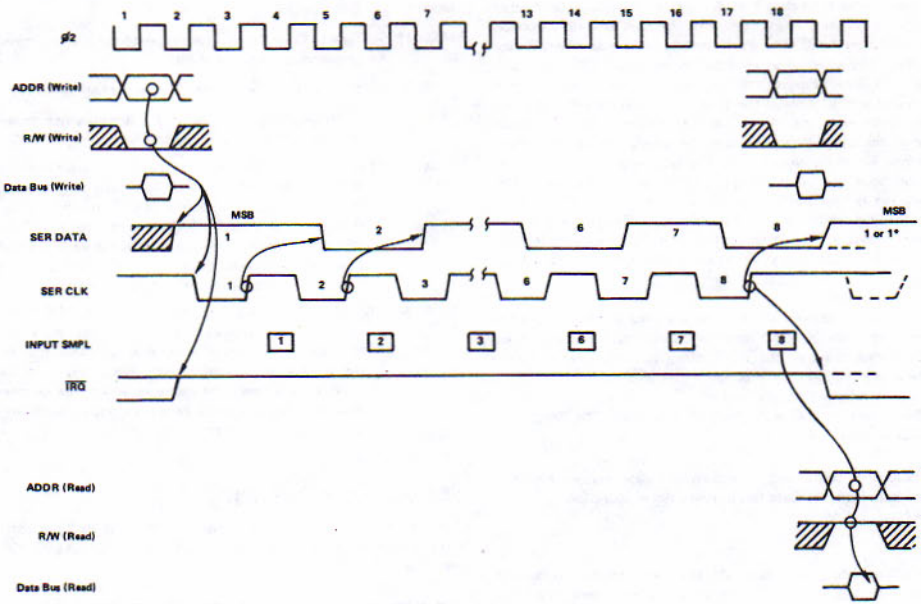
Auxiliary Control Register bit 6 sets the serial data direction. Data are shifted in or out with the most significant bit first under control of the shift clock.

In the external clock mode, the completion of eight shifts of the serial register will set bit 5 of the interrupt flag register. If the corresponding bit of the Interrupt Enable Register is also set an Interrupt Request Pending flag will be set.

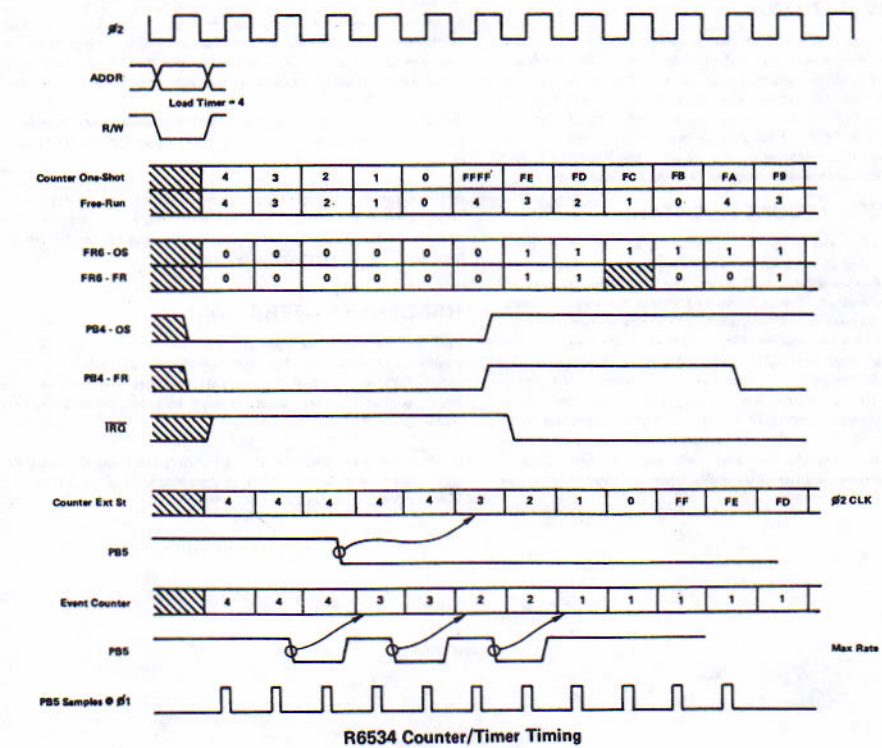
## HANDSHAKE OPERATIONS

PB0 and PB1 may be used as handshake control lines for data transmissions over Port PA; see PCR definition. PB0 is a control input, PB1 is a control output. PB1 switches low on a read or write to Port PA, and switches high in response to a negative transition on PB0.

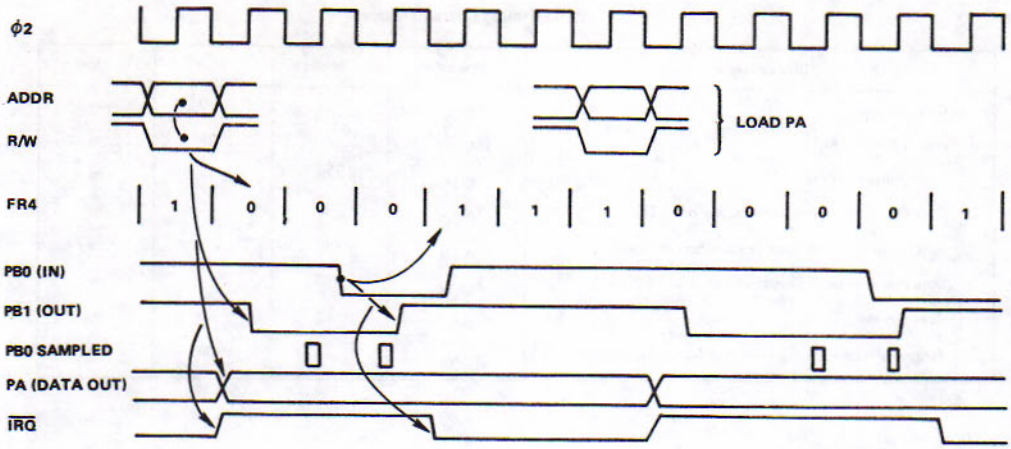
IFR4 in the Flag Register is set by a negative transition on PB0, and cleared by a Read or Write to Port PA; see Handshake Timing Diagram for timing details.




R6534 Serial Timing




R6534 Counter/Timer Timing

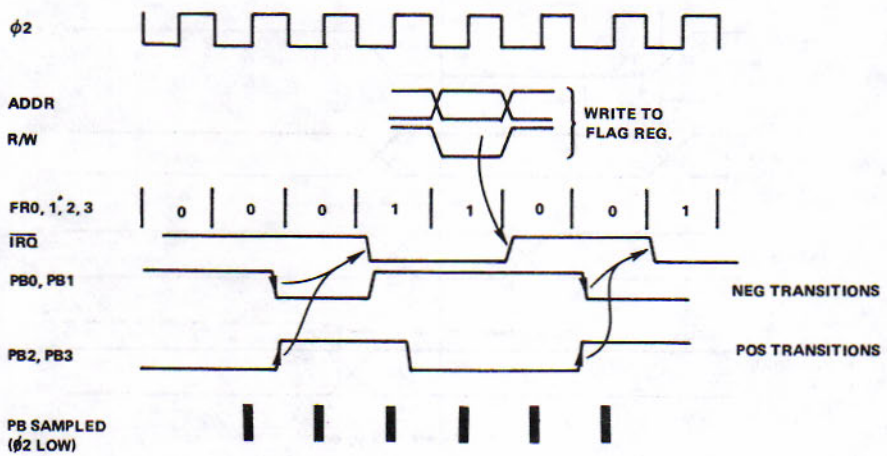



**PB1 CONTROL**

SET BY:
- RESET
- LOAD CRB
- ON PB0

RESET BY:
- LOAD PORT PA
- READ PORT PA

R6534 Timing for Handshake Mode



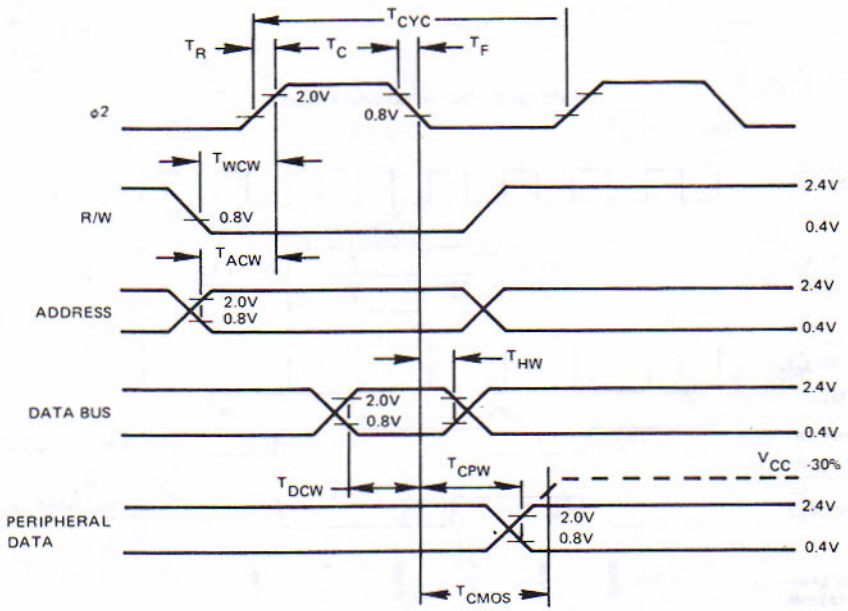

**INTERRUPT FLAG REG. CONTROL**

SET @ INPUT ACTIVE TRANSITIONS
RESET @ RESET OR WRITE "1" TO CORRESPONDING IFR BIT

R6534 Timing for Interrupt Mode

**Write Timing Characteristics**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Clock Period | $T_{CYC}$ | 1 | 10 | μs |
| Rise & Fall Times | $T_R$, $T_F$ | | 25 | ns |
| Clock Pulse Width | $T_C$ | 470 | | ns |
| R/W valid before positive transition of clock | $T_{WCW}$ | 180 | | ns |
| Address valid before positive transition of clock | $T_{ACW}$ | 180 | | ns |
| Data Bus valid before negative transition of clock | $T_{DCW}$ | 270 | | ns |
| Data Bus Hold Time | $T_{HW}$ | 10 | | ns |
| Peripheral data valid after negative transition of clock | $T_{CPW}$ | | 900 | ns |

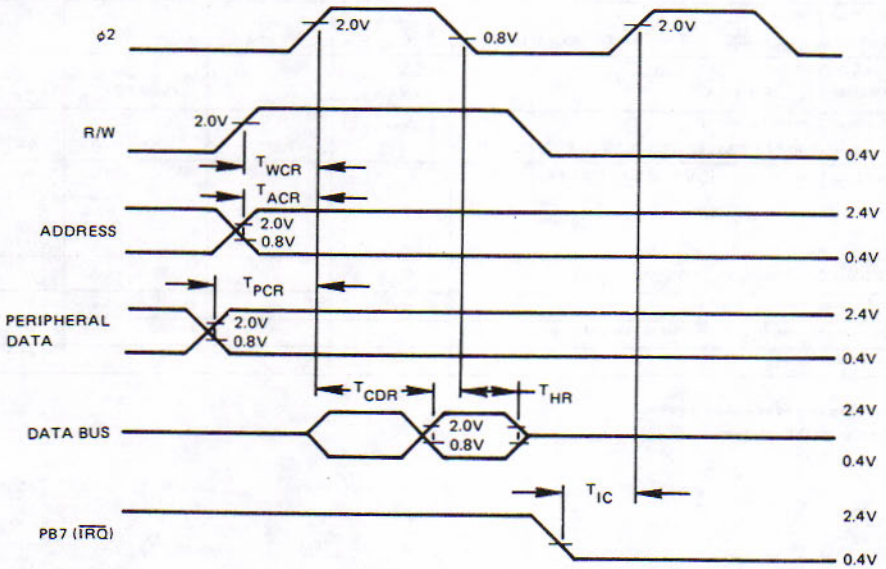



## Write Timing Characteristics

**Read Timing Characteristics**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| R/W valid before positive transition of clock | $T_{WCR}$ | 180 | | ns |
| Address valid before positive transition of clock | $T_{ACR}$ | 180 | | ns |
| Peripheral data valid before positive transition of clock | $T_{PCR}$ | 270 | | ns |
| Data Bus valid after positive transition of clock | $T_{CDR}$ | | 350 | ns |
| Data Bus Hold Time | $T_{HR}$ | 10 | | ns |
| IRQ valid after negative transition of clock | $T_{IC}$ | | 900 | ns |

Loading = 100 pF + 1 TTL load for PA0-PA7, PB0-PB6, PC0-PC7
= 130 pF + 1 TTL load for D0-D7




## Read Timing Characteristics

## SPECIFICATIONS

### Maximum Ratings

| Rating | Symbol | Voltage | Unit |
|---|---|---|---|
| Supply Voltage | VCC | -0.3 to + 7.0 | V |
| Input/Output Voltage | $V_{IN}$ | -0.3 to + 7.0 | V |
| Operating Temperature Range | $T_A$ | 0 to 70 | °C |
| Storage Temperature Range | $T_{STG}$ | -55 to + 150 | °C |

All inputs contain protection circuitry to prevent damage due to high static changes. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

### Electrical Characteristics

(VCC = 5V±10%)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 2.0 | VCC | V |
| Input Low Voltage | $V_{IL}$ | -0.3 | +0.8 | V |
| Input Leakage Current; $V_{IN} = V_{SS} + 5V$, $V_{CC} = +5V$ A0-A12, CS, R/W, RES, ϕ2, PD0-PD2 | $I_{IN}$ | | 2.5 | μA |
| Leakage Current for High Impedance State, $V_{CC} = +5V$ (Three State); $V_{IN} = 0.4V$ to 2.4V; D0-D7, PA0-PA7, PB0-PB6 | $I_{TSI}$ | | ±10.0 | μA |
| Output High Voltage VCC = MIN, $I_{LOAD} \leq -200$ μA (PA0-PA7, PB-PB6, D0-D7) | $V_{OH}$ | VSS + 2.4 | | V |
| Output Low Voltage VCC = MIN, $I_{LOAD} \leq 2.1$ mA | $V_{OL}$ | | VSS + 0.4 | V |
| Output High Current (Sourcing); VOH ≥ 2.4V (PA0-PA7, PB0-PB6, PC0-PC7, PD0-PD2, D0-D7) | $I_{OH}$ | -200 | | μA |
| Output Low Current (Sinking); VOL ≤ 0.4V (PA0-PA7) (PB0-PB6) (PC0-PC7) | $I_{OL}$ | 2.1 | | mA |
| Clock Input Capacitance, $V_{CC} = 5V$ | $C_{Clk}$ | | 20 | pF |
| Input Capacitance, $V_{CC} = 5V$ | $C_{IN}$ | | 10 | pF |
| Output Capacitance, $V_{CC} = 5V$, chip deselected | $C_{OUT}$ | | 10 | pF |
| Power Dissipation | $P_D$ | | 1.0 | W |

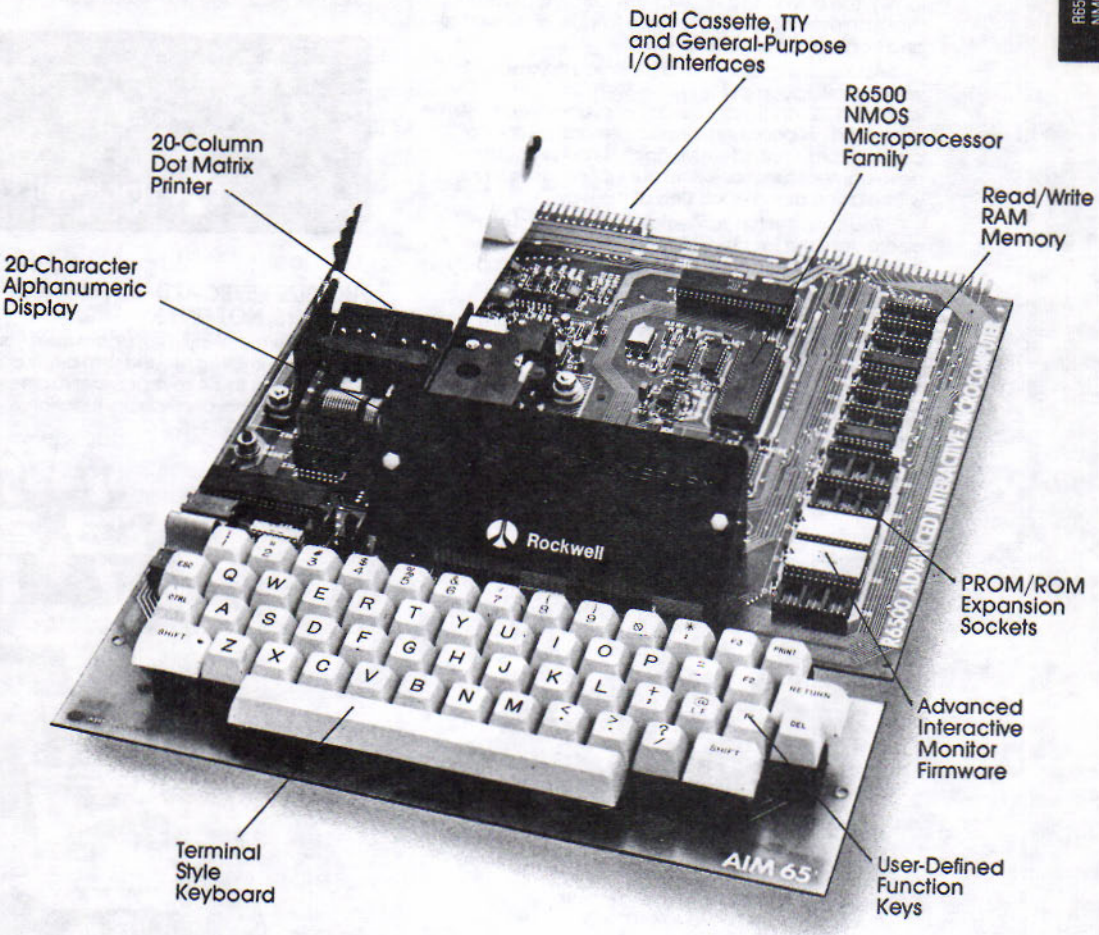
*When programmed as address pins

All values are D.C. readings

# R6500

## Support and Development Systems

# For learning, designing, work or just plain fun...




# Rockwell AIM 65

## The Head-Start in Computers

Rockwell International

# On-Board Printer, Display, Keyboard, Microprocessor, Interfaces and Software Assure Your Computer Head-Start.

## ROCKWELL'S AIM 65...

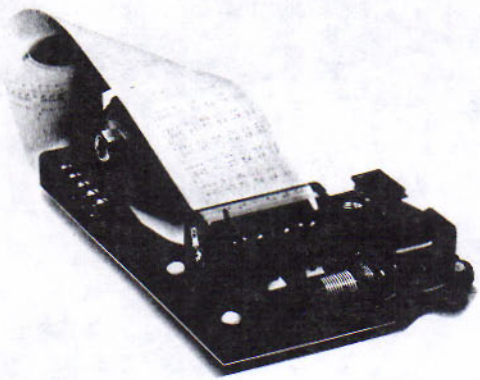
Rockwell's AIM 65 Advanced Interactive Microcomputer can get you into the exciting world of microcomputers a lot easier and at a lower cost than you may have thought possible. And you'll be working with the 6500 family, the advanced state-of-the-art NMOS system that's an ever-increasing favorite for new commercial and hobbyist applications.

As a learning aid, AIM 65 gives you an assembled, versatile microcomputer system with a full-size keyboard, 20-character display and, uniquely, a thermal printer. An on-board Advanced Interactive Monitor program provides extensive control and program development functions. And our AIM 65 User's Manual will help you along each step of the way.

You'll master fundamentals rapidly. Then you'll appreciate the fact that unlike the computer "toys" on the market, AIM 65 offers flexibility and expandability you would expect to find in a sophisticated microcomputer development system.

## THERMAL PRINTER GIVES YOU HARD COPY — FAST AND QUIET.

AIM 65's 20-column Thermal Printer prints on low-cost, thermal roll paper at a fast 120 lines per minute. It produces all of the standard 64 ASCII characters with a crisp-printing five-by-seven dot matrix. AIM 65's on-board printer is a unique feature for a low-cost computer.

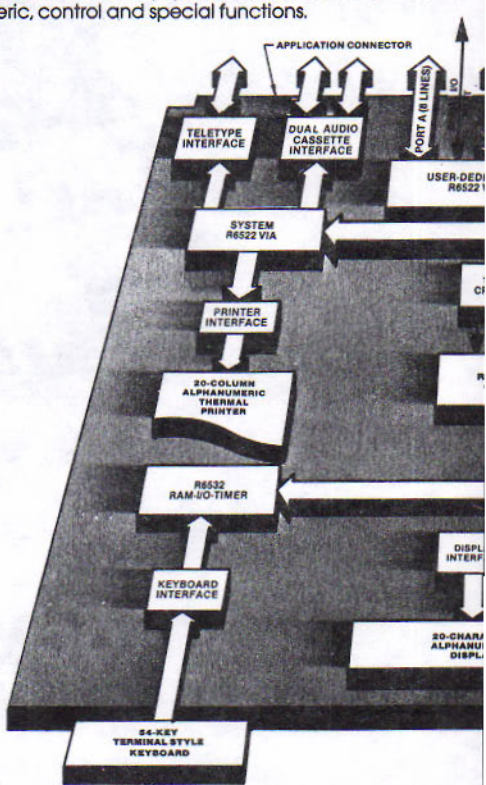


## EXTENDED ALPHANUMERIC DISPLAY IS BUILT FOR UNDERSTANDING, NOT DECIPHERING.

AIM 65 comes with a 20-character true Alphanumeric Display. Information is displayed with bright, magnified 16-segment font monolithic characters. It's both unambiguous and easily readable.


## FULL-SIZE KEYBOARD IS DESIGNED FOR HUMANS, NOT ELVES.

AIM 65's terminal-style keyboard frees you from the hassles of fumbling around with a tiny calculator-type keypad. And its 54 keys provide 70 different alphabetic, numeric, control and special functions.

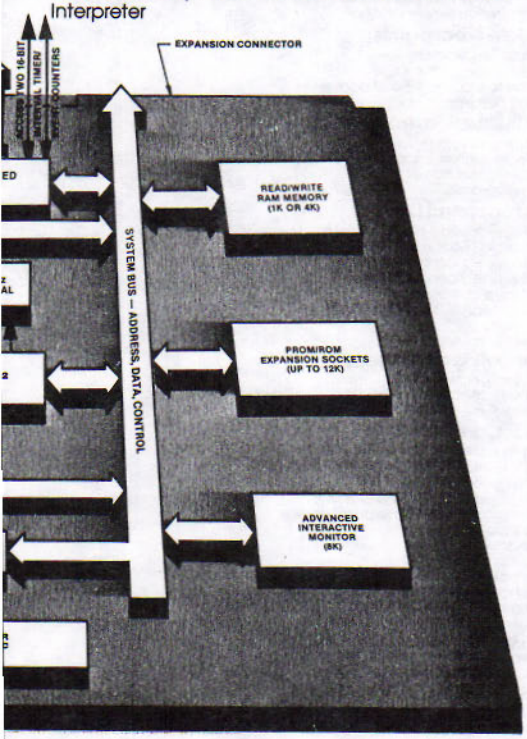


## ON-BOARD ADVANCED INTERACTIVE MONITOR GETS YOUR PROGRAMS UP AND RUNNING.

The ROM-resident AIM 65 Advanced Interactive Monitor Program provides a comprehensive set of easy-to-use, single-keystroke commands for debugging your programs, and offers features normally available only in larger, expensive microcomputer development systems. And with the AIM 65 Monitor, there's no guesswork involved: the Monitor gives a self-explanatory prompt when it needs information and it will generate a meaningful error message if an error has occurred.

The AIM 65 Monitor includes commands to

- Enter and edit programs directly — no "opcode" memorization
- List programs on Printer or TTY
- Display/alter registers and memory
- Set breakpoints, trace and debug program execution
- Control the Thermal Printer
- Transfer information to/from attached Cassette Recorders or TTY
- Execute programs in on-board or external RAM, ROM or PROM memory
- Interface the optional AIM 65 Assembler and BASIC Interpreter




## AIM 65'S ADVANCED R6500 NMOS ARCHITECTURE.

The R6502 Central Processing Unit is the heart of AIM 65. It provides demonstrated speed and simplicity, plus 65K addressability and the power of a 56-command, minicomputer-like instruction set.

The R6532 RAM-Input/Output-Timer (RIOT) combination device is used by the AIM 65 Monitor for scratchpad memory and Keyboard operations.

Two R6522 Versatile Interface Adapter (VIA) devices are provided. One device supports AIM 65's Thermal Printer and the TTY and Cassette Interfaces, the other supports two user-dedicated 8-line I/O ports, plus an 8-bit serial I/O port and access to two 16-bit interval timer/event counters, on the module's Application Connector.

AIM 65 comes with two R2332 4K Read Only Memory (ROM) devices installed. These hold the Advanced Interface Monitor program. Spare sockets allow the user to expand on-board ROM up to 20K bytes. These sockets will accept user programs on R2332 ROMs or compatible PROMs, or can be used to install the optional AIM 65 Assembler and BASIC Interpreter ROM devices.

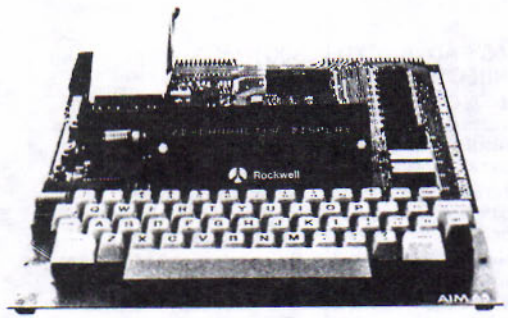
On-Board Read/Write RAM memory is available in 1K-byte and 4K-byte configurations.

## AIM 65 HAS EXPANSION BUILT IN.

And to allow AIM 65 to grow the way **you** want it to, we've provided an Application Connector and an Expansion Connector. The Application Connector permits you to plug on a TTY (20 ma. current loop) and one or two standard audio cassette recorders. It also has the pinouts for the VIA's General-Purpose I/O ports. The Expansion Connector extends AIM 65's system bus — address, data and control — out to additional memory, or anything else you might attach.

And, BASIC high-level language programming is a built-in option.

# AIM 65 Technical Overview




AIM 65 is fully assembled, tested and warranted. With the addition of a low cost, readily available power supply, it's ready to start working for you.

AIM 65 features on-board thermal printer and alphanumeric display, and a terminal-style keyboard. It has an addressing capability up to 65K bytes, and comes with a user-dedicated 1K or 4K RAM. Two installed 4K ROMs hold a powerful Advanced Interface Monitor program, and three spare sockets are included to expand on-board ROM or PROM up to 20K bytes.

An Application Connector provides for attaching a TTY and one or two audio cassette recorders, and gives external access to the user-dedicated general purpose I/O lines.

Also included as standard are a comprehensive AIM 65 User's Manual, a handy pocket reference card, an R6500 Hardware Manual, an R6500 Programming Manual and an AIM 65 schematic.

AIM 65 is packaged on two compact modules. The circuit module is 12 inches wide and 10 inches long, the keyboard module is 12 inches wide and 4 inches long. They are connected by a detachable cable.

## THERMAL PRINTER

Most desired feature on low-cost microcomputer systems...
- Wide 20-column printout
- Versatile 5 x 7 dot matrix format
- Complete 64-character ASCII alphanumeric format
- Fast 120 lines per minute
- Quiet thermal operation
- Proven reliability

## FULL-SIZE ALPHANUMERIC KEYBOARD

Provides compatibility with system terminals...
- Standard 54 key, terminal-style layout
- 26 alphabetic characters
- 10 numeric characters
- 22 special characters
- 9 control functions
- 3 user-defined functions

## TRUE ALPHANUMERIC DISPLAY

Provides legible and lengthy display...
- 20 characters wide
- 16-segment characters
- High contrast monolithic characters
- Complete 64-character ASCII alphanumeric format

## PROVEN R6500 MICROCOMPUTER SYSTEM DEVICES

Reliable, high performance NMOS technology...
- R6502 Central Processing Unit (CPU), operating at 1 MHz. Has 65K address capability, 13 addressing modes and true index capability. Simple, but powerful 56 instructions.
- Read/Write Memory, using R2114 Static RAM devices. Available in 1K byte and 4K byte versions.
- 8K Monitor Program Memory, using R2332 Static ROM devices. Has sockets to accept additional 2332 ROM or 2532 PROM devices, to expand on-board Program Memory up to 20K bytes.
- R6532 RAM-Input/Output-Timer (RIOT) combination device. Multipurpose circuit for AIM 65 Monitor functions.
- Two R6522 Versatile Interface Adapter (VIA) devices, which support AIM 65 and user functions. Each VIA has two parallel and one serial 8-bit, bidirectional I/O ports, two 2-bit peripheral handshake control lines and two fully-programmable 16-bit interval timer/event counters.

## BUILT-IN EXPANSION CAPABILITY

- 44-Pin Application Connector for peripheral add-ons
- 44-Pin Expansion Connector has full system bus
- Both connectors are KIM-1 compatible

## TTY AND AUDIO CASSETTE INTERFACES

Standard interface to low-cost peripherals...
- 20 ma. current loop TTY interface
- Interface for two audio cassette recorders
- Two audio cassette formats: ASCII KIM-1 compatible and binary, blocked file assembler compatible

## ROM-RESIDENT ADVANCED INTERACTIVE MONITOR

Advanced features found only on larger systems...
- Monitor-generated prompts
- Single keystroke commands
- Address independent data entry
- Debug aids
- Error messages
- Option and user interface linkage

## ADVANCED INTERACTIVE MONITOR COMMANDS

### Major Function Entry

(RESET Button) — Enter and initialize Monitor
ESC — Re-enter Monitor
E — Enter and initialize Text Editor
T — Re-enter Text Editor
N — Enter Assembler
5 — Enter and initialize BASIC Interpreter
6 — Re-enter BASIC Interpreter

### Instruction Entry and Disassembly

I — Enter mnemonic instruction entry mode
K — Disassemble memory

### Display/Alter Registers and Memory

. — Alter Program Counter to (address)
A — Alter Accumulator to (byte)
X — Alter X Register to (byte)
Y — Alter Y Register to (byte)
P — Alter Processor Status to (byte)
S — Alter Stack Pointer to (byte)
R — Display all registers
M — Display four memory locations, starting at (address)
(SPACE) — Display next four memory locations
/ — Alter current memory location

### Manipulate Breakpoints

# — Clear all breakpoints
4 — Toggle breakpoint enable on/off
B — Set one to four breakpoint addresses
? — Display breakpoint addresses

### Control Instruction/Trace

G — Execute user's program
Z — Toggle instruction trace mode on/off
V — Toggle register trace mode on/off
H — Trace Program Counter history

### Control Peripheral Devices

L — Load object code into memory from peripheral I/O device
D — Dump object code to peripheral I/O device
1 — Toggle Tape 1 control on/off
2 — Toggle Tape 2 control on/off
3 — Verify tape checksum
CTRL PRINT — Toggle Printer on/off
LF — Line Feed
PRINT — Print Display contents

### Call User-Defined Functions

F1 — Call User Function 1
F2 — Call User Function 2
F3 — Call User Function 3

### Text Editor Commands

R — Read lines into text buffer from peripheral I/O device
I — Insert line into text buffer from Keyboard
K — Delete current line of text
(SPACE) — Display current line of text
L — List lines of text to peripheral I/O device
U — Move up one line
D — Move down one line
T — Go to top line of text
B — Go to bottom line of text
F — Find character string
C — Change character string
Q — Quit Text Editor, return to Monitor

## LOW COST PLUG-IN ROM OPTIONS

- 4K Assembler — symbolic, two-pass
- 8K BASIC Interpreter

## POWER SUPPLY SPECIFICATIONS

- +5 VDC ± 5% regulated @ 2.0 amps (max)
- +24 VDC ±15% unregulated @ 2.5 amps (peak) 0.5 amps (average)

**For more information: Marketing Services, D/727**
**RC55, Rockwell International, Microelectronic Devices**
**P.O. Box 3669, Anaheim, CA 92803 Phone (714) 632-3729**

**Rockwell International**

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The Third-Generation
R6500 Microcomputer System
Puts the Economics on Your Side . . .
Rockwell Adds
Solid Development Support

with the

# SYSTEM65

MICROCOMPUTER DEVELOPMENT SYSTEM

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*SYSTEM 65 has been designed by Rockwell to meet all of the development needs of the R6500 Microcomputer System.*

Rockwell

# SYSTEM65

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## We Think It's More Practical than Any Other Microcomputer Development System . . . And with a Disk Operating System at Under $5500, You Know the Price is Right . . .

Rockwell has included in the SYSTEM 65 every design requirement we've encountered in our long microprocessor experience. (We've been selling microprocessors since 1972, and most industry analysts rate us among the technology's leaders.)

We designed SYSTEM 65 around Rockwell's powerful R6502 CPU. We included two mini-floppy disk drives and a 16K byte static NMOS RAM memory for your software. And we didn't cheat you out of any of this program storage. Our line-oriented, symbolic Text Editor with character and string functions, and our two-pass Assembler and symbolic Debug/Monitor Package are totally stored in ROM. The disk and RAM storage is yours to use.

We made our system software commands easy to use — they're initiated with a single keystroke and they automatically send back meaningful prompts if any additional information is required.

From intimate knowledge of the interfacing requirements Designers encounter during microcomputer development, we included RS-232C and current loop interfaces to accept serial input terminals with operating speeds of between 110 baud and 9600 baud. We added an 8-bit parallel port to permit automatic interfacing to high-speed printers. And because we know how the imaginations of Designers grow as they work with a microcomputer system as versatile as the R6500, we provided six vacant slots in the SYSTEM 65 chassis so that system memory and I/O capability can be expanded at will.

## Here's a Summary of Reasons Why SYSTEM 65 is Just What You're Looking For . . .

- Rockwell R6502 microprocessor (CPU) operates at 1 MHz or (optionally) 2 MHz, and has 65K byte addressing and multi-level interrupts.
- Dual, user-dedicated mini-floppy disk drives. Each drive has a 60-file, 78K byte storage capacity
  User-dedicated 16K byte static RAM memory, expandable in 16K byte increments
- Integral power supply
- System firmware resides in static ROM, fast operation with no loading or reloading required
  - — Symbolic Text Editor performs line, string and character editing functions
  - — Two-pass Assembler can accept source input from either RAM memory or disk and direct object output to any system device
  - — Symbolic Debug/Monitor package operates in single step or real-time
- Eight software breakpoints, for debugging
- Hardware breakpoint on any fetch, read or write to a specified memory location. Scope sync pulse on rear panel connector with each occurance of hardware breakpoint, for real-time debugging.
- Individual RS-232C and current loop interfaces support serial input terminals from 110 baud to 9600 baud
- 8-bit parallel port provides automatic support of high-speed printers for hard copy
- Six vacant circuit board slots tied to system bus, for memory and I/O expansion

**Rockwell's optional USER 65 (User System EvaluatoR) module allows . . .**
the full power of the SYSTEM 65 to be extended into the user's system. By removing the R6500 CPU from the user system and connecting the USER 65 cable into the CPU socket, the SYSTEM 65 Debug firmware can be used to test and troubleshoot microprocessor systems.

## Here Are the SYSTEM 65's Hardware Details

The SYSTEM 65 enclosure contains four printed circuit modules:

- CPU Module holds the R6502 microprocessor and its supporting circuits, and serial baud rate select switch
- Monitor Module contains 1K bytes of static RAM and 14K bytes of static ROM, which holds all system software
- RAM Memory Module contains 16K bytes of user-dedicated static RAM
- I/O Module provides the hardware interface to the system input/output devices

Note that since all RAM memory is static, the processor is not required to provide the clock and strobe functions associated with dynamic memory.

The SYSTEM 65 enclosure also has six vacant slots, which allow users to add any combination of memory and I/O interfaces in building a customized development system.

The built-in mini-floppy disk drives can each hold up to 60 files with a per drive storage capacity of 78K bytes. Like the RAM memory, the mini-floppy disk drives are 100% user-dedicated.

The RUN/STEP switch on the front panel allows you to select either single step execution or real-time execution of programs.

The back panel has four device connectors: an 8-bit parallel port for connecting a high-speed printer, an RS-232C serial interface connector, a current loop serial interface connector and a scope sync connector. The CPU Module has a rotary switch to select any of eight baud rates — 110, 150, 300, 600, 1200, 2400, 4800 or 9600 baud — for compatability with the serial input/output device.

### And Rockwell offers these options to SYSTEM 65:

- PL/65 High-Level Language
- USER 65 in-circuit emulation option
- PROM Programmer Module, for programming a 2704/2708/2716/2758 PROM device from the front panel socket
- R6500/1 Personality option, for developing with the R6500/1 single-chip microcomputer
- 16K x 8 Static RAM Modules
- PROM/ROM Module, accepts 2316/2332 ROM or 2708/2716/2758 PROM devices
- Wire-wrap Design Prototyping Module
- Extender Card for circuit probing

## Here Are the SYSTEM 65's Software Details

### The Text Editor

The SYSTEM 65 Text Editor is used to prepare user programs for assembly. The Text Editor writes the program source code into RAM memory from any system device and, when editing has been completed, writes it to any system device. The editing operation can include line editing, string editing and character editing.

The line-oriented commands provide overall control in finding lines to be edited, and specify the system devices for input and output of text. The string-oriented commands can be used to insert program source code into memory, or to search for an existing character string — perhaps a program label or a certain opcode/operand combination — and (if desired) provide a substitute for that string. The character-oriented commands provide control over the cursor position on a line and a character delete command.

### Text Editor Command Summary

#### Line-Oriented Commands

R - Read lines into text buffer from [device]
I - Insert one line from system terminal
K - Delete [count] lines of text, starting with current line
U - Backspace [count] lines of text
D - Advance [count] lines of text
T - Go to top (beginning) line of text; i.e., re-enter Text Editor
B - Go to bottom (last) line of text
L - List [count] lines on [output device]
? - Show address of current and last lines
G - Go to line [number]
(sp) - Show current line

#### String-Oriented Commands

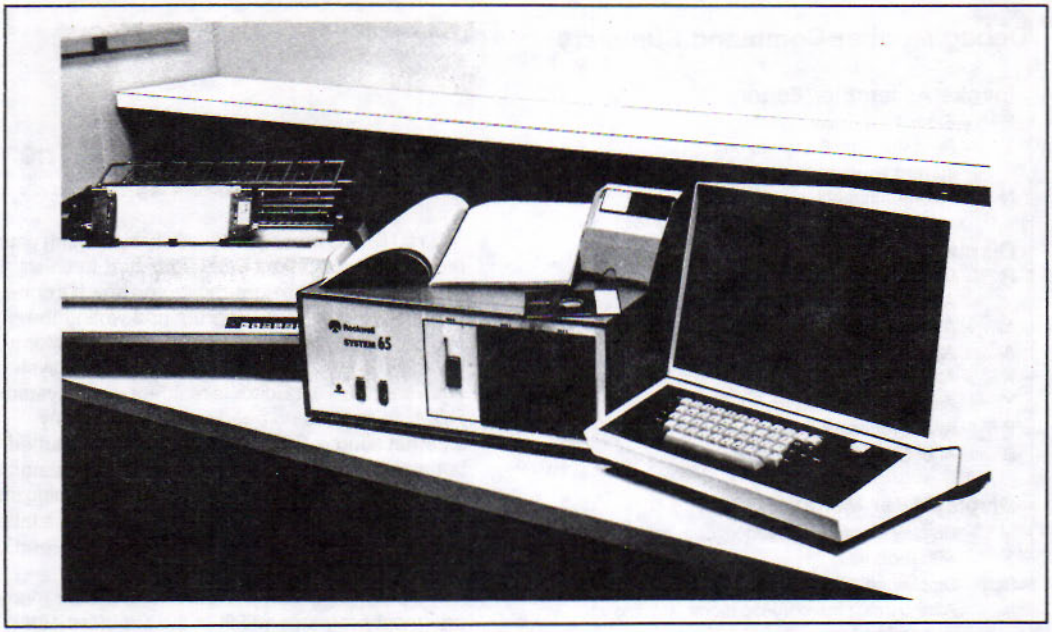
F - Find [string], starting with current line
C - Find [string], starting with current line, and change it to [string]
A - Add [string] to line, starting with current cursor position

#### Character-Oriented Commands

/ - Delete current character
+ - Advance cursor [count] positions
– - Backspace cursor [count] positions

#### Miscellaneous

Q - Exit to Debug




## The Assembler

The SYSTEM 65 Assembler is a two-pass assembler that includes the option to list only the errors detected, if any. This "errors-only" option generates a display of all source statements that contain syntax errors, unresolved references and the like. With the results of this quick check, the Text Editor can be used to make the proper corrections before the Assembler generates the full assembly listing, symbol table and object code. The "errors-only" option can prove to be quite a time- and paper-saver.

The Assembler can accept input from either RAM memory or disk, and has a powerful chaining feature that allows multiple disk files of a large program to be assembled in one operation. These files may reside on either disk, or even on a disk that has not been mounted (the Assembler will direct you to mount it).

For output, the Assembler gives the user complete control over the extent of the listing, which system device will receive the output and whether the entire text of ASCII strings is to be output.

## The Debug/Monitor Package

The SYSTEM 65 Debug/Monitor package provides a comprehensive set of easy-to-use commands and functions for debugging development programs in either single step or real-time mode.

The register commands allow you to display the current contents of the Processor registers, and to selectively alter any of these registers.

The memory commands allow you to display the contents of memory in blocks of eight locations, to alter one or more consecutive locations and to write protect any 8K block of addresses in memory. Further, memory can be loaded from or output to any system device.

Debug also has a compliment of breakpoints, to give you an easy way to trace program execution. Upon encountering a breakpoint the program displays a symbolic disassembly of the label (if any), opcode and operand field at the breakpoint location. This important feature ties the symbol table, created by the Assembler, with the Debug software. This means that all debugging is done at the assembler language level — without the need to plod through machine code printouts. There are eight software breakpoints and one hardware breakpoint (in addition to the BRK instruction in the R6500 instruction set).

The Debug command set iricludes all the commands necessary to set and clear software breakpoints, as well as to enable and disable them.

Debug also makes disk management virtually transparent, reducing functions like initializing, compressing, opening and deleting files to single keystroke commands.

## Debug/Monitor Command Summary

### Invoke Assembler/Editor

E - Enter Text Editor
T - Re-enter Text Editor, to edit current source
N - Invoke Assembler

### Display/Alter Registers

R - Display registers (Program Counter, Accumulator, X, Y, Status and Stack Pointer)
* - Alter Program Counter to [address]
A - Alter Accumulator to [byte]
X - Alter X Register to [byte]
Y - Alter Y Register to [byte]
P - Alter Processor Status to [byte]
S - Alter Stack Pointer to [byte]

### Display/Alter Memory

M - Display eight memory locations, starting with [address]
(sp) - Display next eight memory locations
/ - Alter current memory locations, starting with [address]
W - Display/alter write protect status

### Load/Dump Memory

L - Load object code into memory from [input device]
D - Dump memory from [address] to [address[ to [output device]

### Manipulate Breakpoints

# - Clear all software breakpoints
4 - Toggle software breakpoint enable on/off
B - Set/clear software breakpoint addresses
? - Display software breakpoint addresses
C - Display/alter hardware breakpoint

### Control Execution/Trap

G - Execute user's program, at currect Program Counter address
Z - Toggle instruction trace mode on/off
V - Toggle register printout on trapping on/off
J - Print register header
H - Display trace history stack, 10 addresses

### Disk Functions

1 - Special disk functions (compress, list, rename, recover, initialize)
2 - List disk directory
3 - Delete file

## Program Development — The Easy SYSTEM 65 Way

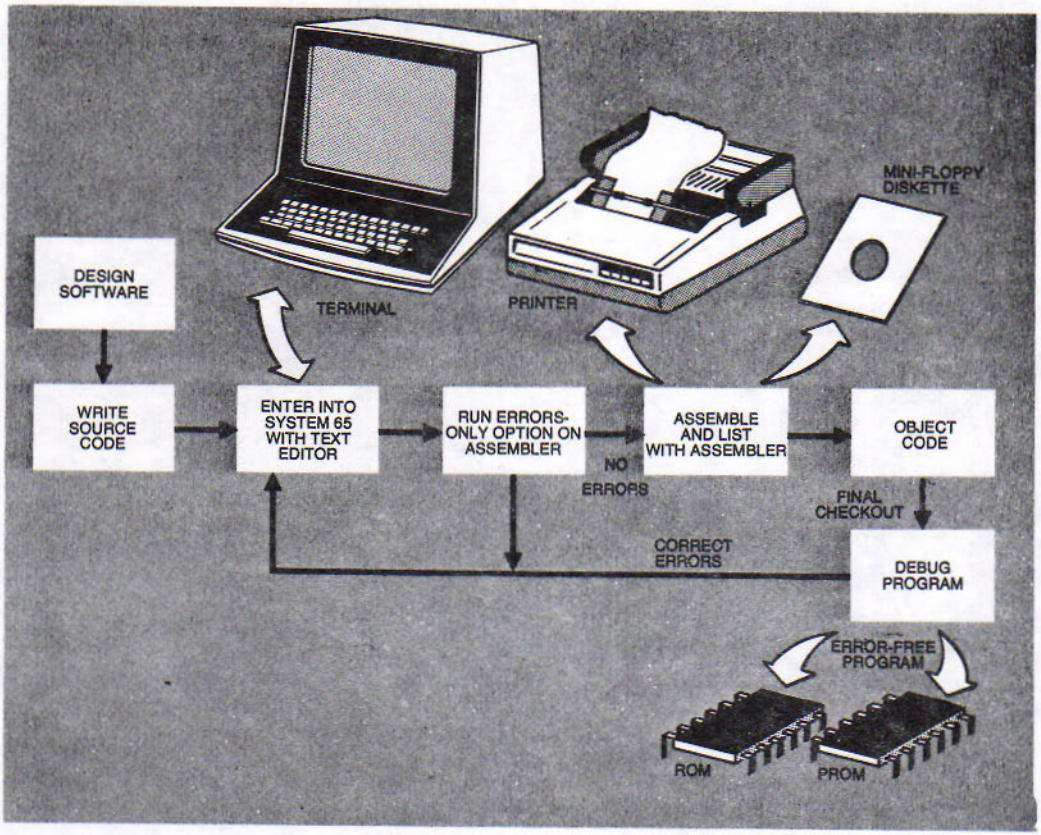
SYSTEM 65 means productivity by making your program development easy from start to finish. The flowchart at the right shows you how it's done.

After designing the program and writing the source code, you will be using the Text Editor to enter the code into RAM memory. Like all system software, the Text Editor is resident in the system ROM, so there is no need to load it from any external source. The Text Editor is line-oriented, but also has string and character manipulation functions. It includes the capability of searching for a specified character string — for example, a label or an opcode-and-operand combination — and replacing it with a different string.

If a program is small relative to available memory (most programs will fit in the standard 16K bytes of RAM) it can remain there through the editing, assembling and debugging processes. Very large programs are usually developed in pieces, stored on disk, and later linked together by the Assembler. SYSTEM 65 is designed to permit easy communication with disk, by handling all files by their logical names and automatically creating each file when its filename is first used.

With the source code entered and edited (and if necessary stored on disk), it can now be assembled. The SYSTEM 65 resident Assembler is called by a single key stroke. The Assembler is a two-pass assembler that includes the option to list only the errors detected. This "errors-only" option is usually used as a first quick, easy check on the integrity of your program. If errors are found, they can be corrected by recalling the Text Editor.

When all errors have been eliminated, the Assembler is used to generate a full assembly listing, symbol table and object code. At this point the symbolic Debug program is used to test and correct the program. Debug may use the symbol table produced by the Assembler, so your original source code labels can be carried through to the debug process. When the program is in completed form and error-free, you can run one more assembly to generate a listing for documentation purposes. The object output can also be put on PROM via the optional PROM Programmer, or sent to Rockwell for storage on ROM.




## Where to Get More on SYSTEM 65

To order SYSTEM 65, or to get a copy of the SYSTEM 65 User's Manual (nominal $5 charge), contact the nearest Rockwell office or distributor listed on the back of this brochure. For in-depth assistance, obtain the name of your nearest Rockwell sales representative from any Rockwell office.

DOCUMENT NO. 29650 N43
OCTOBER 1978

PART NOs.
M65-001, M65-002

Rockwell

# R6500 Microcomputer System PRODUCT DESCRIPTION



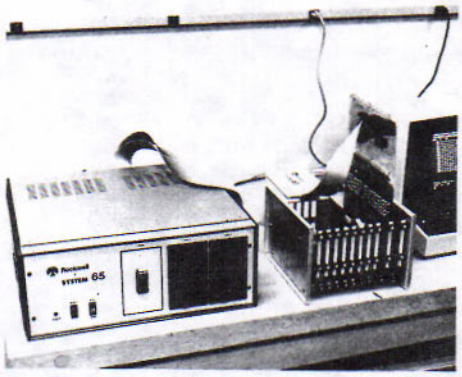


## USER 65 OPTION

### OVERVIEW

The USER 65 permits users who are developing R6500-based products to extend the full power of SYSTEM 65 into their equipment for in-circuit emulation. Available in both 1- and 2-MHz versions (M65-001 and 002), USER 65 supports all ten R6500 CPU's.

USER 65 consists of two modules — a Host Module and a Buffer Module — and two interconnect cables. The USER 65 Host Module replaces the CPU Module in the SYSTEM 65 chassis; it performs all CPU Module functions, plus several external functions. The USER 65 Buffer Module extends the SYSTEM 65 bus lines (address, data and control) to the user equipment.



### FUNCTIONAL DESCRIPTION

#### USER 65 HOST MODULE

The USER 65 Host Module (shown in block diagram form in Figure 1) replaces the CPU Module in the SYSTEM 65 chassis. It is capable of performing all functions of the CPU Module, plus external address selection, automatic power up, and external clock selection. The schematic of the Host Module is PS00-X183. The Host Module interface signals are listed in Table 1.

The heart of the Host Module is the R6502 (Z11) microprocessor. It controls all functions of the SYSTEM 65 and the user's external equipment. Crystal Y1 (1 or 2 MHz) generates the internal clock for the R6502 CPU. Switch S3 is used to select either the internal generated clock or an externally provided clock input.

The Host Module has automatic power-up circuit consisting of an NE555 timer (Z3) and associated discrete capacitors and resistors. This circuit will generate a 100 msec reset pulse following power-up.

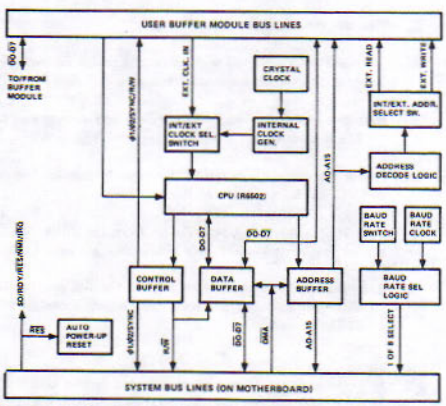



**Figure 1. USER 65 Host Module Functional Block Diagram**

The Host Module also contains the RS-232C and TTY baud rate generator circuitry. Crystal Y2 (1.8432 MHz) and baud rate generator MC14411 (Z13) generate a baud rate clock. The Clock rate is multiplied by 16 (x16) to provide a selectable output baud rate from 110 to 9600. Switch S4 and the SN74152 (Z12) select the baud rate. This output is then provided to the SYSTEM 65 bus to be used by the Monitor Module.

The internal/external address selection is based on a decode of A15-A12, using an SN74159N (Z1) decoder. This device has sixteen active low outputs. Each output represents a 4K address space and is selected by Switches S1 and S2. The outputs are ORed together and inverted by SN7406 (Z2). This enable signal is then gated with R/$\overline{W}$ signal to form a READ signal and a WRITE signal, which are used in the USER 65 Buffer Module.

The address lines and control lines $\phi$1, $\phi$2, $\overline{DMA}$, and SYNC are buffered with I.C.'s 8T97 (Z8-Z10, Z5). The data lines are inverted and buffered with I.C.8T26 (Z6, Z7). All of these lines are brought to the SYSTEM 65 bus and are also taken out to the USER 65 Buffer Module through series terminators (A1-A4).

The Control lines S.O., RDY, $\overline{RES}$, $\overline{NMI}$, $\overline{IRQ}$ are brought to the SYSTEM 65 bus and are also brought from the USER 65 Host Module, then buffered with open collector buffers SN7407(Z15). These inputs come only from the user's equipment; the RESET switch on the front panel will not reset the external equipment.

SYSTEM 65 bus line $\overline{DMA}$ is used to control the address and data bus lines. This line is pulled up internally with a 3K resistor. By pulling $\overline{DMA}$ low, the address, data and R/W lines are set to the float state, allowing an external board to control them for DMA operations. The $\overline{DMA}$ line does not stop the CPU — this must be done by controlling the RDY line as outlined in the R6500 Microprocessor Data Sheet (29000 D39).

**Table 1. USER 65 Host Board to Buffer Board Interface Signals**

Note: Even-numbered pins are connected to Ground.

| CONNECTOR J1 | | CONNECTOR J2 | |
|---|---|---|---|
| PIN | SIGNAL | PIN | SIGNAL |
| 1 | A0 | 1 | EXT. CLOCK |
| 3 | A1 | 3 | Ø2 |
| 5 | A2 | 5 | Ø1 |
| 7 | A3 | 7 | GATED READ |
| 9 | A4 | 9 | GATED WRITE |
| 11 | A5 | 11 | $\overline{D7}$ |
| 13 | A6 | 13 | $\overline{D6}$ |
| 15 | A7 | 15 | $\overline{D5}$ |
| 17 | A8 | 17 | $\overline{D4}$ |
| 19 | A9 | 19 | $\overline{D3}$ |
| 21 | A10 | 21 | $\overline{D2}$ |
| 23 | A11 | 23 | $\overline{D1}$ |
| 25 | A12 | 25 | $\overline{D0}$ |
| 27 | A13 | 27 | +5V |
| 29 | A14 | 29 | +5V |
| 31 | A15 | 31 | +5V |
| 33 | SYNC | 33 | +5V |
| 35 | R/$\overline{W}$ | 35 | +5V |
| 37 | RDY | 37 | +5V |
| 39 | $\overline{RESET}$ | 39 | +5V |
| 41 | $\overline{NMI}$ | | |
| 43 | $\overline{IRQ}$ | | |
| 45 | S0 | | |

### USER 65 BUFFER MODULE

The USER 65 Buffer Module receives the address, data and control lines from the USER 65 Host Module, buffers these signals and interfaces them to the user's equipment. Figure 2 is a block diagram. The schematic of the USER 65 Buffer Board is P500-X193.

The address lines, SYNC and R/$\overline{W}$ lines are buffered with I.C.'s 8T97 (Z1-Z3). The control lines RDY, $\overline{RES}$, $\overline{NMI}$, $\overline{IRQ}$, and S.O. are buffered with open collector I.C.'s SN7407 (Z4). The data lines are inverted and buffered with I.C.'s 8T26A (Z7 and Z8). They have series terminators of 150 ohms (Z9).

The Ø1 and Ø2 clocks are buffered by 8T97 (Z5). To use an external clock, jumper N must be installed. To use Ø1, jumper M must be installed. The DBE signal is provided for use during emulation of the R6512 CPU. This line has an internal pullup resistor of 3K. When brought low it will disable the data bus drivers.

Two other signals, READ and WRITE, are buffered by Z5. The READ signal is generated by the Host Module and is high when the R/$\overline{W}$ line is high and an external address is active. The WRITE signal, also generated by the Host Module, is high when R/$\overline{W}$ line is low and an external address is active. These two lines control the data bus buffers Z7 and Z8.

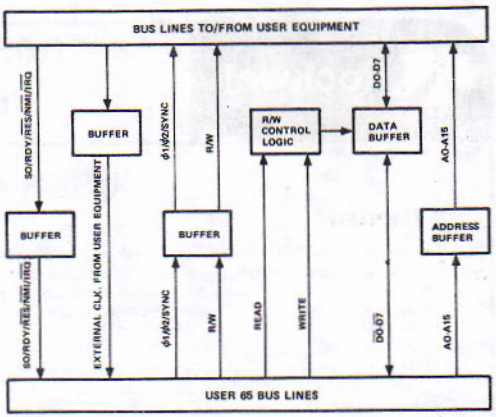



**Figure 2. USER 65 Buffer Module Functional Block Diagram**

### USER 65 CABLES

The cable assembly supplied with the USER 65 option provides the signal paths between the USER 65 Host and Buffer Modules, and between the Buffer Module and the user's equipment. Since the USER 65 option is designed to emulate all versions of the R6500 Family of CPU's, both a 40-pin cable and two 28-pin types of cables are provided.

## INSTALLATION

### USER 65 HOST MODULE INSTALLATION

Install the USER 65 Host Module in the SYSTEM 65 as follows:

1. Turn SYSTEM 65 power off.

   **CAUTION**

   Never install or remove modules with SYSTEM 65 power on — it may cause damage to the module and/or to the system.

2. Remove the top cover of the SYSTEM 65.
3. Remove the CPU Module.
4. Set switches S1, S2, S3 and S4 on the USER 65 Host Module per Table 2. The switch positions are shown in Figure 3.
5. Plug the USER 65 Host Module into any convenient slot in the SYSTEM 65 chassis.
6. Route the cables from the Buffer Module through the back panel of SYSTEM 65, through the slot provided.
7. Connect the 40- and 50-pin cables from the Buffer Module to the top of the Host Module (the connectors are keyed with arrows).
8. Set switches S1 and S2 on the RAM Module per Tables 3 and 4 to enable/disable and to select the address range of the internal SYSTEM 65 RAM.

   **NOTE**

   If external RAM addresses are selected on the USER 65 and the same addresses are selected and enabled on the SYSTEM 65 internal RAM board(s), the internal RAM will override and prevent proper operation of the external RAM.

9. Install the top cover of the SYSTEM 65.

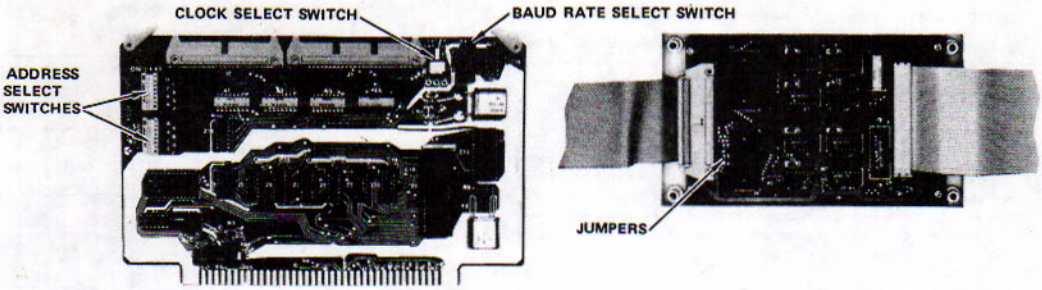



Figure 3. USER 65 Host and Buffer Modules

Table 2. USER 65 Host Module Switches

| SWITCH | FUNCTION |
|---|---|
| S1/S2 | ADDRESS SELECT<br>These switches determine whether address selection is internal or external for each 4K byte portion of memory space. External memory is selected when the switch is ON, internal memory is selected when the switch is OFF.<br><br>S1 Switch — Address Range<br>1 — $0000 - $0FFF<br>2 — $1000 - $1FFF<br>3 — $2000 - $2FFF<br>4 — $3000 - $3FFF<br>5 — $4000 - $4FFF<br>6 — $5000 - $5FFF<br>7 — $6000 - $6FFF<br>8 — $7000 - $7FFF<br><br>S2 Switch — Address Range<br>1 — $8000 - $8FFF<br>2 — $9000 - $9FFF<br>3 — $A000 - $AFFF<br>4 — $B000 - $BFFF<br>5 — $C000 - $CFFF<br>6 — $D000 - $DFFF<br>7 — $E000 - $EFFF<br>8 — $F000 - $FFFF |
| S3 | CLOCK SELECT<br>Switch S3 selects either the SYSTEM 65 clock (INT) or an external, user-supplied clock (EXT). If an external supplied clock is used, the frequency must be 1 or 2 MHz + 1% if operation of the SYSTEM 65 mini-floppy disks is required. It must always be a TTL level, square wave, clock input. |
| S4 | BAUD RATE SELECT<br>This switch determines the baud rate for either the RS-232C or TTY ports. Switch settings are:<br><br>(S4) POSITION — BAUD RATE<br>0 — 110<br>1 — 150<br>2 — 300<br>3 — 600<br>4 — 1200<br>5 — 2400<br>6 — 4800<br>7 — 9600 |

Table 3. RAM Module Enable/Disable Switch Definition

| Switch S1/S2-4 Position | RAM Enable/Disable State |
|---|---|
| Up (Off) | RAM Disabled (Deselected) |
| Down (On) | RAM Enabled (Selected) |

Table 4. RAM Address Range Select Switch Settings

| Switch S1/S2 Position | | | |
|---|---|---|---|
| -1 | -2 | -3 | 8K Address Range Selected |
| Up | Up | Up | $0000 - $1FFF |
| Down | Up | Up | $2000 - $3FFF |
| Up | Down | Up | $4000 - $5FFF |
| Down | Down | Up | $6000 - $7FFF |
| Up | Up | Down | $8000 - $9FFF |
| Down | Up | Down | $A000 - $BFFF |
| Up | Down | Down | $C000 - $DFFF |
| Down | Down | Down | $E000 - $FFFF |

Note: "Up" is toward the top edge of the module

## USER 65 BUFFER MODULE INSTALLATION

Since the Buffer Module is designed to support all CPU's in the R6500 family, specific jumpers or straps must be inserted to support the exact CPU being emulated. Table 5 gives the strapping requirements. Jumper locations are shown in Figure 3.

The Buffer Module has two modes for the R/W line. For 40-pin CPU emulation (R6502 and R6512), the R/W line is connected to the user's equipment as is. Since the 28-pin CPU's do not provide all the address lines to the user's equipment, address conflicts can occur during SYSTEM 65 Monitor execution. A gated R/W line is provided to prevent these conflicts; this line is normally high, and goes low only when an external address is present and R/W is low.

The Buffer Module also has straps for clock selection. One strap allows the Ø1 (OUT) signal to go to the user's equipment. The other strap is used to allow an external clock [Ø0 (IN) or Ø2 (IN)] to be used. Switch S3 on the Host Module must be set to EXT when the external clock is used.

The Buffer Module is provided with three sockets and three cables. The 40-pin socket (J3) should be used for either of the 40-pin CPU's, R6502 or R6512. The cable labeled PS00-D603-001 should be used to connect from J3 to the user's equipment. The other two sockets (J4 and J5) are for use with the 28-pin CPU's. Table 5 correlates the socket and 28-pin cable to be used for each of the 28-pin CPU versions.

The DBE (Data Bus Enable) line for the R6512 is available to the user's equipment. There is an internal 3K pullup resistor in the Buffer Module, so it can be left open if desired. To disable the data output drivers, pull the DBE line low.

The installation procedure is:

1. Remove the top of the USER 65 Buffer Module assembly.
2. Insert the desired jumpers, per Table 5.
3. Connect either the 40-pin cable to plug J3 or the 28-pin cable to plug J4 or J5, as appropriate.
4. Reinstall the top of the Buffer Module assembly.
5. Plug the free connector of the cable into the user's equipment.

**NOTE**

Any conductive foam must be removed from the CPU plug pins to allow proper SYSTEM 65 operation even when the CPU plug is not connected to user equipment.

6. Turn SYSTEM 65 and user's equipment power on.

**Table 5. USER 65 Buffer Module Connection Requirements**

| User Equipment CPU | Buffer Module Socket | Cable To User Equipment | Jumper | Signal | User's CPU Pin |
|---|---|---|---|---|---|
| R6502 | J3 | PS00-D603-001 | R | R/W | 34 |
| | | | M | Ø1 (OUT) | 3 |
| | | | N* | Ø0 (IN) | 37 |
| R6503 | J4 | PS00-D605-001 | P | R/W | 26 |
| | | | B | $\overline{RES}$ | 1 |
| | | | D | VSS | 2 |
| | | | E | $\overline{IRQ}$ | 3 |
| | | | F | $\overline{NMI}$ | 4 |
| | | | A | Ø2 (OUT) | 28 |
| | | | N* | Ø0 (IN) | 27 |
| R6504 | J5 | PS00-D605-001 | P | R/W | 26 |
| | | | B | $\overline{RES}$ | 1 |
| | | | D | VSS | 2 |
| | | | E | $\overline{IRQ}$ | 3 |
| | | | A | Ø2 (OUT) | 28 |
| | | | N* | Ø0 (IN) | 27 |
| R6506 | J4 | PS00-D605-001 | P | R/W | 26 |
| | | | B | $\overline{RES}$ | 1 |
| | | | D | VSS | 2 |
| | | | K | RDY | 3 |
| | | | S | $\overline{IRQ}$ | 4 |
| | | | A | Ø2 (OUT) | 28 |
| | | | N* | Ø0 (IN) | 27 |
| R6506 | J4 | PS00-D605-001 | P | R/W | 26 |
| | | | B | $\overline{RES}$ | 1 |
| | | | D | VSS | 2 |
| | | | L | Ø1 (OUT) | 3 |
| | | | S | $\overline{IRQ}$ | 4 |
| | | | A | Ø2 (OUT) | 28 |
| | | | M | Ø1 (OUT) | 3 |
| | | | N* | Ø0 (IN) | 27 |
| R6507 | J5 | PS00-D605-001 | P | R/W | 26 |
| | | | B | $\overline{RES}$ | 1 |
| | | | D | VSS | 2 |
| | | | K | RDY | 3 |
| | | | A | Ø2 (OUT) | 28 |
| | | | N* | Ø0 (IN) | 27 |
| R6512 | J3 | PS00-D603-001 | R | R/W | 34 |
| | | | N* | Ø2 (IN) | 37 |
| R6513 | J4 | PS00-D604-001 | P | R/W | 26 |
| | | | C | VSS | 1 |
| | | | E | $\overline{IRQ}$ | 3 |
| | | | F | $\overline{NMI}$ | 4 |
| | | | T | $\overline{RES}$ | 28 |
| | | | N* | Ø2 (IN) | 27 |
| R6514 | J5 | PS00-D604-001 | P | R/W | 26 |
| | | | C | VSS | 1 |
| | | | E | $\overline{IRQ}$ | 3 |
| | | | T | RES | 28 |
| | | | N* | Ø2 (IN) | 27 |
| R6515 | J4 | PS00-D604-001 | P | R/W | 26 |
| | | | C | VSS | 1 |
| | | | J | RDY | 2 |
| | | | L | | |
| | | | S | $\overline{IRQ}$ | 4 |
| | | | T | $\overline{RES}$ | 28 |
| | | | N* | Ø2 (IN) | 27 |

*Jumper N is required with an external clock. Switch S3 on the USER 65 Host Module must be positioned to the EXT position when the extended clock or frequency reference is used.

## USER 65 TYPICAL APPLICATION

A typical application for the USER 65 option is depicted in Figure 4.

The user's system may include any combination of ROM's, PROM's, RAM's, I/O devices, and a 40- or 28-pin CPU socket. For emulation purposes, the USER 65 option is installed in the CPU socket instead of a CPU. The user must provide page 0($0000-$00FF) and page 1($0100-$01FF) either internally or externally for use by the SYSTEM 65 Monitor. For system development purposes, the user's ROM may be emulated with one or more RAM modules provided in the SYSTEM 65 chassis. This permits easy manipulation, debugging, and reassembly of the user's program during the development phase. For editing and assembling of the source program, the user may use the SYSTEM 65 RAM or may provide his own RAM modules externally.

The USER 65 option may be used with the SYSTEM 65 Monitor enabled or disabled. With SYSTEM 65 Monitor enabled, the full resources of the SYSTEM 65 Monitor are available for program checkout and debugging. In this mode the SYSTEM 65 uses addresses $C000-$FFFF; these addresses cannot be used by the programmer.

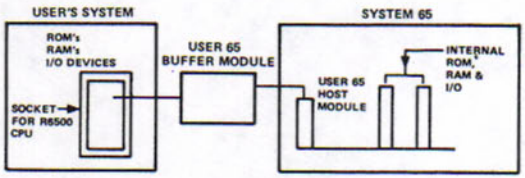



**Figure 4. USER 65 Option Hook-up**

## USER 65 HOST AND BUFFER MODULE SPECIFICATIONS

**Common Specifications**

Operating Frequency: 1 MHz or 2 MHz

Operating Temperature: $0^{o}$ to $70^{o}$C

Power Requirements: +5 VDC ± 5% @ 1.5A

**Host Module Specifications**

Module Dimensions: 9.75 in. wide x 7.50 in. high

Edge Contacts: 86 pins on 0.156 in. centers

Edge Contact Signals: SYSTEM 65 compatible

**Buffer Module Specifications**

Module Dimensions: 4.125 in. wide x 7.375 in. high

Cable Lengths:

| | | |
|---|---|---|
| To | SYSTEM 65 | 60 in. |
| To | User Equipment | 12 in. |

DOCUMENT NO. 29650 N46
AUGUST 1978

PART NUMBERS
M65-031, M65-032

Rockwell

# R6500 Microcomputer System PRODUCT DESCRIPTION



# 16K STATIC RAM MODULE

## OVERVIEW

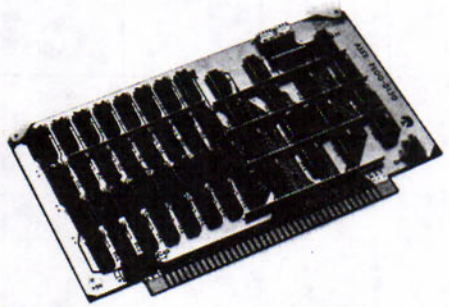
The Static RAM Module contains 16K (16,384) bytes of Random Access Memory (RAM), implemented with 32 R2114 1024 x 4 Static RAM devices. The Module also includes address decoding and selection, write protection and data buffering circuitry.

The Module's 16K bytes of RAM memory are segmented into two independent 8K-byte sections. Each 8K section is controlled by an enable/disable switch and three address range select switches, located at the top of the Module. Each 8K section can be independently write-protected via special lines.

The Static RAM Module is directly compatible with Rockwell's SYSTEM 65 Microcomputer Development System, and can be used to increase the System's read/write memory capacity from 16K bytes to 48K bytes, without hardware modification. The Module may also be installed into user-designed equipment, via the Auxiliary Card Cage.

## FEATURES

- SYSTEM 65 compatible
- Available in 1 MHz (450 ns access) and 2 MHz (250 ns access) versions.
- 16K bytes of Random Access Memory, with two independent 8K sections
- Separate write protect capability for each 8K section
- Static — no clocks or strobes required
- 9.75 in. x 6.00 in. module
- Single +5V supply



## FUNCTIONAL DESCRIPTION

In reading the text to follow, refer to the Functional Block Diagram below and the attached schematics:

- PS00-X131, the -001 assembly of the RAM Module
- PS00-X133, the -071 assembly of the RAM Module

The edge connector pin assignments for the RAM Module are compatible with the Motherboard pin assignments given in Section 4 of the SYSTEM 65 User's Manual (Document No. 29650 N35).

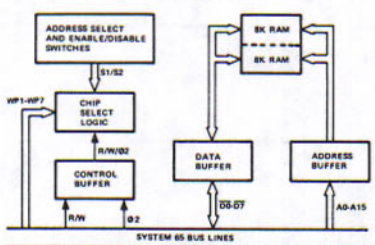
The RAM Module's 16K bytes of read/write memory are provided by 32 R2114 1024 x 4-bit Static RAM devices.

Address Buffers Z47, Z46 and Z33 and Data Buffers Z32 and Z45 present a single TTL load to the Motherboard edge connector. The data signals are inverted to make them compatible with the SYSTEM 65 Data Bus ($\overline{D0}$-$\overline{D7}$).

Module Switches S1 and S2 provide independent 8K RAM section enable/disable and address selection. S1-4 and S2-4 permit each 8K section of RAM to be enabled or disabled. S1-1, -2 and -3 and S2-1, -2 and -3 select the base address to which the respective 8K sections will respond. These switch settings are compared to upper address bits A13, A14 and A15 in Address Comparator devices Z10 and Z21. The Comparator outputs enable or disable 1-of-8 Decoder devices Z9 and Z20 to provide the input chip select signals to the two 8K RAM sections.

Write protection is controlled by seven Write Protect lines, WP1-WP7, one line for each 8K section of memory (the lowest section, addresses $0000-$1FFF, may not be write protected; note that Z48-2 is tied to ground to permanently enable writing to this section). A low voltage on WP1-WP7 enables writing into the associated 8K section.

When the Address Comparator enables the RAM Device Select Decoders, Address Select switches S1-1 through S1-3 and S2-1 through S2-3 are used by Z35 and Z36 to select one of the seven Write Protect lines. The selected line controls the RAM Write Control signals, Z34-6 and Z34-8.




RAM Module Functional Block Diagram

## INSTALLATION

The procedure below should be used to install 16K Static RAM Modules in the SYSTEM 65 or, with appropriate changes, in an Auxiliary Card Cage.

1. Turn SYSTEM 65 power off.

**CAUTION**

Never install or remove modules with SYSTEM 65 power on — It may cause damage to the module and/or to the System.

2. Remove the top cover of the SYSTEM 65.

3. The RAM Module has two banks of switches — S1 and S2 — one bank for each 8K section of RAM. Using Tables 1 and 2, select the enable/disable and address range characteristics for each 8K section.

**NOTES**

For proper SYSTEM 65 operation . . .

a. Page 0 (address range $0000-$00FF) and Page 1 ($0100-$01FF) must be provided in RAM — either internal RAM or external RAM as interfaced by USER 65 or its equivalent.

b. RAM addresses in the range $C000-$FFFF are used by the SYSTEM 65 Monitor Board, and must not be enabled in RAM Modules.

4. Insert the RAM Module(s) into any vacant slot(s) in the SYSTEM 65 chassis.

5. Install the top cover of the SYSTEM 65.

6. Turn SYSTEM 65 power on.

**Table 1. RAM Enable/Disable Switch Settings**

| Switch S1/S2-4 Position | RAM Enable/Disable State |
|---|---|
| Up (Off) | RAM Disabled (Deselected) |
| Down (On) | RAM Enabled (Selected) |

**Table 2. RAM Address Range Select Switch Settings**

| Switch S1/S2 Position | | | |
|---|---|---|---|
| -1 | -2 | -3 | 8K Address Range Selected |
| Up | Up | Up | $0000 - $1FFF |
| Down | Up | Up | $2000 - $3FFF |
| Up | Down | Up | $4000 - $5FFF |
| Down | Down | Up | $6000 - $7FFF |
| Up | Up | Down | $8000 - $9FFF |
| Down | Up | Down | $A000 - $BFFF |
| Up | Down | Down | $C000 - $DFFF |
| Down | Down | Down | $E000 - $FFFF |

NOTE: "Up" is toward the top edge of the Module.

## SPECIFICATIONS

| | |
|---|---|
| Memory Size: | 16K bytes |
| Word Length: | 8 bits |
| Interface: | SYSTEM 65 compatible |
| Max. Access Time: | 450 ns (P/N M65-031)<br>250 ns (P/N M65-032) |
| Module Components: | 32 R2114 Static 1024 x 4-bit RAM devices |
| Module Dimensions: | 9.75 in. wide x 6.00 in. high |
| Edge Connector: | 86 pins on 0.156-in. centers |
| Operating Temperature: | $0^{\circ}C$ to $+70^{\circ}C$ |
| Power Requirements: | +5 VDC ±5% @ 3.0 amps (typical) |

## LOGIC LEVELS

$T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = +5V \pm 5\%$

| Characteristic | Symbol | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| Inputs ($\overline{D0}$-$\overline{D7}$), A0-A15, WP1-WP7, Ø2, R/$\overline{W}$) | | | | | |
| Input Low Voltage | $V_{IL}$ | | 0.8 | V | $I_{IL} = 400\ \mu a$ |
| Input High Voltage | $V_{IH}$ | 2.0 | $V_{CC}$ | V | $I_{IH} = 40\ \mu a$ |
| Outputs ($\overline{D0}$-$\overline{D7}$) | | | | | |
| Output Low Voltage | $V_{OL}$ | | 0.5 | V | $I_{OL} = 48$ ma |
| Output High Voltage | $V_{OH}$ | 2.4 | $V_{CC}$ | V | $I_{OH} = 10$ ma |

DOCUMENT NO. 29650 N42
REV. 1, APRIL 1979

PART NUMBER
M65-040

Rockwell

# R6500 Microcomputer System PRODUCT DESCRIPTION



## PROM PROGRAMMER MODULE

### OVERVIEW

The PROM Programmer Module provides SYSTEM 65 users with a means to program, verify, read and check Programmable Read Only Memory (PROM) devices, and supports 2704, 2708, 2716, 2516, 2532 and 2758 devices. The PROM Programmer Module connects directly to the PROM Socket on the front panel of the SYSTEM 65 chassis, via supplied cable.

The Module is supplied with a mini-floppy diskette which holds a set of software routines that allow the user to check a PROM for proper initialization, program the PROM from SYSTEM 65 memory, verify the PROM with SYSTEM 65 memory, and read the contents of the PROM into memory. Utility functions to load, verify and dump memory are also supplied.

### FEATURES

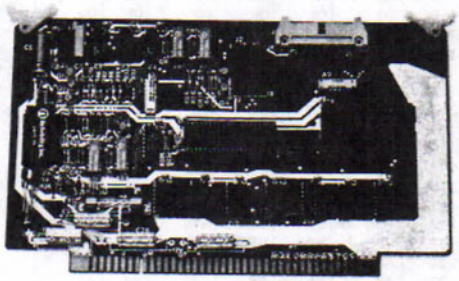
- SYSTEM 65 compatible
- Supports programming of 2704, 2708, 2516, 2532, 2716 (Intel and Texas Instruments) and 2758 PROM devices.
- Comes with software on mini-floppy diskette

### FUNCTIONAL DESCRIPTION

In reading the text to follow, refer to the Functional Block Diagram in Figure 1 and the attached schematic, PS00-X201. The edge connector pin assignments for the PROM Programmer Module are identical to the Motherboard pin assignments given in Section 4 of the SYSTEM 65 User's Manual (Document No. 29650 N35).

Table 1 summarizes the PROM Socket interface, and applies to both the PROM socket located on the PROM Programmer Module and the PROM socket located on the SYSTEM 65 front panel.

The PROM Programmer Module consists of two R6520 Peripheral Interface Adapters (PIAs), data buffers, address decoders, 26V power supply, level shifters and power-up circuitry.



The power-up circuitry (Z9) generates an automatic reset during power-up. A reset signal may also come from the Reset line of the SYSTEM 65 Bus.

The PROM Programmer Module contains data bus buffers, Z12 and Z13, to provide a logical inversion and a single TTL load to the SYSTEM 65 bus signals. The two R6520 PIAs, Z5 and Z8, are used to store the address, data and control information for the PROM device. The address, Read/Write ($R/\overline{W}$), and $\phi 2$ signals are buffered and decoded by Z10, Z11, Z14, Z15 and Z16. PIA No. 1 is addressed at locations $C018-$C01B. PIA No. 2 is addressed at locations $C01C-$C01F.

The PROM device receives address lines A0-A9 and data lines D0-D7 directly from the PIA devices. The program lines (see Table 1, PROM socket pin nos. 18, 19 and 20) are level-shifted to provide either 0V, +5V, +12V, +25V or +26V to the PROM device, depending on the device type. The 26-volt power is generated from the +5-volt power through a DC-DC converter, Z6, and an adjustable voltage regulator, Z1. Relays XR1 through XR4 are used to switch the power lines (see Table 1, PROM socket pin nos. 21 and 23) to +5V, +12V and -5V to the PROM device, depending on the device type. The -5V power is generated from the -12V power line through a voltage regulator, Q9.

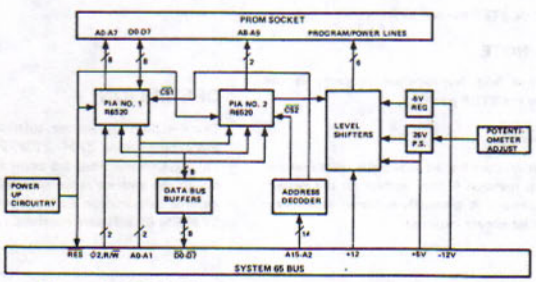



**Figure 1. PROM Programmer Functional Block Diagram**



Specifications subject to change without notice

Table 1. SYSTEM 65 PROM Socket Interface Summary

| PROM Socket Pin Number | PROM Device Type | | | | | | Connector J1 Pin Number |
|---|---|---|---|---|---|---|---|
| | 2532 | 2704 | 2708 | T.I. 2716 | 2758 | 2516 Intel 2716 | |
| 1 | A7 | A7 | A7 | A7 | A7 | A7 | 21 |
| 2 | A6 | A6 | A6 | A6 | A6 | A6 | 19 |
| 3 | A5 | A5 | A5 | A5 | A5 | A5 | 17 |
| 4 | A4 | A4 | A4 | A4 | A4 | A4 | 15 |
| 5 | A3 | A3 | A3 | A3 | A3 | A3 | 23 |
| 6 | A2 | A2 | A2 | A2 | A2 | A2 | 25 |
| 7 | A1 | A1 | A1 | A1 | A1 | A1 | 26 |
| 8 | A0 | A0 | A0 | A0 | A0 | A0 | 24 |
| 9 | D0 | D0 | D0 | D0 | D0 | D0 | 22 |
| 10 | D1 | D1 | D1 | D1 | D1 | D1 | 20 |
| 11 | D2 | D2 | D2 | D2 | D2 | D2 | 18 |
| 12 | GND | GND | GND | GND | GND | GND | 16 |
| 13 | D3 | D3 | D3 | D3 | D3 | D3 | 10 |
| 14 | D4 | D4 | D4 | D4 | D4 | D4 | 8 |
| 15 | D5 | D5 | D5 | D5 | D5 | D5 | 6 |
| 16 | D6 | D6 | D6 | D6 | D6 | D6 | 2 |
| 17 | D7 | D7 | D7 | D7 | D7 | D7 | 4 |
| 18 | A11 | PGM | PGM | PGM/$\overline{CS}$ | $\overline{CE}$ | $\overline{CS}$ | 13 |
| 19 | A10 | VDD | VDD | VDD | GND | A10 | 11 |
| 20 | PD/PGM | $\overline{CS}$/WE | $\overline{CS}$/WE | A10 | $\overline{OE}$ | PD/PGM | 9 |
| 21 | VPP | VBB | VBB | VBB | VPP | VPP | 7 |
| 22 | A9 | GND | A9 | A9 | A9 | A9 | 5 |
| 23 | A8 | A8 | A8 | A8 | A8 | A8 | 3 |
| 24 | VCC | VCC | VCC | VCC(PE) | VCC | VCC | 1 |

## MODULE INSTALLATION

Install the PROM Programmer Module as follows:

1. Turn SYSTEM 65 power off.

**CAUTION**

Never install or remove modules with SYSTEM 65 power on — it may cause damage to the module and/or to the System.

2. Remove the top cover of the SYSTEM 65.
3. Insert the PROM Programmer Module into any vacant slot in the SYSTEM 65 chassis.
4. Connect one end of the supplied cable to the connector on top of the PROM Programmer Module and the other end to the connector mounted on the inside front panel of SYSTEM 65. Observe the correct polarity of the plugs and sockets; i.e., align the arrows marked on the plugs and sockets.
5. Install the top cover of the SYSTEM 65.
6. Set the SYSTEM 65 RUN/STEP Switch to RUN.

**NOTE**

The PROM Programmer will not operate properly if the RUN/STEP Switch is in the STEP position.

7. Turn SYSTEM 65 power on.
8. The PROM Programmer Module has an automatic reset feature. The standard power-up message should appear on the system terminal device at power-on. A manually-initiated reset may, however, be performed whenever required.

## PROM DEVICE INSERTION/REMOVAL

**CAUTION**

The PROM device is fragile, and dropping, twisting or uneven pressure may break it. Never press down on the window area of the chip

The PROM device may be inserted into SYSTEM 65 front panel socket or into the socket located on the PROM Programmer Module.

**CAUTION**

Only one PROM device should be installed at a time — in either the SYSTEM 65 socket or the PROM Programmer Module socket. Programming with PROM devices installed in both locations may cause erroneous results and/or damage to the PROM.

### PROM INSERTION/REMOVAL ON THE SYSTEM 65 FRONT PANEL

To insert the PROM device:

1. Push the PROM socket lever out from the SYSTEM 65 front panel, to release pin pressure.
2. Position the PROM device in front of the socket, being careful to observe the Pin 1 location.

**CAUTION**

Incorrect PROM installation may cause PROM damage and/or may blow Fuses F1 and F2 on the PROM Programmer Module.

3. Insert the PROM into the socket, then push up and in on the socket lever to apply pressure to the pins.

To remove the PROM device, grasp the PROM device at each end, then push the socket lever away from the SYSTEM 65 front panel to release pin pressure.

### PROM INSERTION/REMOVAL ON PROM PROGRAMMER MODULE

To insert the PROM device, position the PROM device in front of the socket, being careful to observe the PIN 1 location.

**CAUTION**

Incorrect PROM installation may cause PROM damage and/or may blow Fuses F1 and F2 on the PROM Programmer Module.

With the PROM properly oriented, gently start all pins evenly into the socket pin guides. Then press firmly and evenly on the device (avoiding contact with the light window) until the device is securely seated.

To remove the PROM device, exert an even, upward force on both sides of the device while counteracting with a lesser, evenly-applied downward force. This will prevent the PROM device from popping out one side and bending or breaking pins still engaged at the other end of the socket.

## OPERATION

The PROM Programmer software allows checking, reading, verifying and programming 2704, 2708, 2758, 2516, 2532 or 2716 type devices. The data/instructions are copied to/from the SYSTEM 65 RAM memory in the address range specified by the user. The user can then transfer this information to/from the diskette (or other I/O device) using SYSTEM 65 software routines.

### LOADING THE PROM PROGRAMMER ROUTINES

There is one PROM programmer object file supplied on the PROM Programmer diskette, PROM*n, where "n" is the program release revision letter. File PROM*n occupies from $0200 to $0FFF. User programs can be loaded starting at $1000. To load the PROM*n program, use the SYSTEM 65 Load Command L. Then enter the file name (PROM*n) and disk drive number desired. Since the PROM*n program may occupy the same memory area in which user's data may reside, an offset may be applied to the user's data to locate it to $1000 or above (See Load, Verify and Dump functions with offset). PROM*n uses page 0 ($0080–$009A) and page 1 ($0100–$01FF).

#### NOTE

The SYSTEM 65 RUN/STEP switch must be in the Run position for PROM programming.

After the program is loaded, use the five (5) key to start the PROM Programmer routines for a 1 MHz system or the six (6) key for a 2 MHz system. The 5 (or 6) key may also be used for reentry into the PROM Programmer routines. Once the routines are entered, the only way to exit back to the SYSTEM 65 monitor is to press the ESC key, if the program is waiting for input, or the Reset switch.

The PROM Programmer PROGRAM PROM (P) and VERIFY PROM (V) functions require that the data to be programmed and/or verified be in RAM memory prior to execution. If the program data resides on diskette (or other media), use the SYSTEM 65 Monitor L command to load the object code into memory before entering the PROM programmer functions with key 5 (or 6). Alternatively, use the PROM Programmer L command to load the program data with optional offset after the PROM Programmer functions have been entered.

### PROM PROGRAMMER OPERATION

Before entering any of the PROM Programmer functions to follow, ensure that the required PROM device is installed in the desired PROM socket – the SYSTEM 65 front panel socket or the PROM Programmer Module's PROM socket – per the PROM Device Insertion/Removal instructions. The PROM Programmer functions may be entered in the absence of an installed PROM device, but this may cause verify errors.

#### CAUTIONS

1. Insert a PROM device only when SYSTEM 65 power is on and either the Monitor prompt (<) or the PROM Programmer prompt (=) is the last character displayed on the system terminal. Failure to do so may cause damage to the PROM device.
2. DC power to the PROM device installed in the PROM socket is set to zero upon SYSTEM 65 power-up or depression of the Reset switch. During a PROM Programmer function, DC power is supplied to the PROM socket after entry of the last address, then the commanded PROM programming function is performed. The DC power is removed upon completion of the programming function, before the next PROM Programmer prompt character (=) is displayed.

Once started, the routines will ask the user for certain information. This information should be entered on the system terminal. For numbers or addresses, type in the number followed by a space or carriage return to terminate the number. Leading zeros are not necessary. Only the last four digits of the number are used. If a mistake is made before pressing the space bar or carriage return, reenter the correct number (all four digits). If a mistake is made after entering a number, exit the PROM Programmer routines using the ESC key or Reset switch on the front panel and restart with key 5 (or 6). If an invalid command or number is entered the routines will print WHAT? and ask you to reenter.

Figure 2 is an example of a PROM Programmer load and initialization along with the user's response.

Next, the data to be copied to the PROM device can be loaded using the L command. In this example, the file USERIN was loaded. Type 5 (or 6) to start the routines. Next, enter the device type. If a 2716 was entered, the message TMS 2716 (Texas Instruments) PROM? will be printed. Enter Y for yes or N for no. The routines will reprint the device type for verification each time a new function is requested. A single character should now be entered to indicate the function requested as outlined in the subsequent text.

```
<L>IN=F  FILE=PROM*C   DISK=1
<5>PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER C)

ENTER 2704,2708,2758,2716,2516, OR 2532
=2716
TMS 2716 PROM?
=Y

**********
DEVICE TYPE=
2716
**********

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=
```

**Figure 2. Power-Up and Loading Responses**

### ADDRESS SELECTION

The addresses entered are the hexadecimal locations of the RAM memory used for checking, programming, reading, or verifying. The upper address bits are then stripped off to form the address for the PROM devices. In general, the addresses must comply with the following restrictions:

1. Cannot be Page 0 ($0000–$00FF) or Page 1 ($0100–$01FF).
2. Cannot overlap the PROM Programmer routine for file name PROM*n ($0200–$0FFF).
3. The last address must be greater than or equal to the first address entered.
4. The address range from first to last must not exceed the size of the PROM being programmed.

In addition, there are further restrictions on certain PROM devices, imposed by the PROM manufacturer. The 2704, 2708, and TI TMS-2716 must be programmed using their total address space during one programming. This means that the 2704, 2708, and TI TMS2716 must start on a 1/2K, 1K or 2K address boundary, respectively. They also have to extend 1/2K, 1K or 2K bytes in length, respectively. The 2516, 2532, 2758 and Intel 2716 do not have this requirement. Therefore, single byte or multi-bytes may be programmed within the address range of the device. The routines are designed to check for any invalid address entered and will print WHAT? and ask for the address again.

### PROGRAM FUNCTION (THE P COMMAND)

The Program Function (P) loads the contents of SYSTEM 65 memory into PROM. It is entered by pressing the P key in response to the ENTER command message. The routines will ask where any errors detected during verifying should be printed. This is indicated by the message ERROR LIST OUT=. Enter any of the standard I/O device characters (space for CRT, P for Printer, etc.).

After the first and last address is entered, the routines will check to see if the PROM is initialized. Since these PROMs are initialized to an all-ones condition by placing them under an ultraviolet light, a check is made prior to programming for an all-one's condition. If any zero is detected in the bounds of the address range entered, the messages PROM NOT INITIALIZED and CONTINUE Y or N will be printed. The user has the option of aborting the programming (type N for no) and initializing the PROM properly or continuing with the programming by typing the Y (yes) key.

It is possible to change a 1 to 0 with the PROM programmer, but the PROM must be exposed to an ultraviolet light to set the bits back to one's according to the respective manufacturer's specifications. If the PROM is initialized or "Y" entered, a star will be printed every 1-5 seconds, indicating programming in progress. After programming, the message VERIFYING will be printed and the PROM device will be verified against the specified RAM locations. This is automatically done every time. If there are no errors detected, the message DONE will be printed and the next operation requested. Any errors detected will be printed on the selected I/O device.

Figure 3 shows an example of the Program Function.

### NOTES

1. A verification error showing a series of 1's in a specific PROM bit position after programming may indicate a poor connector contact caused by improper PROM installation in the PROM socket. See the PROM Device Insertion/Removal instructions.
2. If fuse F1 or F2 on the PROM Programmer Module is blown, the PROM may not verify correctly. Verify that both are good if a verify error occurs.

```
<5>PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER C)

ENTER 2704,2708,2758,2716,2516, OR 2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=P
PROGRAM
ERROR LIST
OUT=
ENTER FIRST ADDRESS
=1000
ENTER LAST ADDRESS
=17FF
**********************************************************************
DONE
VERIFYING

DONE

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=
```

**Figure 3. Program Function Example**

### VERIFY FUNCTION (THE V COMMAND)

The Verify Function (V) verifies the contents of the PROM with the contents of SYSTEM 65 RAM. It is entered by pressing the V key in response to the ENTER command message.

The routines will request where any errors detected should be printed. This is indicated by the message ERROR LIST OUT=. Enter any of the standard I/O device characters defined in the SYSTEM 65 User's Manual (space for CRT, P for Printer, etc.). Next, type in the first and last addresses. As soon as the last address is entered, power will be applied to the PROM device and the contents of the PROM compared to the respective content of the RAM. If no errors are found, the message DONE will be printed, and the next operation requested. If errors are detected, the address, contents of PROM, and contents of RAM in disagreement will be displayed/printed on the selected I/O device. Figure 4 shows an example of the Verify Function with errors.

```
<5>PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER C)

ENTER 2704,2708,2758,2716,2516, OR 2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=V
VERIFY
ERROR LIST
OUT=
ENTER FIRST ADDRESS
=1000
ENTER LAST ADDRESS
=17FF
ERROR
ADDR PROM RAM
1000  4C   11
1400  49   22
17FF  15   33

DONE

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=
```

**Figure 4. Verify Function Example with Errors**

### READ FUNCTION (THE R COMMAND)

The Read Function (R) reads the contents of PROM into SYSTEM 65. RAM. It is entered by pressing the R key in response to the ENTER command message.

After the first and last addresses are entered, power will be applied to the PROM and the contents copied into the specified RAM locations. When completed, the message DONE will be printed and the next operation requested. Figure 5 shows an example of a Read Function.

The PROM Programmer READ function reads program data into SYSTEM 65 RAM memory from PROM. After reading is complete, save the PROM data on diskette (or other media) using the SYSTEM 65 Monitor D Command after exiting the PROM Programmer functions. Alternatively, use the PROM Programmer D command to dump the data with optional offset before the PROM Programmer functions are exited. The amount to be stored or loaded at one time is limited only by the RAM locations available.

```
<5>PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER C)

ENTER 2704,2708,2758,2716,2516, OR 2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=R
READ
ENTER FIRST ADDRESS
=1000
ENTER LAST ADDRESS
=17FF

DONE

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=
```

**Figure 5. Read Function Example**

### CHECK FUNCTION (THE C COMMAND)

The Check Function (C) is used to check that the PROM is initialized. It is entered by pressing the C key in response to the ENTER command message.

After the first and last addresses are entered, power is applied to the device and all specified locations are checked for $FF. The message PROM NOT INITIALIZED will be printed if all locations do not contain $FF. The message DONE will be printed when the Check Function is complete.

Figure 6 is an example of a successful Check Function.

```
<5>PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER C)

ENTER 2704,2708,2758,2716,2516, OR 2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=C
CHECK
ENTER FIRST ADDRESS
=1000
ENTER LAST ADDRESS
=17FF
PROM NOT INITIALIZED

DONE

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=
```

**Figure 6. Check Function Example**

### LOAD MEMORY WITH OFFSET FUNCTION (THE L COMMAND)

The Load Memory with Offset Function (L) copies data from an input object code file into memory addresses offset by an entered amount from the addresses on the input file. The entered offset value is additive with carry from bit 15 ignored, e.g.;

| Input File Address | Offset Value | Address in Memory |
|---|---|---|
| $1000 | 0 | $1000 |
| $1000 | $2000 | $3000 |
| $7000 | $A000 | $1000 |
| $E000 | $2000 | $1000 |

Figure 7 is an example of the Load Memory with Offset Function.

```
<5>PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER C)

ENTER 2704,2708,2758,2716,2516, OR 2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=L
LOAD
OFFSET=D000 IN=F  FILE=AIMBAS   DISK=2

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=
```

**Figure 7. Load Memory with Offset Function Example**

### VERIFY MEMORY WITH OFFSET FUNCTION (THE F COMMAND)

The Verify Memory with Offset Function (F) compares the contents of an object code file with the contents of memory at addresses in memory offset by an entered amount from the addresses on the reference object code file. The entered offset is additive in the same manner as the Load with Offset function. The contents of both memory (MEM) and reference file (FILE) are displayed/printed along with the address (ADDR) if any differences in value are detected.

Figure 8 is an example of the Verify Memory with Offset Function showing two detected errors.

```
<5>PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER C)

ENTER 2704,2708,2758,2716,2516, OR 2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=F
VERIFY
OFFSET=D000 IN=F  FILE=AIMBAS  DISK=2
ERROR LIST
OUT=
ADDR/MEM/FILE
1000 56 4C  13F0 76 E8

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=
```

**Figure 8. Verify Memory with Offset Function Example with Errors**

### DUMP MEMORY WITH OFFSET FUNCTION (THE D COMMAND)

The Dump Memory with Offset Function (D) copies data from memory to an output object code file with addresses in the output file offset an entered amount from the addresses in memory. The entered offset value is additive from the output file to memory with carry from bit 15 ignored; e.g.:

| Output File Address (FROM=) | Offset Value | Address in Memory |
|---|---|---|
| $1000 | 0 | $1000 |
| $4000 | $D000 | $1000 |
| $1000 | $8000 | $9000 |
| $A000 | $1000 | $B000 |

Figure 9 is an example of the Dump Memory with Offset Function.

```
<5>PROM PROGRAMMER FOR 1 MHZ SYSTEM (VER C)

ENTER 2704,2708,2758,2716,2516, OR 2532
=2716
TMS 2716 PROM?
=N

**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=D
DUMP
OFFSET=D000 OUT=F  FILE=PRMOUT  DISK=2
FROM=4000TO=47FF

MORE?N
**********************
DEVICE TYPE=
2716
**********************

ENTER PROM COMMAND: VERIFY(V),PROGRAM(P),READ(R),OR CHECK(C)
 OR MEMORY COMMAND: VERIFY(F),LOAD(L),OR DUMP(D)
=
```

**Figure 9. Dump Memory with Offset Function Example**

## SPECIFICATIONS

| | |
|---|---|
| PROM Devices Supported: | 2704, 2708, 2758, Intel 2716 and Texas Instruments 2716 |
| Programming Time (approximately): | 2704 – 100 sec.<br>2708 – 200 sec.<br>2758 – 60 sec.<br>Intel 2716 – 120 sec.<br>T.I. 2716 – 400 sec.<br>2516 – 120 sec.<br>2532 – 240 sec. |
| Interface: | SYSTEM 65 compatible |
| Module Dimensions: | 9.75 in. wide x 6.00 in. high |
| Edge Connector: | 86 pins on 0.156-in. centers |
| Operating Temperature: | $0^{o}$ to + $70^{o}$C |
| Power Requirements: | +5 VDC ± 5% @ 750 ma (fused at 2 amps)<br>+12 VDC ± 5% @ 50 ma (fused at ½ amp)<br>-12 VDC ± 5% @ 50 ma. |
| Fuse Description: | F1 – AGC ½A–250V (Bussman)<br>F2 – AGC 2A–250V (Bussman) |

DOCUMENT NO. 29650 N47
AUGUST 1978

PART NUMBER
M65-045

Rockwell

# R6500 Microcomputer System
# PRODUCT DESCRIPTION





## PROM/ROM MODULE

### OVERVIEW

The PROM/ROM Module (Part Number M65-045) permits system read only memory to be increased by up to 16K bytes. The Module provides 16 24-pin DIP sockets for accepting industry-standard 2708, 2716 or 2758 PROM devices, or 2316 or 2332 ROM devices. PROMs and ROMs cannot be mixed on the Module.

The PROM/ROM Module's 16K-byte address space is segmented into four independent 4K-byte sections. Each 4K-byte section is provided with a switch for selecting its base address. Further, each socket has an individual enable/disable switch, providing resolution down to 1K bytes.

### FEATURES

- SYSTEM 65 compatible
- 16K-byte read only memory capacity
- Accepts 2708, 2716 or 2758 PROM devices
- Accepts 2316 or 2332 ROM devices
- Sockets can be individually enabled/disabled
- Base address is switch-selectable for each 4K-byte address space
- Single +5V supply

### FUNCTIONAL DESCRIPTION

In reading the text to follow, refer to the Functional Block Diagram below and the attached schematics:

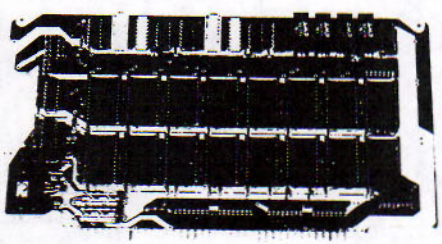
- PS00-X-141, the -001 version of the PROM/ROM Module
- PS00-X-143, the -011 version of the PROM/ROM Module

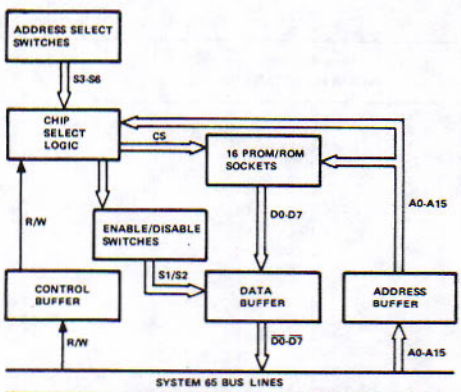
The edge connector pin assignments for the PROM/ROM Module are identical to the Motherboard pin assignments given in Section 4 of the SYSTEM 65 User's Manual (Document No. 29650 N35).

The PROM/ROM Module comes with 16 sockets for accepting the following types of memory devices:

- Up to four 2332 ROMs, or
- Up to eight 2316 ROMs, or
- Up to eight 2716 PROMs, or
- Up to 16 2708 or 2758 PROMs

The address switches on the Module are set in accordance with the type and number of PROM or ROM devices installed. Each socket may also be selected by a switch. Further, each 4K address space also has a separate switch for selection of its base address. The Chip Select Logic specifies the PROM/ROM to be accessed and the address lines from the System bus select the memory location. The selected PROM/ROM device responds by placing 8 bits of data on the data lines ($\overline{D0}$ through $\overline{D7}$) for transfer to the CPU.






PROM/ROM Module Functional Block Diagram

## SWITCHES AND JUMPERS

The PROM/ROM Module can accommodate a variety of standard PROM and ROM devices. The user must configure the Module for his specific application, and does so with various switches and jumpers on the Module itself.

The PROM/ROM Module has a total address space of 16K bytes, divided into four 4K-byte sections. Each 4K section has a separate base address select switch, S3 through S6, which must be set to the desired hexadecimal value (0 - F). For example, if Switch S3 is set to C, the base address for Sockets Z4, Z5, Z6 and Z7 is $C000 (where $ indicates hexadecimal). Further, each individual socket can be enabled or disabled from driving the Data Bus by setting/resetting Switches S1 and S2.

There is a further restriction for ROMs: Since ROMs have chip selects, they will only work in the proper sockets with proper base address switch settings. For example, a 2316 ROM with CS3=1, CS2=0 and CS1=1 will work only in Socket Z22 (see Table 4) and with a selected base address value of 2, 6, A or E.

As mentioned above, the PROM/ROM Module must also be jumper-configured for the device being used. Jumper information is given with switch select tables. The function of each jumper is summarized in Table 1.

**Table 1. PROM/ROM Board Jumper Functions**

| Jumper No. | Jumper Function |
|---|---|
| 1 | Connects A12 to Pin 18 of all sockets |
| 2 | Enables 1K address selection |
| 3 | Connects +12VDC to Pin 19 of all sockets |
| 4 | Enables 2K address selection |
| 5 | Connects A13 to Pin 21 of all sockets |
| 6 | Connects A10 to Pin 19 of all sockets |
| 7 | Connects A11 to Pin 21 of all sockets |
| 8 | Connects +5VDC to Pin 21 of all sockets |
| 9 | Connects A11 to Pin 18 of all sockets |
| 10 | Connects -5VDC to Pin 21 of all sockets |
| 11 | Connects GND to Pin 18 of all sockets |
| 12 | Enables active low chip selects on Sockets Z7, Z14, Z22 and Z29 |

**Table 2. Switch Settings for 2716 PROM Operation**

| Base Address (A15, A14, A13, A12) | Address A11 | Socket | Enable/Disable Switch |
|---|---|---|---|
| S3 (0-F) | 0 | Z5 | S1-2 |
| | 1 | Z7 | S1-4 |
| S4 (0-F) | 0 | Z11 | S1-6 |
| | 1 | Z14 | S1-8 |
| S5 (0-F) | 0 | Z18 | S2-2 |
| | 1 | Z22 | S2-4 |
| S6 (0-F) | 0 | Z24 | S2-6 |
| | 1 | Z29 | S2-8 |

**For 2716 PROMs,** add Jumpers 4, 6, 8, 11 and 12.

**Table 3. Switch Settings for 2708 or 2758 PROM Operations**

| Base Address (A15, A14, A13, A12) | Address A11 A10 | Socket | Enable/Disable Switch |
|---|---|---|---|
| S3 (0-F) | 0 0 | Z4 | S1-1 |
| | 0 1 | Z5 | S1-2 |
| | 1 0 | Z6 | S1-3 |
| | 1 1 | Z7 | S1-4 |
| S4 (0-F) | 0 0 | Z10 | S1-5 |
| | 0 1 | Z11 | S1-6 |
| | 1 0 | Z13 | S1-7 |
| | 1 1 | Z14 | S1-8 |
| S5 (0-F) | 0 0 | Z17 | S2-1 |
| | 0 1 | Z18 | S2-2 |
| | 1 0 | Z21 | S2-3 |
| | 1 1 | Z22 | S2-4 |
| S6 (0-F) | 0 0 | Z23 | S2-5 |
| | 0 1 | Z24 | S2-6 |
| | 1 0 | Z28 | S2-7 |
| | 1 1 | Z29 | S2-8 |

**For 2708 PROMs,** add Jumpers 2, 3, 4, 11 and 12 **and** add Capacitors C6-C9, C14-C17, C21-C24, C29-C32, C37-C40, C45-C48, C52-C55 and C59-C62. All capacitors are 0.1 μf.

**For 2758 PROMs,** add Jumpers 2, 8, 11 and 12 **and** jumper left post of Jumper 3 to right post of Jumper 4.

Table 4. Switch Settings for 2316 ROM Operation

| Base Address (A15, A14, A13, A12) | ROM Chip Selects* A13 CS3 | A12 CS2 | A11 CS1 | Socket | Enable/Disable Switch |
|---|---|---|---|---|---|
| S3 (0, 4, 8, C) | 0 | 0 | 0 | Z5 | S1-2 |
| | 0 | 0 | 1 | Z7 | S1-4 |
| S4 (1, 5, 9, D) | 0 | 1 | 0 | Z11 | S1-6 |
| | 0 | 1 | 1 | Z14 | S1-8 |
| S5 (2, 6, A, E) | 1 | 0 | 0 | Z18 | S2-2 |
| | 1 | 0 | 1 | Z22 | S2-4 |
| S6 (3, 7, B, F) | 1 | 1 | 0 | Z24 | S2-6 |
| | 1 | 1 | 1 | Z29 | S2-8 |

*Assumes CS1=A11, CS2=A12 and CS3=A13

**For 2316 ROMs**, add Jumpers 1, 4, 5 and 6

Table 5. Switch Settings for 2332 ROM Operation

| Base Address (A15, A14, A13, A12) | ROM Chip Selects* A13 S2 | A12 S1 | Socket | Enable/Disable Switch |
|---|---|---|---|---|
| S3 (0, 4, 8, C) | 0 | 0 | Z7 | S1-4 |
| S4 (1, 5, 9, D) | 0 | 1 | Z14 | S1-8 |
| S5 (2, 6, A, E) | 1 | 0 | Z22 | S2-4 |
| S6 (3, 7, B, F) | 1 | 1 | Z29 | S2-8 |

*Assumes S1=A12 and S2=A13

**For 2332 ROMs**, add Jumpers 2, 5, 6 and 9

## INSTALLATION

The procedure below should be used to install PROM/ROM Modules in the SYSTEM 65 chassis or, with appropriate changes, in an Auxiliary Card Cage.

1. Turn SYSTEM 65 power off.

**CAUTION**

Never install or remove modules with SYSTEM 65 power on — it may cause damage to the module and/or to the System.

2. Remove the top copver of the SYSTEM 65.
3. Set the switches on the PROM/ROM module per Tables 2 through 5. The base memory addresses are assigned by four hexadecimal switches, S3 through S6. Individual sockets are enabled/disabled by Switches S1 and S2.
4. Install the required jumpers per directions given with the switch table.
5. Install the required PROM or ROM devices in their appropriate sockets.
6. Insert the PROM/ROM Module(s) into any vacant slot(s) in the SYSTEM 65 chassis. .
7. Install the top cover of the SYSTEM 65.
8. Turn SYSTEM 65 power on.

## SPECIFICATIONS

| | |
|---|---|
| Memory Capacity: | 16K bytes |
| Word Length: | 8 bits |
| Interface: | SYSTEM 65 compatible |
| Module Components: | 16 24-pin DIP sockets |
| Module Dimensions: | 9.75 in. wide x 6.00 in. high |
| Edge Connector: | 86 pins on 0.156-in. centers |
| Operating Temperature: | $0^{\circ}C$ to $+70^{\circ}C$ |
| Power Requirements: | +5 VDC + 5% @ 500 ma. with no devices installed |

## LOGIC LEVELS

$T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = +5V + 5\%$

| Characteristic | Symbol | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| Inputs ($\overline{D0}$-$\overline{D7}$, A0-A15, $\phi 2$, R/$\overline{W}$) | | | | | |
| Input Low Voltage | $V_{IL}$ | | 0.8 | V | $I_{IL} = 400\ \mu a$ |
| Input High Voltage | $V_{IH}$ | 2.0 | $V_{CC}$ | V | $I_{IH} = 40\ \mu a$ |
| Outputs ($\overline{D0}$-$\overline{D7}$) | | | | | |
| Output Low Voltage | $V_{OL}$ | | 0.5 | V | $I_{OL} = 48$ ma |
| Output High Voltage | $V_{OH}$ | 2.4 | $V_{CC}$ | V | $I_{OH} = 10$ ma |

DOCUMENT NO. 29650 N41
AUGUST 1978

PART NUMBER
M65-060

Rockwell

# R6500 Microcomputer System
# PRODUCT DESCRIPTION



## EXTENDER CARD

### OVERVIEW

The Extender Card is used to provide easy access to a printed circuit module installed in its system enclosure, for signal tracing or troubleshooting. In that context, the Extender Card consists of a series of bus lines connecting the Card's standard contact edge, on one end, and a connector used for accepting the standard contact edge of an 86-pin system module.

This contact edge and the edge connector pins are connected pin-for-pin via the bus lines on the Card. Each of the bus lines is provided with a clip-on terminal to allow test equipment to be readily connected. With the module under test connected to the Extender Card and this assembly installed in the system's Auxiliary Card Cage or SYSTEM 65 chassis, the user is given free access to both sides of the module being tested.

The edge connector pin assignments for the SYSTEM 65 Motherboard are given in Section 4 of the SYSTEM 65 User's Manual (Document No. 29650 N35).

### SPECIFICATIONS

| | |
|---|---|
| Edge Contacts: | 86 pins on 0.156-in. centers |
| Edge Connector: | 86 pins on 0.156-in. centers |
| Extender Card Dimensions: | 9.75 in. wide x 9.00 in. high x 0.062 in. thick |

### INSTALLATION

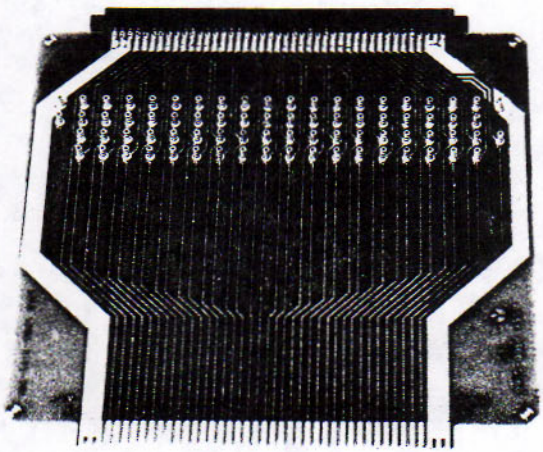
The procedure below should be used to install an Extender Card in the SYSTEM 65 chassis or, with appropriate changes, in an Auxiliary Card Cage.

1. Turn SYSTEM 65 power off.

**CAUTION**

Never install or remove modules with SYSTEM 65 power on — it may cause damage to the module and/or to the System.

2. Remove the top cover of the SYSTEM 65.
3. Remove the desired circuit module from SYSTEM 65, if installed.
4. Insert the Extender Card into any vacant slot in the SYSTEM 65 chassis.
5. Insert the desired circuit module into the plug on top of the Extender Card.
6. Turn SYSTEM 65 power on.



DOCUMENT NO. 29650 N45
AUGUST 1978

PART NUMBER
M65-070

Rockwell

# R6500 Microcomputer System
# PRODUCTION DESCRIPTION





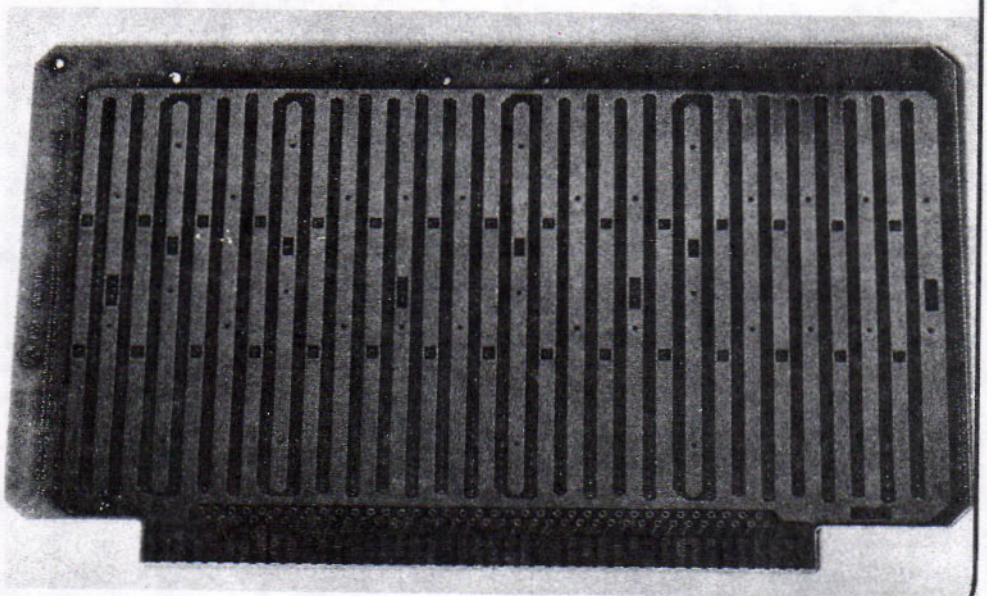
## DESIGN PROTOTYPING MODULE

### OVERVIEW

The Designing Prototyping Module (Part Number M65-070) allows development of custom circuits for installation in either Rockwell's SYSTEM 65 Microcomputer Development System or in user-designed equipment, via the Auxiliary Card Cage.

This Module is a SYSTEM 65-compatible printed circuit module with no mounted components, but with pre-routed power bus and power return lines. Spaced beside the power lines are plated-through holes that permit wire-wrap sockets to be installed. Additional holes, at the top edge of the Module, permit two 50-pin wire-wrap flat ribbon cable connectors to be installed.

The pin assignments for the Design Prototyping Module's 86-pin edge connector are identical to the Motherboard pin assignments given in Section 4 of the SYSTEM 65 User's Manual (Document No. 29650 N35).



## INSTALLATION

The procedure below should be used to install a Design Prototyping Module in the SYSTEM 65 or, with appropriate changes, in an Auxiliary Card Cage.

1. Turn SYSTEM 65 power off.

**CAUTION**

Never install or remove modules with SYSTEM 65 power on – it may cause damage to the module and/or to the System.

2. Remove the top cover of the SYSTEM 65.
3. Insert the Design Prototyping Module into any vacant slot in the SYSTEM 65 chassis.

**CAUTION**

Installation of improperly-operating circuits may cause malfunction and/or damage to the SYSTEM 65.

4. Install the top cover of the SYSTEM 65.
5. Turn SYSTEM 65 power on.

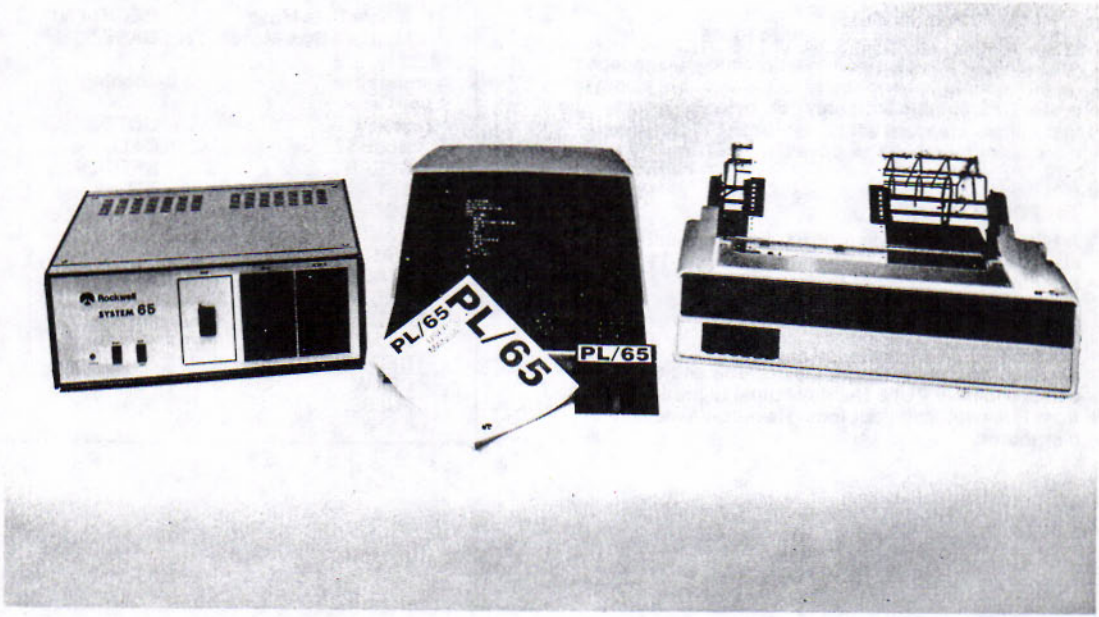
## SPECIFICATIONS

| | |
|---|---|
| Component Mounting Area: | |
| Number of Component Rows: | 15 |
| Number of Hole Rows: | 30 |
| Vertical Hole Spacing: | 45 holes on 0.1-in. centers |
| Horizontal Hole Spacing: | 30 holes on 0.3-in. centers |
| Flat Ribbon Connector Mounting Area: | |
| Number of Connector Areas: | 2 |
| Number of Pins Per Connector: | 50 |
| Module Dimensions: | 7.50 in. high x 9.75 in. wide x 0.062 in. thick |
| Edge Connector: | 86 pins on 0.156-in. centers |

## Now Rockwell Cuts The Low-Cost of R6500 Designing . . .

Rockwell

# PL/65
# A High-Level Language for the R6500 Microprocessor Family




In Rockwell's SYSTEM 65, you have one of the industry's most cost-effective microcomputer development systems. By coupling SYSTEM 65 with the advanced low-cost PL/65 Compiler option, you're even further ahead with valuable savings in time, effort and cost.

Resembling PL/1 and ALGOL in general form, PL/65 is designed to improve your productivity and efficiency by simplifying the overall software development effort.

The coding is easier, since PL/65's powerful, high level language statements enable you to implement even complex applications with minimal programming.

Program readability is enhanced by the self-documenting nature of PL/65. This results in programs that are easier to understand. These programs are easier to update, too, which means lower maintenance costs.

Rockwell International

### PL/65 = Software Simplification

All language features are aimed at improving productivity by simplifying software development. PL/65's structured programming support features encourage modular program design, and its general control structure for conditional and iterative looping allows the language to be applied to highly structured programs.

### Coding Flexibility . . . When You Need It Most

PL/65 allows you to freely mix assembly language instructions in portions of the program where timing or code optimization requirements are critical.

This flexibility carries through the compile cycle: The PL/65 compiler outputs source code to SYSTEM 65's resident assembler, rather than object code. You'll be able to enhance or debug at the assembler level and indeed to drop into assembly language whenever you desire — a big plus in structured programming. PL/65 thereby provides the structuring potential and programming simplicity of a high-level language, while retaining the power and flexibility of an assembler.

### No "Hidden" Memory Costs With PL/65

And while other microcomputer high-level languages require adding more memory to the host development system, PL/65 runs with only 16K bytes of RAM — and that comes **standard** with every SYSTEM 65 as do the dual minifloppy disk drives.

### For PDP 11 Users

A PL/65 Compiler and an R6500 cross-assembler are also available for installation using the RT-11 operating system.

### The PL/65 Package

A pre-programmed minifloppy diskette and the comprehensive PL/65 User's Manual is available now from Rockwell and your local Hamilton/Avnet distributor.

For more information on PL/65, SYSTEM 65, AIM 65, or the rapidly growing family of R6500 products, contact

ROCKWELL INTERNATIONAL
Microelectronic Devices
P.O. Box 3669
Anaheim, CA 92803
Attn: Marketing Services
D/727 RC55

or phone 714/632-3729.

**PL/65 LANGUAGE STATEMENTS**

**Declaration**

DECLARE
DEFINE
DATA
Comment

**Assignment**

Single-Byte Move
Multiple-Byte Move

**Imperative**

SHIFT
ROTATE
CLEAR
SET
CODE
HALT
WAIT
STACK
UNSTACK
INC
INCW
DEC
DECW
PULSE

**Specification**

ENTRY
EXIT

**Conditional**

IF-THEN-ELSE
IF-THEN
BEGIN-END
CASE

**Branching**

GOTO
CALL
RETURN
RTI
BREAK

**Looping**

FOR-TO-BY
WHILE

# RAM
## Memory Devices

NMOS
MEMORY
PRODUCTS

DOCUMENT NO. 29000 D44
REVISION 2, OCT. 1978

PART NUMBER
**R2114**

Rockwell

# R6500 Microcomputer System
# DATA SHEET

# 1024 X 4 STATIC RANDOM ACCESS MEMORY

## SYSTEM ABSTRACT

The 8-bit R6500 microcomputer system is produced with N-Channel, Silicon-Gate technology. Its performance speeds are enhanced by advanced system architecture. Its innovative architecture results in smaller chips – the semiconductor threshold to cost-effectivity. System cost-effectivity is further enhanced by providing a family of software-compatible microprocessor memory, and I/O devices. . .as well as low-cost design aids and documentation.

## FEATURES

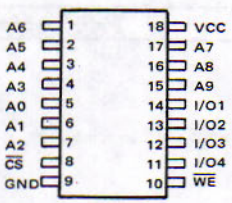
- 450 ns Maximum Access
- Low Operating Power Dissipation 0.1 mW/Bit Typical
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible:
  All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package

## DESCRIPTION

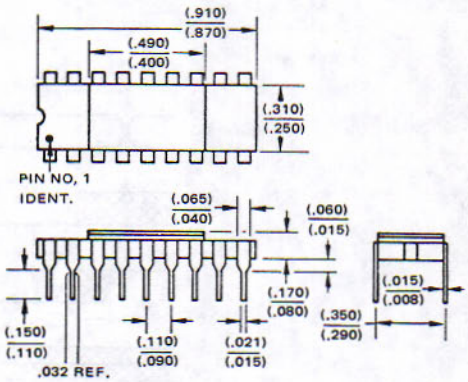
The R2114 is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clocks or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of bus oriented systems, and can drive 2 standard TTL loads.

The R2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select ($\overline{CS}$) input allows easy selection of an individual device when outputs are or-tied.

The R2114 is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel Ion Implanted, Silicon-Gate technology – a technology providing excellent performance characteristics as well as protection against contamination allowing the use of low cost packaging techniques.




**Pin Configuration**




**Package Dimensions**

**Ordering Information**

| Order Number | Package Type | Access Time | Temperature Range |
|---|---|---|---|
| R2114C | Ceramic | 450 nsec | 0°C to +70°C |
| R2114P | Plastic | 450 nsec | 0°C to +70°C |



Specifications subject to change without notice

## DATA STORAGE

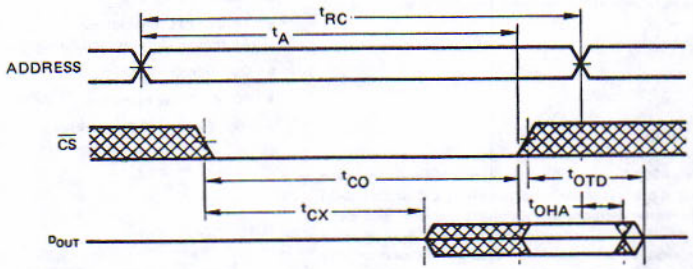
When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from being written into the array. As long as $\overline{WE}$ remains high, the data stored cannot be affected by the Address, Chip Select, or Data I/O logic levels or timing transitions.

Data storage also cannot be affected by $\overline{WE}$, Addresses, or the I/O ports as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ or both can prevent extraneous writing due to signal transitions.

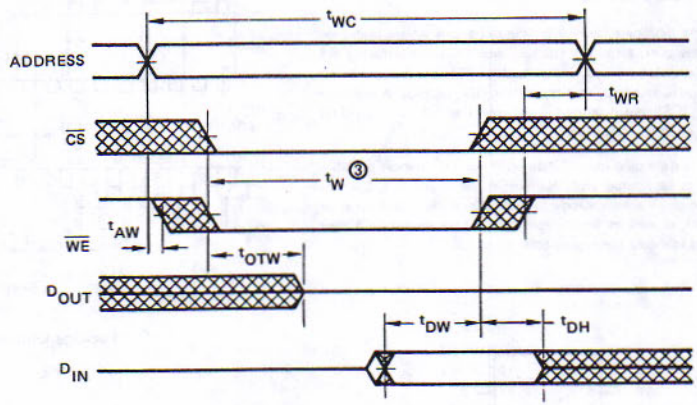
Data within the array can only be changed during Write time – defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. The addresses must be properly established during the entire Write time plus $t_{WR}$.

Internal delays are such that address decoding propagates ahead of data inputs and therefore no address setup time is required. If the Write time precedes the addresses, the data in previously addressed locations, or some other location, may be changed. Addresses must remain stable for the entire Write cycle but the Data Inputs may change in the beginning of the cycle. The data which is stable for $t_{DH}$ at the end of the Write time will be written into the addressed location.

**Read Cycle** ②




**Write Cycle**




**Notes:**

② $\overline{WE}$ is high for a Read Cycle

③ $t_W$ is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

**Timing Diagrams**

## SPECIFICATIONS

### Absolute Maximum Ratings

| | |
|---|---|
| Temperature Under Bias | -10°C to 80°C |
| Storage Temperature | -65°C to 150°C |
| Voltage on Any Pin with Respect to Ground | -0.5V to +7V |
| Power Dissipation | 1.0W |

### Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### Electrical Characteristics

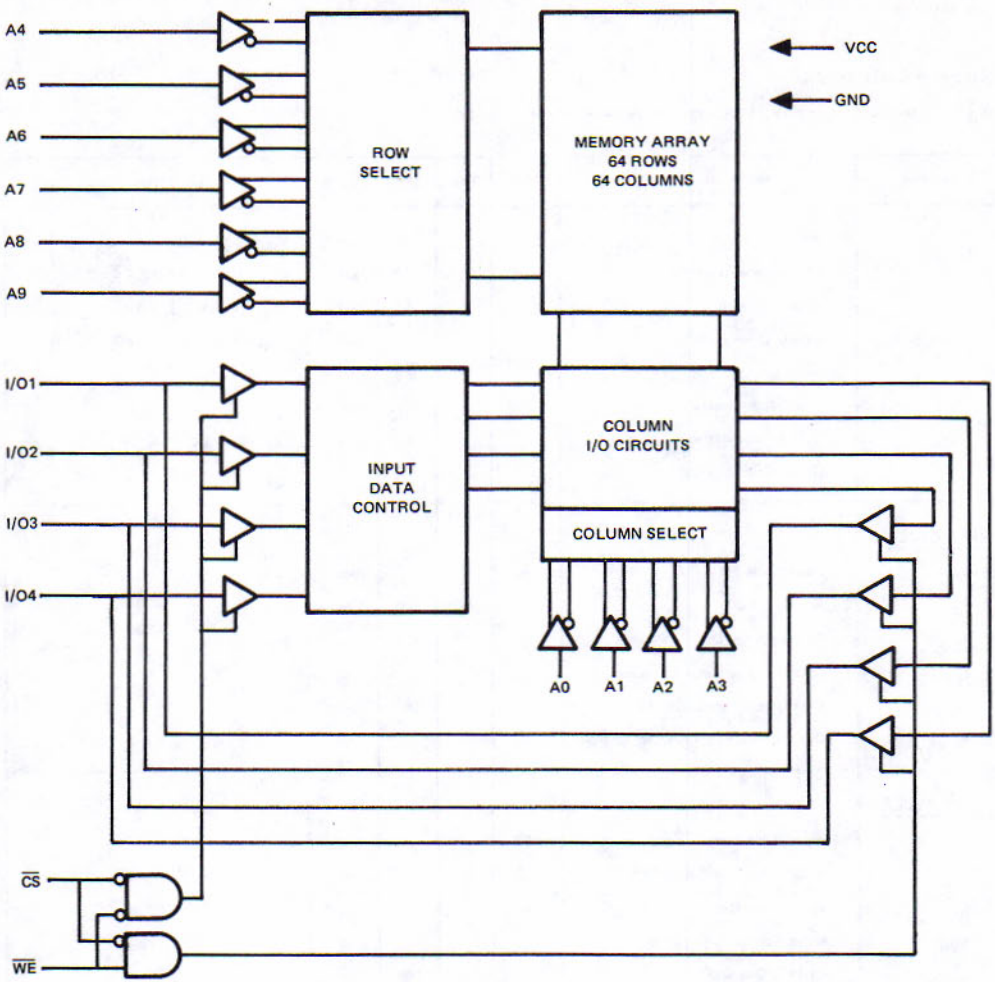
$T_A$ = 0°C to +70°C, $V_{CC}$ = 5V ±5% (Unless Otherwise Specified)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| ILI | Input Current | | | 10 | µA | $V_{IN}$ = 0 to +5.25V |
| ILO | I/O Leakage Current | | | 10 | µA | $V_{IO}$ = 0.45V to 4.0V, $\overline{CE}$ = 2.0V |
| ICC1 | Supply Current | | 80 | | mA | $V_{CC}$ = 4.75V, $I_{IO}$ = 0 mA, $T_A$ = 25°C |
| ICC2 | Supply Current | | | | mA | $V_{CC}$ = 4.75V, $I_{IO}$ = 0 mA, $T_A$ = 0°C |
| VIL | Input Low Voltage | -0.5 | | 0.8 | V | |
| VIH | Input High Voltage | 2.0 | | $V_{CC}$ | V | |
| VOL | Output Low Voltage | | | 0.4 | V | $I_{OL}$ = 3.2 mA |
| VOH | Output High Voltage | 2.4 | | | | $I_{OH}$ = -1.0 mA |
| READ CYCLE | | | | | | |
| $t_{RC}$ | Read Cycle Time | 450 | | | ns | |
| $t_A$ | Access Time | | | 450 | ns | |
| $t_{CO}$ | Chip Select to Output Valid | | | 150 | ns | |
| $t_{CX}$ | Chip Select to Output Enabled | 0 | | | | |
| $t_{OTD}$ | Chip Deselect to Output Off | | | 150 | ns | |
| $t_{OHA}$ | Output Hold From Address Change | 50 | | | ns | |
| WRITE CYCLE | | | | | | |
| $t_{WC}$ | Write Cycle Time | 450 | | | ns | |
| $t_{AW}$ | Address to Write Setup Time | 0 | | | ns | |
| $t_W$ | Write Pulse Width | 250 | | | ns | |
| $t_{WR}$ | Write Release Time | 50 | | | ns | |
| $t_{OTW}$ | Write to Output Off | | | 150 | ns | |
| $t_{DW}$ | Data to Write Overlap | 250 | | | ns | |
| $t_{DH}$ | Data Hold | 0 | | | | |
| CI/O | Input/Output Capacitance at 25°C | | | 10 | pF | f = 1 MHz |
| CIN | Input Capacitance at 25°C | | | 8 | pF | f = 1 MHz |

NOTE: This parameter is periodically sampled and not 100% tested.

### A.C. Test Conditions

Input Pulse Levels. . . . . 0.8V to 2.0V
Input Rise and Fall Time. . . . . 10 nsec
Timing Measurement Levels: Input . . . . . 1.5V
Output . . . . . 0.8 and 2.0V
Output Load. . . . . 1 TTL Gate and 50 pF




**Block Diagram**

# ROM
## Memory Devices

NMOS
MEMORY
PRODUCTS

DOCUMENT NO. 29000 D43
REVISION 2, OCT. 1977

PART NUMBER
**R2316A/B**

Rockwell

# R6500 Microcomputer System

## DATA SHEET

# 2048 X 8 STATIC READ ONLY MEMORY



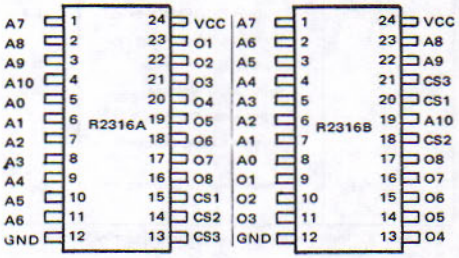


## DESCRIPTION

The R2316A and R2316B high performance read only memories are organized 2048 words by 8 bits with access times of less than 550 ns and 450 ns. These ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

The R2316A/B operate totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

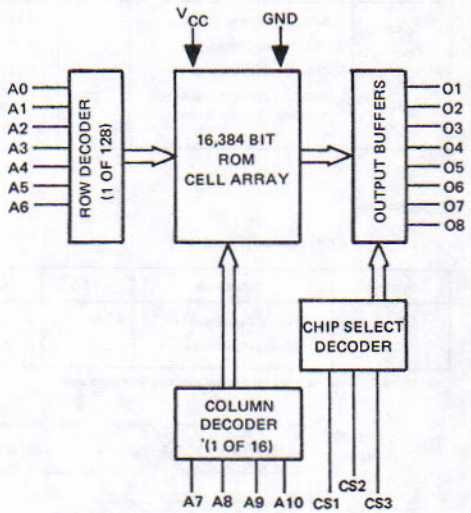
Designed to replace two 2708 8K EPROMs, the R2316B can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.




**Pin Configuration**

## FEATURES

- 2048 x 8 Bit Organization
- Single +5 Volt Supply
- Metal Mask Programming
- Two Week Prototype Turnaround
- Access Time – 550 ns/450 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- R2316A – Replacement for Intel 2316A
- R2316B – Pin Compatible with 2708 EPROM
  – Replacement for Two 2708s




**Block Diagram**

### Ordering Information

| Order Number | Package Type | Access Time | Temperature Range |
|---|---|---|---|
| R2316AC | Ceramic | 550 ns | 0°C to +70°C |
| R2316AP | Plastic | 550 ns | 0°C to +70°C |
| R2316BC | Ceramic | 450 ns | 0°C to +70°C |
| R2316BP | Plastic | 450 ns | 0°C to +70°C |

A custom number will be assigned by Rockwell.



Specifications subject to change without notice

## SPECIFICATIONS

### Absolute Maximum Ratings

| | |
|---|---|
| Ambient Operating Temperature | $0^{\circ}$ to $+70^{\circ}C$ |
| Storage Temperature | $-65^{\circ}C$ to $+150^{\circ}C$ |
| Supply Voltage to Ground Potential | -0.5V to +7.0V |
| Applied Output Voltage | -0.5V to +7.0V |
| Applied Input Voltage | -0.5V to +7.0V |
| Power Dissipation | 1.0W |

### Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### D.C. Characteristics

$T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = 5.0V \pm 5\%$ (unless otherwise specified)

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.4 | $V_{CC}$ | Volts | $V_{CC} = 4.75V$, $I_{OH} = 200\ \mu A$ |
| $V_{OL}$ | Output LOW Voltage | | 0.4 | Volts | $V_{CC} = 4.75V$, $I_{OL} = 2.1$ mA |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | $V_{CC}$ | Volts | |
| $V_{IL}$ | Input LOW Voltage | -0.5 | 0.8 | Volts | See Note 1 |
| $I_{LI}$ | Input Load Current | | 10 | $\mu A$ | $V_{CC} = 5.25V$, $0V \leq V_{in} \leq 5.25V$ |
| $I_{LO}$ | Output Leakage Current | | 10 | $\mu A$ | Chip Deselected<br>$V_{out} = +0.4V$ to $V_{CC}$ |
| $I_{CC}$ | Power Supply Current | | 98 | mA | Output Unloaded<br>$V_{CC} = 5.25V$, $V_{in} = V_{CC}$ |

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

### A.C. Characteristics

$T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = 5.0V \pm 5\%$ (unless otherwise specified)

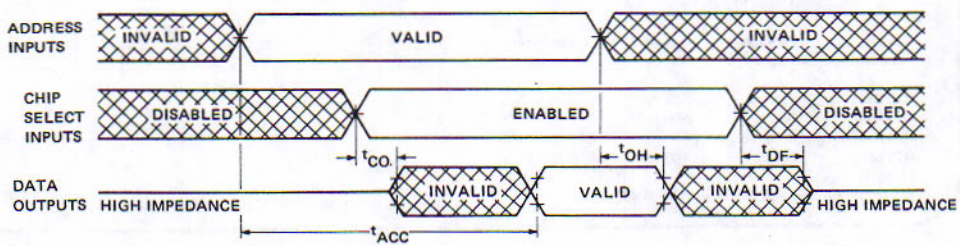
| Symbol | Parameter | R2316B | | R2316A | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $t_{ACC}$ | Address Access Time | | 450 | | 550 | ns | Output load: 1 TTL load and 100 pF |
| $t_{CO}$ | Chip Select Delay | | 250 | | 300 | ns | |
| $t_{DF}$ | Chip Deselect Delay | | 250 | | 300 | ns | Input transition time: 20 ns |
| $t_{OH}$ | Previous Data Valid After Address Change Delay | 20 | | 20 | | ns | Timing reference levels:<br>Input: 1.5V<br>Output: 0.8V and 2.2V |

### Capacitance

$t_A = 25^{\circ}C$, f = 1.0 MHz, See Note 2

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $C_I$ | Input Capacitance | | 7 | pF | All pins except pin under test tied to AC ground |
| $C_O$ | Output Capacitance | | 10 | pF | |

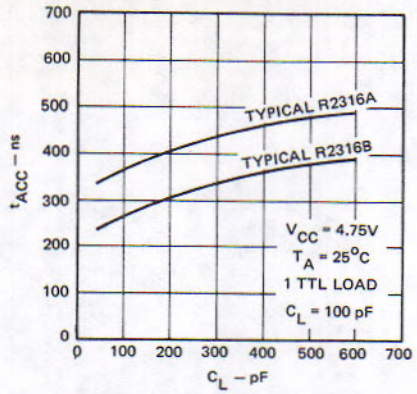
Note 2: This parameter is periodically sampled and is not 100% tested.



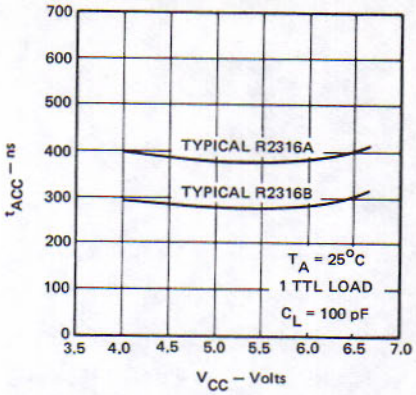

Timing Diagram

## Typical Characteristics

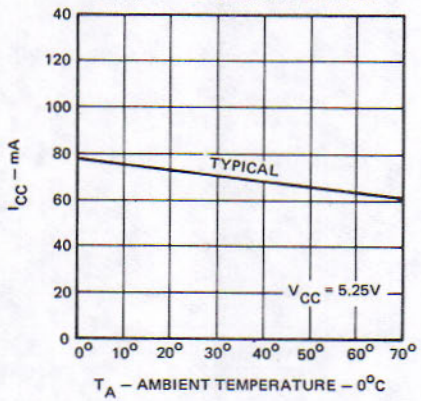
### Access Time vs Capacitive Load



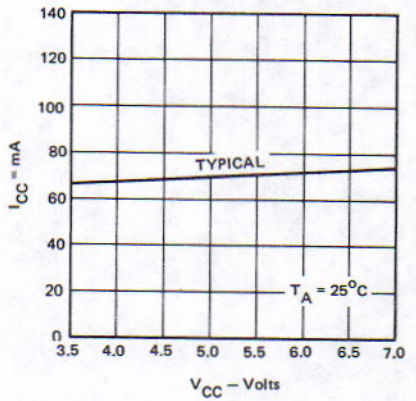

### Access Time vs Supply Voltage




### Supply Current vs Ambient Temperature

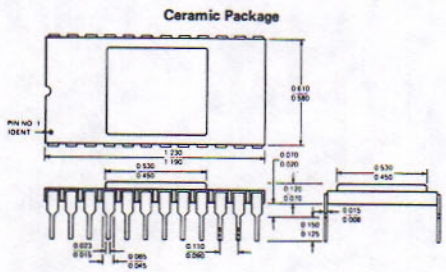



### Supply Current vs Supply Voltage

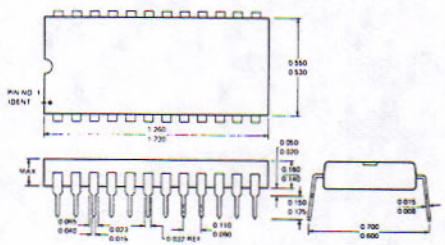



## Packaging Diagram

### Ceramic Package



### Plastic Package



NMOS
MEMORY
PRODUCTS

DOCUMENT NO. 29000 D48
REVISION 3, JAN. 1979

PART NUMBER
R2332, R2332-3

Rockwell

# DATA SHEET

# 4096 X 8 STATIC READ ONLY MEMORY



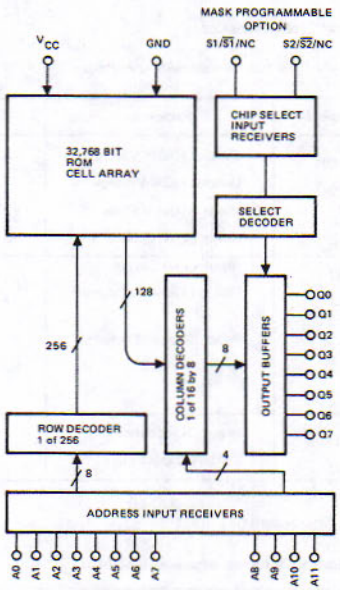
## DESCRIPTION

The R2332 is a high performance, 32,768-bit static Read Only Memory, organized 4,096 words by 8 bits. The device is an industry standard, 24-pin, dual-in-line package, and is available in ceramic or low cost plastic packages. This fully static 32K ROM is compatible with all eight bit N-channel microprocessors including the R6500 family of microprocessors. The R2332 offers TTL input and output levels with a minimum noise immunity of 0.4 volts.

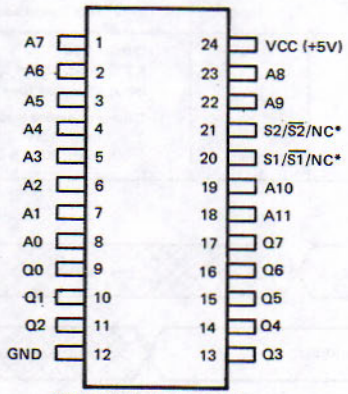
The R2332 operates totally asynchronously; no clock input is required. Two programmable chip select inputs allow up to four R2332 32K ROMs to be OR-tied without external coding. The device provides three-state output buffers for memory expansion.

## FEATURES

- 32,768 bits, organized in 4,096 8-bit words
- Max access time: 450 ns for R2332
  300 ns for R2332-3
- Typical power dissipation is 400 mW
- Drives one TTL load and 100 pF
- Single +5-volt power input
- Totally static operation, no clock input required
- Completely TTL compatible
- Two programmable chip select inputs
- Three state outputs for memory expansion
- Identical cycle and access time




R2332 Block Diagram




*Mask-programmable option

R2332 Pin Configuration

### Ordering Information

**Order Number:** R2332 ___ or R2332-3 ___ ___

Temperature Range:

- No suffix = 0°C to +70°C
- E = -40°C to +85°C (Industrial)
- MT = -55°C to +125°C (Military)
- M = MIL-STD-883, Class B

Package:

- C = Ceramic
- P = Plastic (Not Available for M or MT suffix)

**NOTE:** Contact your local Rockwell Representative for availability.



Specifications subject to change without notice

## SPECIFICATIONS

### Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.3 to +7.0 | Vdc |
| Input Voltage | $V_{in}$ | -0.3 to +7.0 | Vdc |
| Operating Temperature | $T_A$ | | °C |
| Commercial | | 0 to +70 | |
| Industrial | | -40 to +85 | |
| Military | | -55 to +125 | |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C |

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

### Electrical Characteristics

$V_{CC}$ = 5.0V ± 5% (unless otherwise specified)

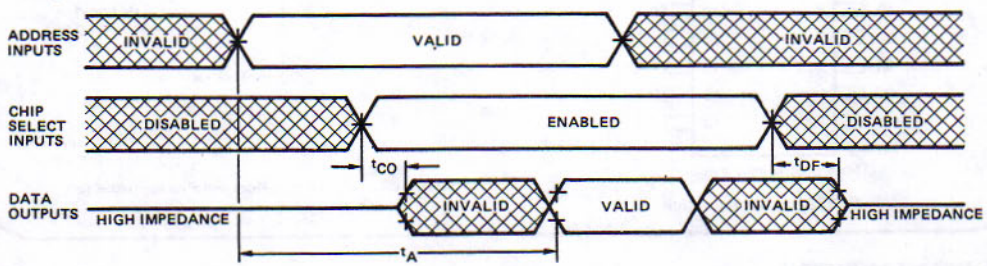
| Symbol | Parameter | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | $V_{CC}$ | Volts | $V_{CC}$ = 4.75V, $I_{OH}$ = -200 μA |
| $V_{OL}$ | Output LOW Voltage | | | 0.4 | Volts | $V_{CC}$ = 4.75V, $I_{OL}$ = 2.1 mA |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | $V_{CC}$ | Volts | |
| $V_{IL}$ | Input LOW Voltage | -0.5 | | 0.8 | Volts | |
| $I_{LI}$ | Input Load Current | | | 10 | μA | $V_{CC}$ = 5.25V, 0V ≤ $V_{in}$ ≤ 5.25V |
| $I_{LO}$ | Output Leakage Current | | | ±10 | μA | Chip Deselected, $V_{CC}$ = 5.25V, $V_{out}$ = +0.4V to $V_{CC}$ |
| $I_{CC}$ | Power Supply Current | | | | mA | $V_{CC}$ = 5.25V |
| | | | 80 | 120 | | 0°C to 70°C, R2332 |
| | | | 80 | 150 | | -55°C to +125°C, R2332 |
| | | | 90 | 135 | | 0°C to 70°C, R2332-3 |
| $C_I$ | Input Capacitance | | | 7 | pF | $V_{CC}$ = 5.0V, chip deselected, pin under test at 0V, $T_A$ = 25°C, f = 1 MHz |
| $C_O$ | Output Capacitance | | | 10 | pF | |

### Timing Characteristics

$V_{CC}$ = 5.0V ± 5% (unless otherwise specified)

| Symbol | Parameter | R2332 Max | R2332-3 Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $t_A$ | Address Access Time | 450 | 300 | ns | Output load: 1 TTL load, 100 pf<br>Input transition time: 20 ns |
| $t_{CO}$ | Chip Select Delay | 200 | 150 | ns | Timing reference levels:<br>Input: 1.5V |
| $t_{DF}$ | Chip Deselect Delay | 200 | 150 | ns | Output: 0.8V & 2.0V |

### Timing



# PPS
Family Brochure

# PPS

MICROPROCESSOR FAMILIES

# PMOS



Rockwell International

PPS
PMOS
PRODUCTS

# Rockwell Microcomputers Are Dedicated to The Real World of Equipment Systems

Rockwell designs its microcomputers to provide basically all-LSI functional systems for your equipment, machines and products.

Too often, the savings and performance promised by other microprocessors are short-changed in the real world of designing equipment systems. These microprocessors are no more than computational sub-systems and adding required peripheral and support circuitry cuts the heart out of anticipated savings.

The most visible evidence of the economics of Rockwell's system-oriented microcomputers is the success of their applications . . . consumer products and games, cash registers, weighing scales and business equipment, advanced terminals, automotive controls and diagnostic equipment, instrumentation, process and production controls, telephones and other telecommunications equipment. . .



Rockwell International

Microelectronic Device Division

## Here Are Highlight Reasons Why Rockwell's System-Oriented Microcomputers Give You Products That Cost Less, Do More

**System Options** - Rockwell offers five compatible microcomputer families, from one-chippers through multi-chip eight-bit systems. You select the most cost-effective microcomputer for your immediate product needs knowing that expansion and changes are only a few LSI chips and simple program modifications away.

**LSI Circuit Options** - Rockwell provides LSI circuit options as interfacing and controlling circuitry for peripherals in the real world of your equipment. For keyboards, displays, printers, memories, telecommunications and even peripherals like floppy disks, you simply select the appropriate LSI circuit . . . And you can add or change interfacing LSI chips with small program modifications - - you don't have to re-do your total program.

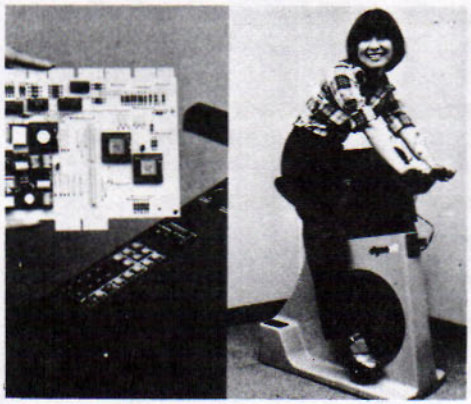
**Powerful, Flexible Instruction Sets** - Rockwell's software is ingeniously designed to simplify program assembly and debugging. Multi-function instructions reduce ROM requirements; instructions can often be pooled to reduce ROM requirements by 30% versus other approaches (and Rockwell offers an 8K x 8 ROM so that more complex equipment has minimum parts' count).

**Parallel Processing/Partitioned Intelligence** - Rockwell uses the economies of LSI techniques for all I/O and peripheral control functions, distributing various levels of intelligence over the system to permit concurrent execution. This distributed processing structure lowers costs and increases system throughput. Simplified bus control, system flexibility and enhanced software modularity are other advantages. On-chip memory address and decode, on-chip interrupt logic in I/O and peripheral controller devices, and innovative instructions are among other design strategies used to achieve the high system performance and economies of Rockwell microcomputers.


MOBILE TELEPHONE


HIGH-SPEED PRINTER

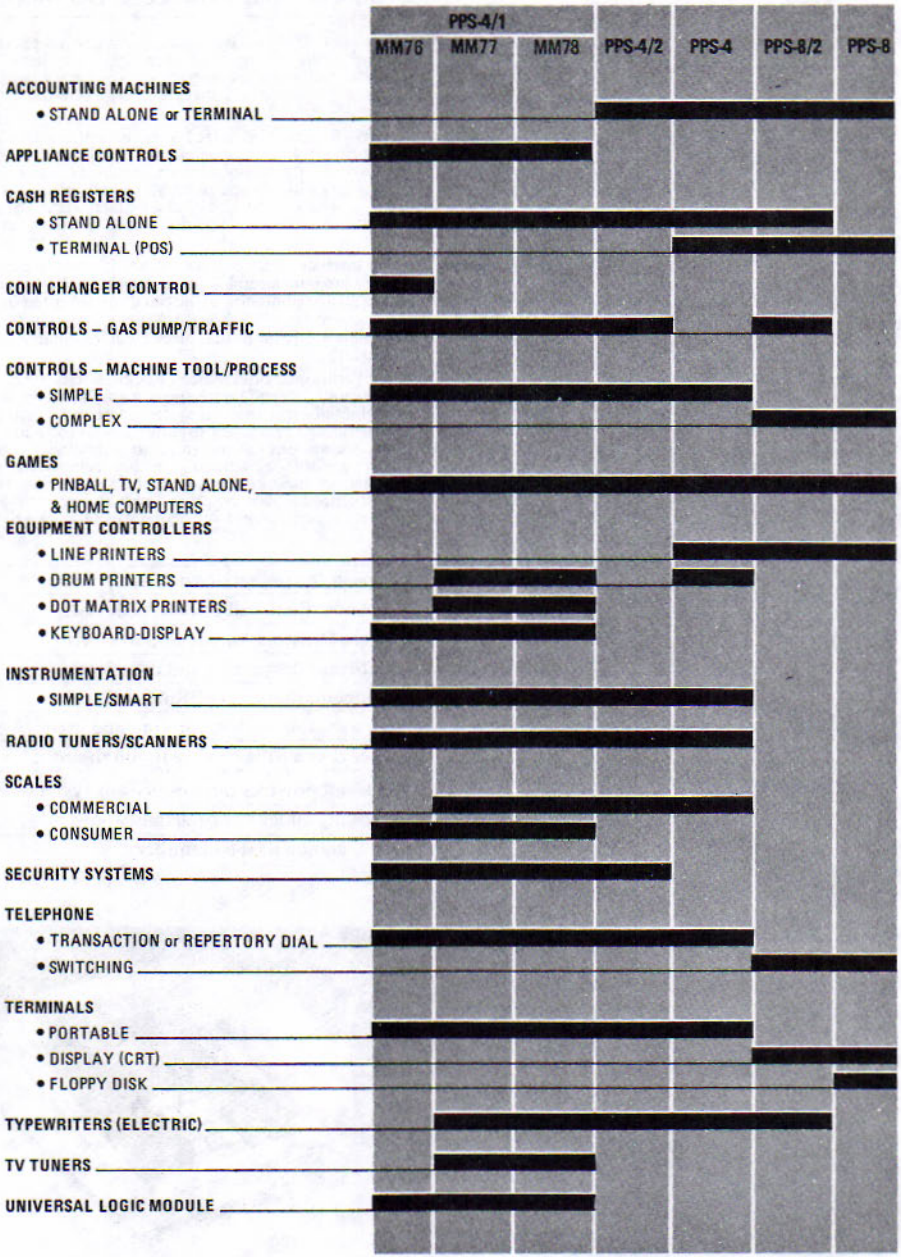
**To speed the design of your equipment systems, Rockwell backs its All-LSI, System-Oriented Microcomputers with efficient design aids and complete documentation . . . Or, Rockwell will design a custom system for you, and even produce it as a subassembly if you desire . . . and Rockwell provides microprocessor systems meeting all levels of reliability- - - commercial and military**




TRANSACTION TELEPHONE

PPS
PMOS
PRODUCTS

# This Summary of Typical PPS Applications Spells Out The Versatility of Rockwell's All-LSI Microcomputers



# Now - Select The Cost-Effective Rockwell Microcomputer For Your Equipment System . . . Your Future's Built In

| | PPS-4/1 | | | PPS-4/2 | PPS-4 | PPS-8/2 | PPS-8 |
|---|---|---|---|---|---|---|---|
| | MM76 | MM77 | MM78 | | | | |
| | (SEE PAGE 4) | | | | | | |
| **MINIMUM MICROCOMPUTER (LSI CHIPS)** | 1 | | | 2 | 3 | 2 | 5 |
| **DIRECT BUS DRIVING CAPABILITY (LSI CHIPS)** | 1 | | | 10 | 32 | 10 | 32 |

*(NOTE: PPS system design and LSI interface chips permit extensive expansion of PPS systems beyond chip levels indicated)*

**LSI SYSTEM OPTIONS:**

| | | | | | | |
|---|---|---|---|---|---|---|
| • LSI I/O CONTROLLER DEVICES | ON CHIP | | | 9 | | 12 |
| • LSI COMMUNICATIONS I/O DEVICES | | | | | | |
| SERIAL | ON CHIP | | | 2 | | |
| PARALLEL | ON CHIP | | | 2 | | 3 |
| • DIRECTLY ADDRESSABLE I/O DEVICES | | | | 16 | | |
| • I/O PORTS (MINIMUM) | 31 | | | 28 | 12 | 16 |
| SERIAL (MINIMUM) | 1 | | | | | 1 |
| • DIRECTLY ADDRESSABLE MEMORY | | | | | | |
| ROM (8-BIT BYTES) | 640 | 1,344 | 2,048 | 4,096 | | 16,384 |
| RAM (4 or 8-BIT BYTES) | 48 | 96 | 128 | 4,096 | | 16,384 |

*(NOTE: PPS system design and I/O chips permit memory expansion many times the maximums indicated through banking and software control)*

**SYSTEM PERFORMANCE CRITERIA:**

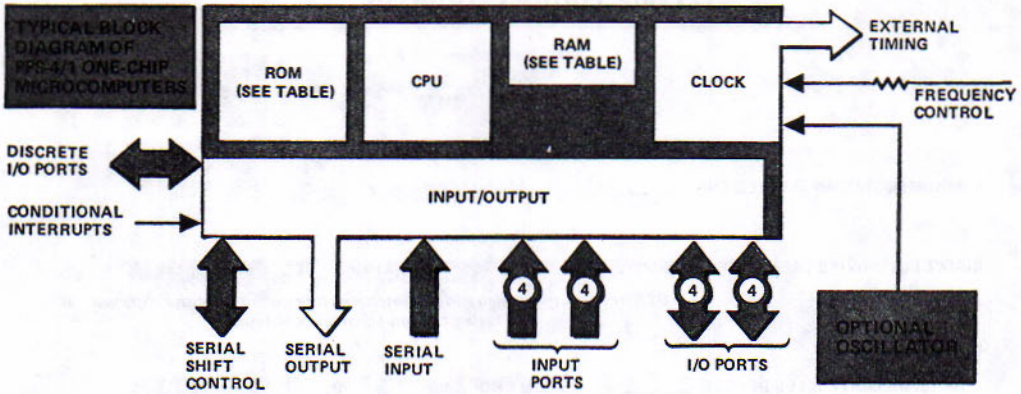
| | | | | | | |
|---|---|---|---|---|---|---|
| • DATA WORD LENGTH (BITS) | 4 | | | | 8 | |
| • INSTRUCTION WORD LENGTHS (BITS) | 8, 16, 24 | | | 8, 16 | 8, 16, 24 | |
| • DIRECT MEMORY ACCESS | | | | | 8 CHANNELS | |
| • DECIMAL ADD/SUBTRACT (μS/DIGIT) Ⓣ | 100 | 87.5 | | 30 | 24 | 15 | 12 |
| • DATA MANIPULATION (μS/BYTE) Ⓣ | 37.5 | | | 30 | 24 | 15 | 12 |
| • TABLE SEARCH (μS/BYTE) Ⓣ | 62.5 | | | 25 | 20 | 15 | 12 |
| • BURST DATA TRANSFER (μS/BYTE) | | | | | | 5 | 4 |
| • INSTRUCTIONS | 50 | | | | | 109 | |
| • INTERRUPT CAPABILITY | PSEUDO 1 LEVEL (2 Lines) | | | NONE | 1 LEVEL | 3 LEVEL (15 Sublevels) | |

Ⓣ *TYPICAL*

**PROGRAMMING AIDS** — *Universal Assemulator with Personality Boards for all systems. Assembler programs in Fortran also available directly or via timesharing. Development modules and all documentation.*

PPS PMOS PRODUCTS

# Versatile One-Chip Rockwell PPS-4/1 Microcomputers Offer Low-Cost Options for A Surprisingly Broad Product Range




PPS PMOS PRODUCTS

## Rockwell PPS-4/1 one-chip microcomputers.

### "CMOS POWER @ PMOS PRICES"

| Features/Models | MM75 | MM76 | MM76C* | MM76E | MM77 | MM78 | MM76L | MM76EL | MM77L | MM78L |
|---|---|---|---|---|---|---|---|---|---|---|
| ROM (X8) | 640 | 640 | 640 | 1024 | 1344 | 2048 | 640 | 1024 | 1536 | 2048 |
| RAM (X4) | 48 | 48 | 48 | 48 | 96 | 128 | 48 | 48 | 96 | 128 |
| Total I/O Lines | 22 | 31 | 39 | 31 | 31 | 31 | 31 | 31 | 31 | 31 |
| Cond. Interrupt | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Parallel Input | 4 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Bidirectional Parallel | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| Discrete | 9 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 |
| Serial | – | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| Package (In-Line) | 28 pin dual | 42 pin quad | 52 pin quad | 42 pin quad | 42 pin quad | 42 pin quad | 40 pin dual | 40 pin dual | 40 pin dual | 40 pin dual |
| Power | –15V @ 70mw (typical) | | | | | | –6.5 to –11V @ 15mw (typical) | | | |

*Two 8-bit or one 16-bit presetable up/down counter

# Details of PPS-4/1 One-Chip Microcomputers

**Available as Production Chips or as Prototype Chips (internal ROM is blank)**

**Part numbers of Prototype Chips are shown in parentheses below.**

## Standard Models

| | | Part Number |
|---|---|---|
| **MM76** | Has CPU, 640 x 8 ROM, 48 x 4 ROM, internal clock logic and 31 I/O lines. 42-pin package. Designed for consumer product applications. | A76XX (A7698) |
| **MM75** | Similar to MM76, but has only 22 I/O lines. 28-pin package. Designed to meet low-cost requirements. | A75XX (A7698) |
| **MM76C** | Has all features of MM76, but also has a highspeed (1 MHz) counter and 39 I/O lines. 52-pin package. | A79XX (A7999) |
| **MM76E** | Same as MM76, but has 1024 x 8 ROM. 42-pin package. | A86XX (A7698) |
| **MM77** | Has CPU, 1344 x 8 ROM, 96 x 4 RAM, internal clock logic and 31 I/O lines. 42-pin package. Versatile 4-bit microcomputer for peripheral controllers, universal logic, etc. | A77XX (A7798) |
| **MM78** | Same as MM77, but has 2048 x 8 ROM and 128 x 4 RAM. 42-pin package. | A78XX (A7898) |

## Low Power, Low Voltage Models

| | | |
|---|---|---|
| **MM76L** | Same internal features as MM76. 40-pin package. | B76XX (B7698) |
| **MM76EL** | Same internal features as MM76E. 40-pin package. | B86XX (B7698) |
| **MM77L** | Same internal features as MM77, but has 1536 x 8 ROM. 40-pin package. | B77XX (B7899) |
| **MM78L** | Same internal features as MM78. 40-pin package. | B78XX (B7899) |

**For Production Chips, minimum quantity is 1000 with your ROM encoding data.**

**The Rockwell XPO-1. . . Low Cost Single-Board Development System With ROM-Resident Utility/Debug/Monitor Program. . . Based on PPS-4/1**

You'll find PPS-4/1 program development easy and inexpensive with our single-board XPO-1 System Development Microcomputer. Briefly, XPO-1 has these features:

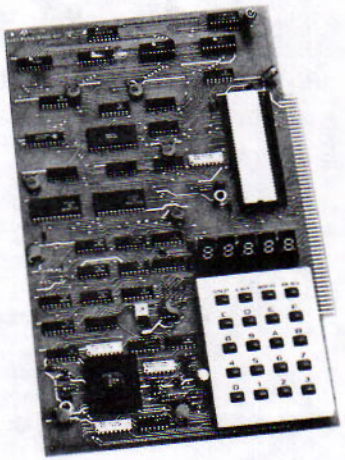
- Your choice of MM76, MM77 or MM78 One-Chip Microcomputer
- 1K x 8 instruction RAM for your program (2K x 8 optional)
- 20-key hexadecimal keyboard for program entry and control
- Five-digit hexadecimal display shows address and data
- ROM - resident Supervisory Program Device chip holds Utility/Debug/Monitor Assembler/Line Editor program.
- Current loop interface, for reading or punching paper tape on an ASR-33 TTY
- 100-pin edge connector, to interface to your prototype product

## XPO-1 Options

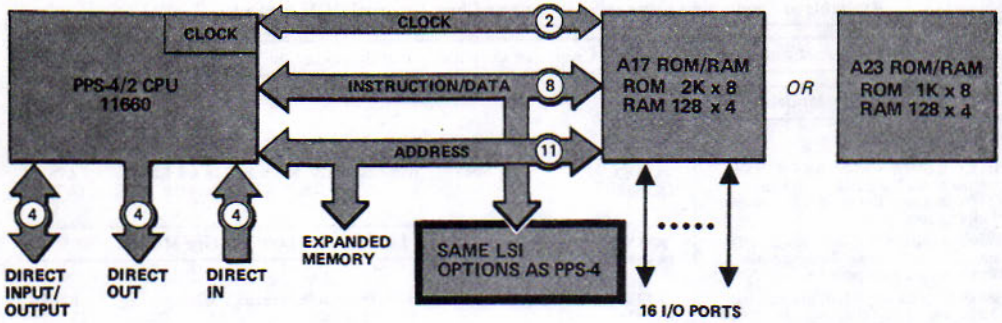
| | | Part Number |
|---|---|---|
| **XPO-1/76** | XPO-1 with MM76 Development Circuit (A7699) | XPO-1/76 |
| **XPO-1/77** | XPO-1 with MM77 Development Circuit (A7799) | XPO-1/77 |
| **XPO-1/78** | XPO-1 with MM78 Development Circuit (A7899) | XPO-1/78 |
| **MM76C** | Adapter Kit | PE00-D301 |

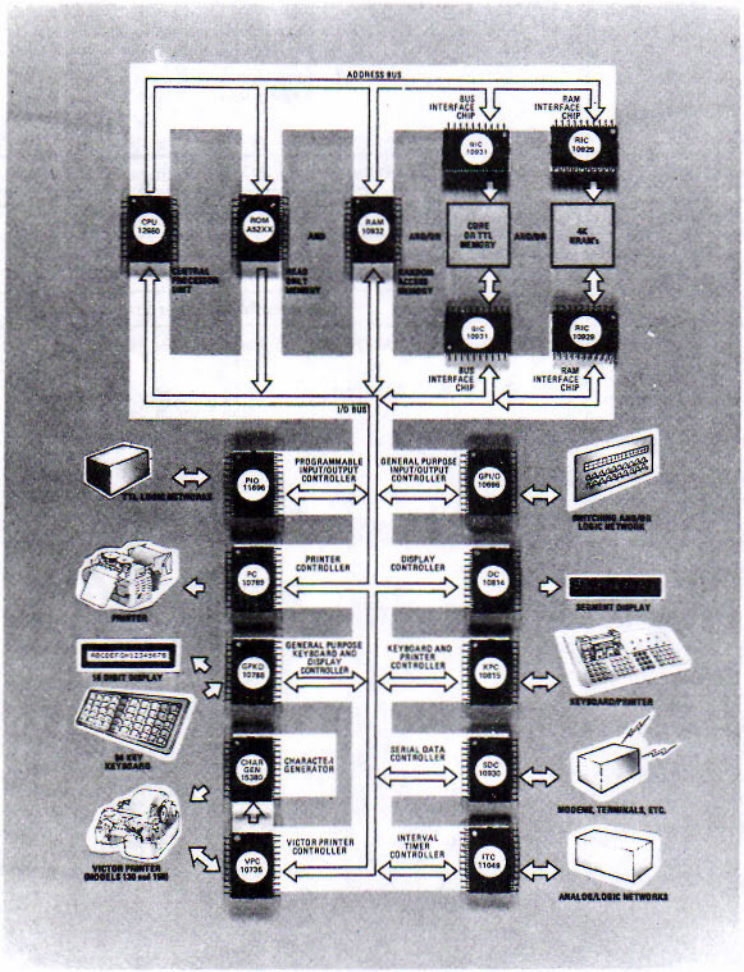
## Assembler/Editor Program Devices

| | | |
|---|---|---|
| **MM76 PD** | MM76 Assembler/Editor Program Device | A7806 |
| **MM77/78 PD** | MM77 and MM78 Assembler/ Editor Program Device | A7807 |



PPS PMOS PRODUCTS


CLOCK
PPS-4/2 CPU
11660
CLOCK
2
INSTRUCTION/DATA
8
ADDRESS
11
A17 ROM/RAM
ROM 2K x 8
RAM 128 x 4
OR
A23 ROM/RAM
ROM 1K x 8
RAM 128 x 4
4
4
4
DIRECT
INPUT/
OUTPUT
DIRECT
OUT
DIRECT
IN
EXPANDED
MEMORY
SAME LSI
OPTIONS AS PPS-4
16 I/O PORTS


ADDRESS BUS
BUS INTERFACE CHIP
RAM INTERFACE CHIP
I/O BUS
PROGRAMMABLE INPUT/OUTPUT CONTROLLER
GENERAL PURPOSE INPUT/OUTPUT CONTROLLER
PRINTER CONTROLLER
DISPLAY CONTROLLER
GENERAL PURPOSE KEYBOARD AND DISPLAY CONTROLLER
KEYBOARD AND PRINTER CONTROLLER
CHARACTER GENERATOR
SERIAL DATA CONTROLLER
VICTOR PRINTER CONTROLLER
INTERVAL TIMER CONTROLLER
PRINTER
SEGMENT DISPLAY
KEYBOARD/PRINTER
MODEMS, TERMINALS, ETC.
ANALOG/LOGIC NETWORKS

# Details of PPS-4 and PPS-4/2 Microcomputer Options

## CPU Devices

| | | Part Number |
|---|---|---|
| 4 | **PPS-4 CENTRAL PROCESSOR UNIT (CPU) WITH INTERRUPT.** Receives and decodes 8-bit instruction words to perform 4-bit arithmetic and logic operations. | 12660 |
| 4/2 | **PPS-4/2 CENTRAL PROCESSOR UNIT (CPU).** Designed to combine with A17XX or A23XX ROM-RAM-I/O to provide a basic two-circuit microcomputer. PPS-4/2 uses identical instruction set as PPS-4 but includes clock generator function within CPU. Bus drive capability; (100 pF, 10 chips). | 11660 |

## RAM Devices

| | | |
|---|---|---|
| 256x4 | **RANDOM ACCESS MEMORY (RAM).** | 10432 |
| 512x4 | **RANDOM ACCESS MEMORY (RAM).** | 10932 |

## ROM Devices

| | | |
|---|---|---|
| 1Kx8 | **READ ONLY MEMORY (ROM).** | A05XX |
| 2Kx8 | **READ ONLY MEMORY (ROM).** | A52XX |
| 4Kx8 | **READ ONLY MEMORY (ROM).** | A66XX |
| 8Kx8 | **READ ONLY MEMORY (ROM).** | A88XX |

## ROM/RAM Devices

| | | |
|---|---|---|
| A08 | **ROM-RAM.** 704 x 8 ROM; 72 x 4 RAM. | A08XX |
| A07 | **ROM-RAM.** 1024 x 8 ROM; 116 x 4 RAM. | A07XX |
| A20 | **ROM-RAM.** 1536 x 8 ROM; 128 x 4 RAM. | A20XX |
| A17 | **ROM-RAM-I/O.** 2048 x 8 ROM; 128 x 4 RAM; 16 one-bit I/O ports. | A17XX |
| A23 | **ROM-RAM-I/O.** 1024 x 8 ROM; 128 x 4 RAM; 16 one-bit I/O ports. | A23XX |
| A1799 | **ROM-RAM-I/O EVALUATION CIRCUIT.** For emulation and program development of PPS-4/2 systems using A17XX or A23XX. ROM is disabled. | A1799 |

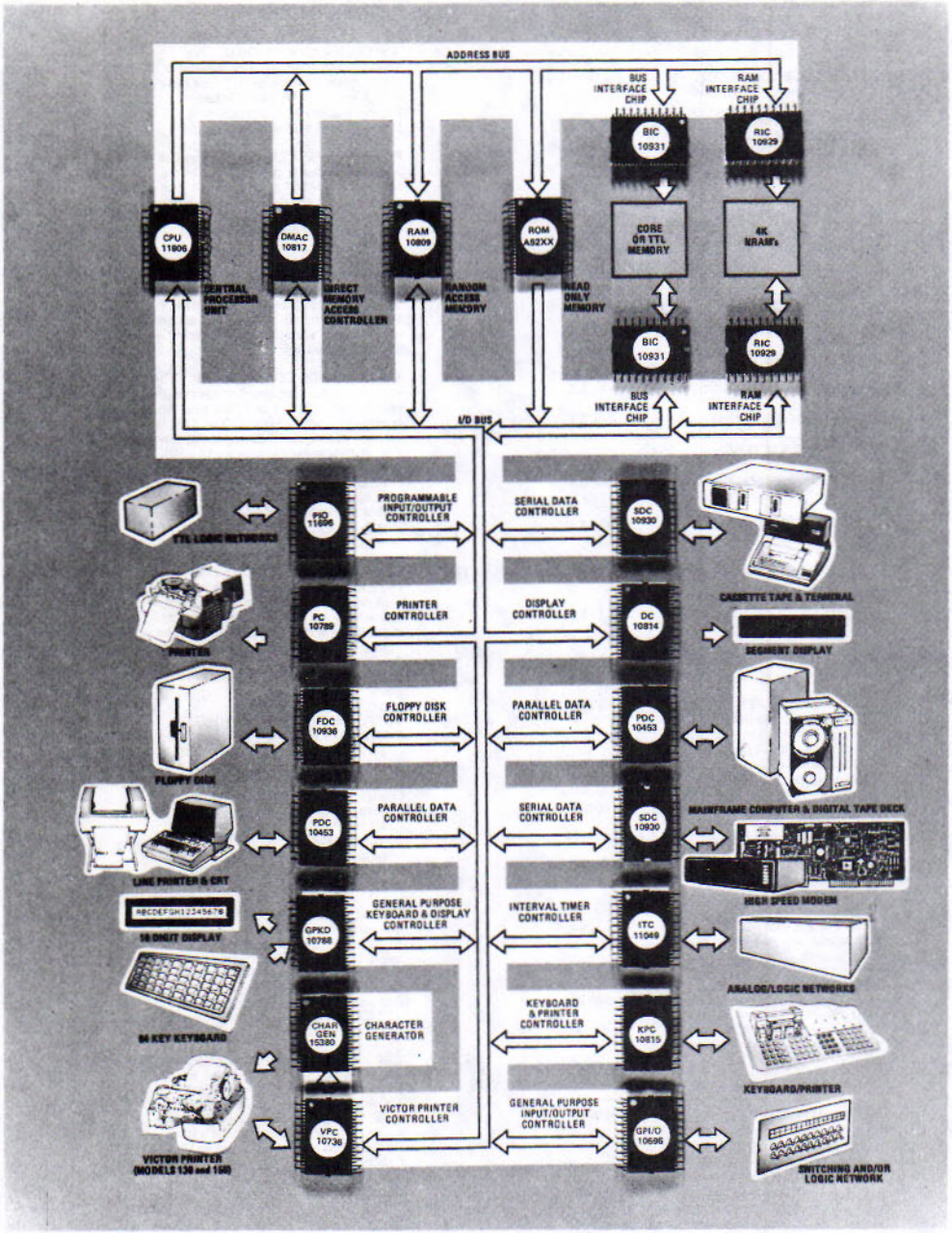
## Supplementary Devices

| | | |
|---|---|---|
| CLK | **CLOCK GENERATOR.** Generates the basic clock signals A and $\overline{B}$ for PPS-4 and PPS-8 microcomputer products. | 10706 |
| BIC | **BUS INTERFACE CIRCUIT.** Permits core, static memories, and TTL I/O access to the PPS bus. | 10931 |
| ITC | **INTERVAL TIMER.** Provides four 12-bit counters that may be used for a variety of real-time counting/timing applications in conjunction with PPS-4 family circuits. | 11049 |
| RIC | **4K RAM INTERFACE.** Provides interface with standard N-channel 16-pin 4K RAM circuits for program or data memory. Performs all refresh and control functions. | 10929 |

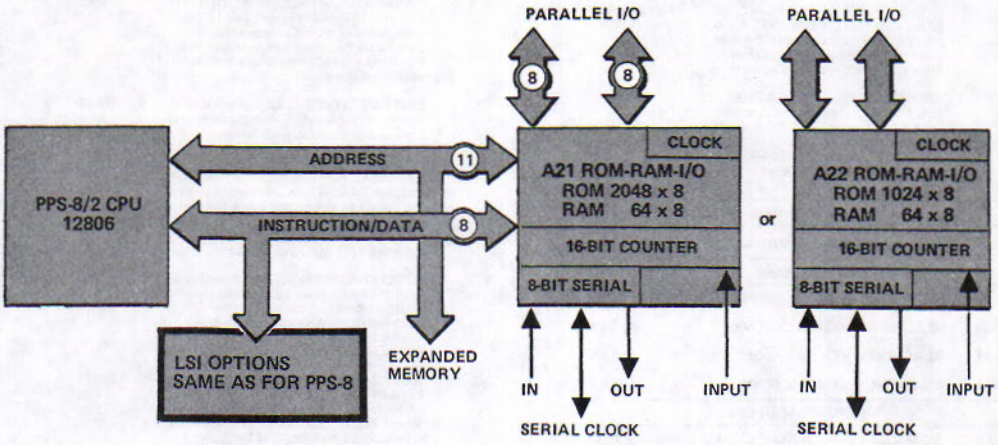
## Input/Output Devices

| | | |
|---|---|---|
| GPI/O | **GENERAL PURPOSE INPUT/OUTPUT.** Provides 12 discrete inputs and 12 discrete outputs, all TTL compatible, for direct data exchange or status and control function exchange with an external peripheral device. | 10696 |
| DC | **DISPLAY CONTROLLER.** Provides control of a 16-digit 7/8 segment display. Uses internal buffer, decode logic and output strobes. | 10814 |
| GPKD | **GENERAL PURPOSE KEYBOARD AND DISPLAY CONTROL.** Provides 64-key strobing, key debounce, 2-key rollover protection, 9-key buffering, and two 16 4-bit character display buffers with automatic segment/digit strobing. | 10788 |
| PC | **PRINTER CONTROLLER.** Provides 21 4-bit character print buffers and automatic control and timing for the commercially-available Shinshu Seiko Company printers, Models 101, 102 and 104. Can be adapted to other printers. | 10789 |
| KPC | **KEYBOARD/PRINTER CONTROLLER.** Provides complete control for the Shinshu Seiko Model 310 and 320 as well as Precisa Model 388-16 and 388-21 printers and the capability of scanning and buffering a 64-key keyboard. | 10815 |
| SDC | **SERIAL DATA CONTROLLER.** The SDC is a digital receiver-transmitter that interfaces the PPS-4 or PPS-8 to a serial communications channel. The SDC is capable of half and full-duplex operation at synchronous rates up to 250K bps (PPS-8) or 100K bps (PPS-4) and asynchronous rates up to 18K bps (PPS-8) or 12K bps (PPS-4). Capable of programmable transmission modes; character length of 5, 6, 7, 8 bits; even, odd, or no parity; one or two stop bits. | 10930 |
| TDI | **TELECOMMUNICATIONS DATA INTERFACE.** The TDI is an advanced type of modem with UART (Universal Asynchronous Receiver/Transmitter) capabilities which provides both full-duplex and half-duplex asynchronous data transmission at 1200 bits per second over non-conditioned voice-grade telephone lines. | 10371 |
| VPC | **VICTOR DOT MATRIX PRINTER CONTROLLER.** A two-chip set used to provide complete control of the Victor alphanumeric dot-matrix printers, Models 130 and 150. Printer Controller 10736 provides control of printing, paper movement, and ribbon color selection. Character Generator 15380 is a special ROM which contains all of the coding required to print out selected characters in dot-matrix patterns. | 10736/ 15380 |
| PI/O | **PARALLEL INPUT/OUTPUT.** Bus compatible with PPS-4 and PPS-8 to provide 24, bidirectional, $T^2L$ compatible I/O lines. Programmable to operate in static, clocked or discrete mode. In static and clocked, performs parallel I/O on 4 or 8-bit bytes. In discrete, 16 I/O lines are individually controlled while 8 lines still operate in parallel. | 11696 |
| LRC | **LRC PRINTER CONTROLLER.** On one chip, all logic and encoded ROM to generate 64, single or double width, 5 x 7 ASCII code characters in maximum lines of 40 characters. Provides single or multiple paper feeds with forward and reverse option. $T^2L$ and CMOS compatible. Optional parallel or serial interface to a host system provided. | RC7000 |

# Standard LSI Options Expand The Demonstrated Power of Rockwell PPS-8 Microcomputers



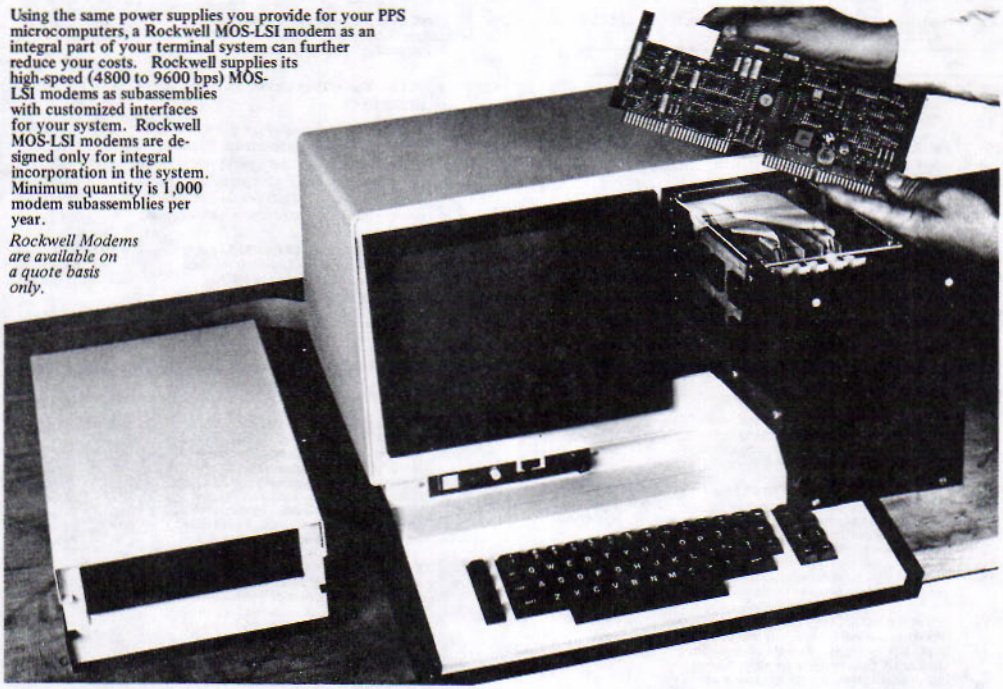
## The Same Instructions and Most of The PPS-8 Options Add Flexibility to Rockwell PPS-8/2 Microcomputers




## Reduce System Costs of Your Terminals with Microcomputers ... and Custom High-Speed MOS-LSI Integral MODEMs.

Using the same power supplies you provide for your PPS microcomputers, a Rockwell MOS-LSI modem as an integral part of your terminal system can further reduce your costs. Rockwell supplies its high-speed (4800 to 9600 bps) MOS-LSI modems as subassemblies with customized interfaces for your system. Rockwell MOS-LSI modems are designed only for integral incorporation in the system. Minimum quantity is 1,000 modem subassemblies per year.

*Rockwell Modems are available on a quote basis only.*



# Details of PPS-8 and PPS-8/2 Microcomputer Options



## CPU Devices

| | | Part Number |
|---|---|---|
| 8 | **PPS-8 CENTRAL PROCESSOR UNIT (CPU).** Receives and decodes 8-bit instruction words to perform 8-bit arithmetic and logic operations. | 11806 |
| 8/2 | **PPS-8/2 CENTRAL PROCESSOR UNIT (CPU).** Designed to combine with A21XX or A22XX ROM-RAM-I/O-CLK to provide a basic two-circuit microcomputer. PPS-8/2 uses identical instruction set as PPS-8. | 12806 |

## RAM Devices

| | | |
|---|---|---|
| 256x8 | **RANDOM ACCESS MEMORY (RAM).** | 10809 |

## ROM Devices

| | | |
|---|---|---|
| 1Kx8 | **READ ONLY MEMORY (ROM).** | A05XX |
| 2Kx8 | **READ ONLY MEMORY (ROM).** | A52XX |
| 4Kx8 | **READ ONLY MEMORY (ROM).** | A66XX |
| 8Kx8 | **READ ONLY MEMORY (ROM).** | A88XX |

## ROM/RAM Devices

| | | |
|---|---|---|
| A21 | **ROM-RAM-I/O WITH CLOCK.** 2048 x 8 ROM; 64 x 8 RAM; on-chip clock; 16 parallel I/O ports; 1 automatic serial I/O port; 16-bit interval timer. Designed to complete PPS-8/2 microcomputer with 12806 CPU. | A21XX |
| A2199 | **RAM-I/O EVALUATION CIRCUIT.** For emulation and development of PPS-8/2 systems using the A21XX. ROM is disabled. | A2199 |
| A22 | **ROM-RAM-I/O WITH CLOCK.** Same as A21XX but with 1024 x 8 ROM. | A22XX |

## Supplementary Devices

| | | |
|---|---|---|
| CLK | **CLOCK GENERATOR.** Generates the basic clock signals A and B for PPS-4 and PPS-8 microprocessor products. | 10706 |
| BIC | **BUS INTERFACE CIRCUIT.** Permits core, static memories, and TTL I/O access to the PPS bus. | 10931 |
| ITC | **INTERVAL TIMER.** Provides four 12-bit counters that may be used for a variety of real-time counting/timing applications in conjunction with PPS-8 family circuits. | 11049 |
| RIC | **4K RAM INTERFACE.** Provides interface with standard N-channel 16-pin 4K RAM circuits for program or data memory. | 10929 |

## Input/Output Devices

| | | |
|---|---|---|
| DMA | **DIRECT MEMORY ACCESS CONTROLLER.** Allows PPS-8 I/O devices to access RAM devices directly without disturbing CPU program execution. Eight independent, prioritized DMA channels are provided. | 10817 |
| PDC | **PARALLEL DATA CONTROLLER.** Provides a flexible programmable interface to external devices or for interfacing multiple PPS systems. The device provides two independent bidirectional input/output channels, each of which operates in a variety of parallel data transfer modes. | 10453 |
| FDC | **FLOPPY DISK CONTROLLER.** Provides control of data transfer to and from a floppy disk. Provides user-defined and/or IBM-compatible formats. Serves up to four drives. Single or double density. | 10936 |
| GPI/O | **GENERAL PURPOSE INPUT/OUTPUT.** Provides 12 discrete inputs and 12 discrete outputs, all TTL compatible, for direct data exchange or status and control function exchange with an external peripheral device. | 10696 |
| DC | **DISPLAY CONTROLLER.** Provides control of a 16-digit 7/8 segment display. Uses internal buffer, decodes logic and output strobes. | 10814 |
| GPKD | **GENERAL PURPOSE KEYBOARD AND DISPLAY CONTROL.** Provides 64-key strobing, key debounce, 2-key rollover protection, 9-key buffering, and two 16 4-bit character display buffers with automatic segment/digit strobing. | 10788 |
| PC | **PRINTER CONTROLLER.** Provides 21 4-bit character print buffers and automatic control and timing for the commercially-available Shinshu Seiko Company printers, Models 101, 102 and 104. Can be adapted to other printers. | 10789 |
| KPC | **KEYBOARD/PRINTER CONTROLLER.** Provides complete control for the Shinshu Seiko Model 310 and 320 as well as Precisa Model 388-16 and 388-21 printers and the capability of scanning and buffering a 64-key keyboard. | 10815 |
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| VPC | **VICTOR DOT MATRIX PRINTER CONTROLLER.** A two-chip set used to provide complete control of the Victor alpha-numeric dot-matrix printers, Models 130 and 150. Printer Controller 10736 provides control of printing, paper movement, and ribbon color selection. Character Generator 15380 is a special ROM which contains all of the coding required to print out selected characters in dot-matrix patterns. | 10736/ 15380 |
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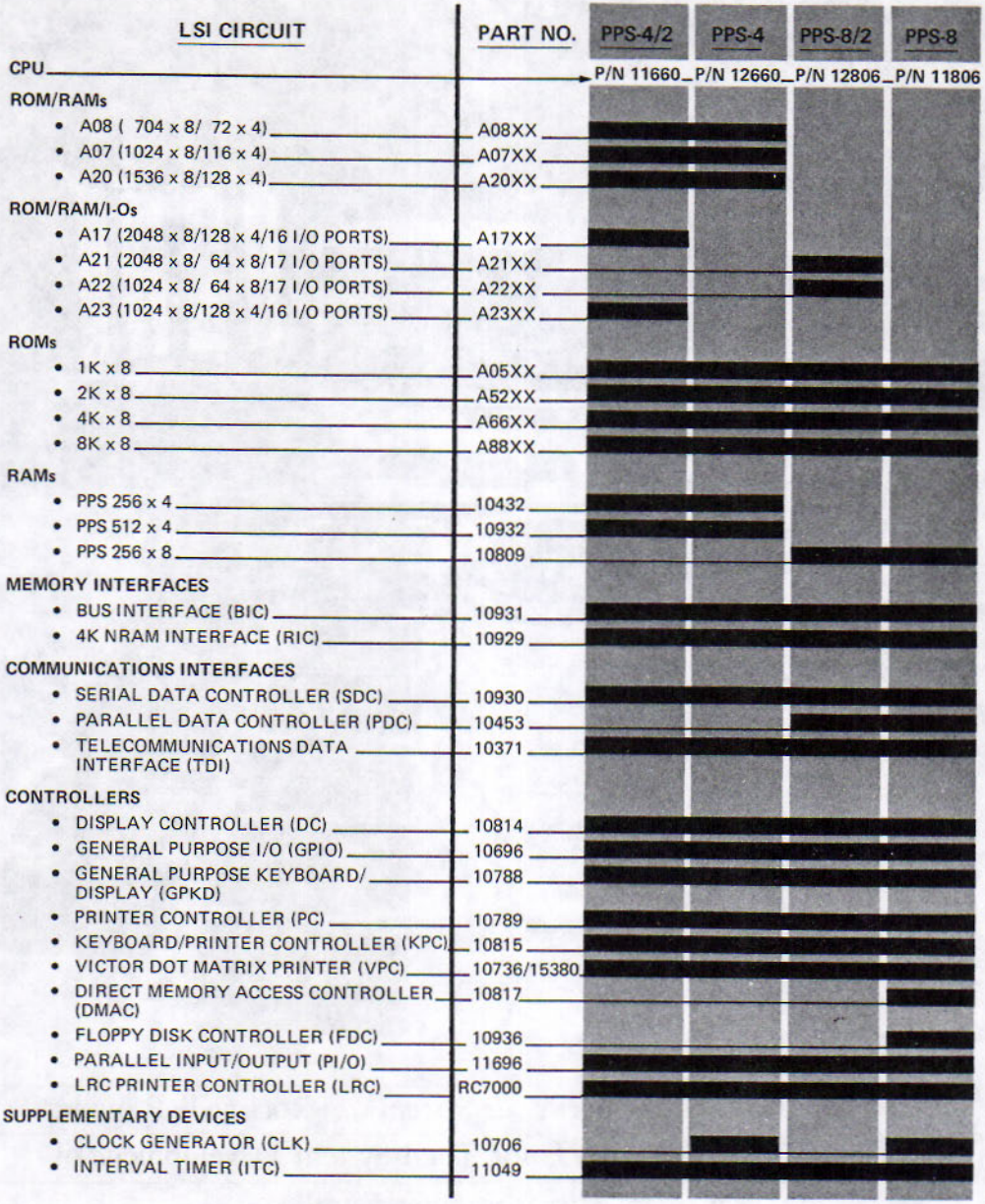
| LRC | **LRC PRINTER CONTROLLER.** On one chip, all logic and encoded ROM to generate 64, single or double width, 5x7 ASCII code characters in maximum lines of 40 characters. Provides single or multiple paper feeds with forward and reverse option. $T^2L$ and CMOS compatible. Optional parallel or serial interface to a host system provided. | RC7000 |

## The Compatibility of LSI Circuit Options Verifies The Built-In Expandability of Rockwell Microcomputer Families




Select What You Need for Your System ... Rockwell Provides All Documents/Design Aids for Total System Development of All of Its Microcomputer Families

# Rockwell Microcomputer Design/Development Aids Fit Your Real World Where Meeting Cost and Marketing Goals Is The Critical Design Issue

Rockwell backs its system-oriented microprocessor families with total system support - - - complete, easily understood documentation, time-saving assemulators or assembler software for program assembly, debug and checkout; evaluation modules and prototype chips for field testing. . .everything designed to speed your design cycle and cut your design costs.

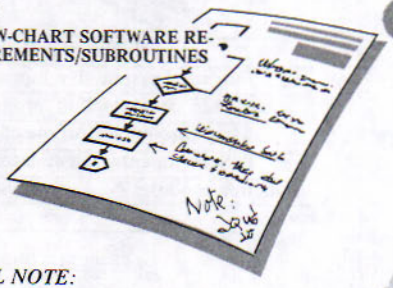
Steps in *Your Equipment Design*

**STEP 1.** **COMPILE YOUR EQUIPMENT FUNCTIONAL SPECIFICATION**

**STEP 2.** **BLOCK-DIAGRAM THE MOST COST-EFFECTIVE PPS SYSTEM**

Rockwell's Product Descriptions, Programmers' Manuals and Electrical/Mechanical Specifications tell the whole story. And our Applications Engineers are as close as your telephone.

**STEP 3.** **FLOW-CHART SOFTWARE REQUIREMENTS/SUBROUTINES**



**STEP 4.** **ASSEMBLE PROGRAM**

**Option 1:** Purchase PPS-MP UNIVERSAL ASSEMULATOR with appropriate SYSTEM "PERSONALITY" MODULE. . . *see next page.* **This is the most economic, expeditious procedure for most systems.** With an assemulator, you're able to perform total system design/development functions - - - program assembly, debug, verify, real time emulation of prototype system. For field testing of prototypes, you purchase prototype evaluation modules, dumping your assembled program from the assemulator into PROM.

**Option 2:** You can use your own computer by purchasing the appropriate Fortran IV Cross Assembler and Simulator programs.

**Option 3:** You can use PPS development programs on worldwide timeshare systems.

**STEP 5.** **ORDER MASK-ENCODED ROMS**

Your Assemulator automatically provides you with the encoded tape with which Rockwell can develop your ROM mask. Prototype quantities are provided for your pre-production system evaluation.

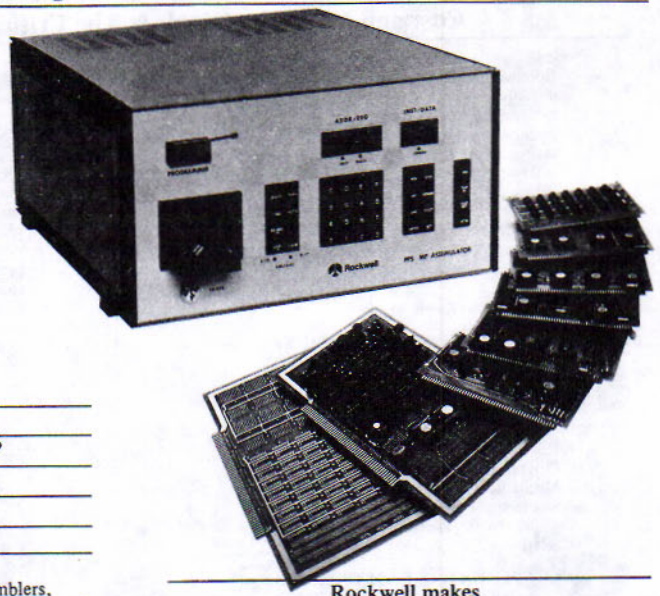
*SPECIAL NOTE:*

***With the purchase of a PPS-MP UNIVERSAL ASSEMULATOR, you can attend, at no charge, a 4-day PPS DESIGNER'S COURSE. Courses are conducted in the U.S.A. in California and New Jersey. In Tokyo, Japan; also in Munich, Germany.***

# The Rockwell PPS MP Universal Assemulator... One Box Does It All:

## Program Assembly... Debug... Emulation... Incoming Device Testing

You save in front-end design aid investment and gain remarkable reductions in design time with the Rockwell PPS MP Universal Assemulator. This specially designed microcomputer has self-contained capabilities to aid your development of programs for all PPS systems. The basic unit is for PPS-8 and 8/2 systems. For others, you simply plug in the appropriate "Personality" module. The Assemulator aids total system development, performing assembly, test, debug, verification, real-time laboratory emulation of prototype system, PROM encoding, ROM mask code generation . . . and you can even use your Assemulator for incoming device testing.



PPS PMOS PRODUCTS

### These Features Tell Why You Want a PPS MP Universal Assemulator in Your Equipment Development Lab

**Powerful Software - -**-Supervisors, Assemblers, Text Editor - for program assembly, debug, lab and prototype checkout.

**Assembler Features . . .**

- Uses mnemonic codes, symbols, decimals or hexadecimal constants.
- Provides listing of source program statements and resulting object code
- Formats object code for loading and executing on assemulator
- Flags statements with actual or potential errors.

**Utility and Debug Features . . .**

- Set up to 8 breakpoint traps
- Single step operation
- Trace printout of CPU registers
- Selective trace on I/O and branch
- Trace at selected memory addresses
- Examine or change locations in program or data memory; change register contents in CPU
- Read program into RAM; output program from RAM
- Go to address selection
- Provides I/O interface with TTY ASR-33, TI 733-ASR or RS-232C devices.

**Text Editor Features . . .**

- Uses fast searching techniques
- Facilitates inserting, deleting or changing source program statements

**Hardware Options . . .**

- Paper tape reader
- Memory expandable to 32K bytes
- Floppy Disk Operating System

### Rockwell makes your total system development easy . . . from LSI chip selection, program assembly, debug through prototype check-out . . . PPS documents, assemulators, software, evaluation modules - - - Everything's Ready For You

**OBJECT LISTING**

```
P12
0074          SOURCE EQU #0074
                ORG #800
0800 80CF8B   LXI SOURCE
0803 668D     LY
0805 66FFFF   LAI 0
0808 5F       SC
0809 46     BACK RAL
080A 6810     DECY
080C 59       B BACK
080D 53       INCX
080E 75       S
```

**TRACE OF CPU REGISTERS**

```
>GT800  <-- Trace on Branch Command
>080C 01 7A 00 04 0074 05 00 00 3FFF 1F 00
>080C 02 7A 00 03 0074 05 00 00 3FFF 1F 00
>080C 04 7A 00 02 0074 05 00 00 3FFF 1F 00
>080C 08 7A 00 01 0074 05 00 00 3FFF 1F 00
>080C 10 7A 00 00 0074 05 00 00 3FFF 1F 00 >
>  P  A  X  Z  Y   ZX  D  LU LL  LI  S  C  >
```

**Typical Register Trace ...**
**The Rockwell Universal Assemulator Makes Debug Easy!**

## PPS MP Universal Assemulator

**PPS MP UNIVERSAL ASSEMULATOR** — Part Number 19703D13

The PPS MP Universal Assemulator is a microcomputer system which simplifies PPS development procedures. The basic unit provides complete programming, debug and system emulation capabilities for PPS-8 and PPS-8/2 systems. The unit includes 6K of memory (4K program and 2K data), interfaces for both TTY and RS-232C terminals and a front panel featuring a hexadecimal keyboard and display. By installing a "personality module (described below) the user can emulate, program and debug PPS-4, PPS-4/2 or PPS-4/1 systems using the same assemulator.

Assemblers for the PPS product line are furnished to convert source program codes. Comprehensive utility and debug functions are ROM resident to assist in every step of product of product development. A powerful Text Editor is provided to allow easy update of source programs.

## "Personality" Module Options

**PPS-4/1 PERSONALITY MODULE.** The PPS-4 Personality Module provides the circuitry necessary to make PPS MP universal assemulator compatible with PPS-4/1 microcomputer. Utilization of this module along with the universal prototyping module (19703D18) permits development, checkout and emulation of PPS-4/1 (MM76 and MM77) systems. — 19703D40

**PPS-4 PERSONALITY MODULE.** The Personality Module makes the PPS MP universal assemulator compatible with the PPS-4 and PPS-4/2 microcomputer. It permits the development, checkout and emulation of PPS-4 and 4/2 systems. — 19703D41

## Memory Module and Associated Options

**INTERNAL BUS BUFFER MODULE.** One Bus Buffer is required for each 8K of memory when 2K x 8 bit (20180D01) modules are utilized. — 19703D17

**8K NRAM MODULE (for PPS MP Assemulators).** Includes two 4K RAM interface devices, P/N 10929, and sixteen 16-pin 4K RAM, P/N 1604-8P plus logic and switching to accomodate the PPS MP Assemulator. In the assemulator the 8K x 8-bit words (PPS-8) or 8K x 4-bit words (PPS-4) may be used as either data or instruction memory. — 20180D23

**8K NRAM MODULE (w/o RAM devices)** Same as above, but with sockets only for RAM devices. — 20180D25

**PROM PROGRAMMER MODULE.** Contains logic for programming and verifying PROMs via the front panel socket. — 19703D15

## Miscellaneous Options

**PAPER TAPE READER, 120 CPS.** Mounted directly on face of assemulator and includes all interfacing control logic. — 19703D03

**TTY MOD KIT.** Permits use of ASR-33 teletypes with paper tape reader. (Not required with high-speed reader option). Mod Kit is installed in user's TTY. — 19703D12

**SYSTEM ANALYSIS MODULE (SAM).** This option consists of a transmitter and receiver module to extend the assemulator bus for customer use in prototyping. It provides for in circuit emulation and complete testing of systems. — 19703D19

**UNIVERSAL PROTOTYPING MODULE (7 x 12).** This module allows user to prototype to own requirements on a PCB that inserts directly into the PPS MP Assemulator back plane bus. Allows the user to readily interconnect a variety of devices during product development and evaluation. Delivered with three Burndy 42-pin sockets and 200 wire wrap pins. — Part Number 19703D18

**BOARD EXTENDER.** Permits vertical extension of PPS-MP Assemulator modules for free access outside the chassis. — 19703D24

## Processor Evaluation Modules

**PPS-4/1 PROCESSOR MODULE - MM76** Contains A7699 prototyping circuit, two 10931 Bus Interface Circuit (BIC) devices and sockets for four PROM's. — 19703D43-6

**PPS-4/1 PROCESSOR MODULE - MM77** Same as MM76 module above, but has A7799 prototyping circuit. — 19703D43-7

**PPS-4/1 PROCESSOR MODULE - MM78** Same as MM76 module above, but has A7899 prototyping circuit. — 19703D43-8

**PPS-4/2 PROCESSOR MODULE.** Contains PPS-4/2 CPU, clock, two ROM/RAM/I/O chips A17XX, 256 x 4-bit RAM and 32 I/Os, 256 x 4-bit additional scratch pad memory and one GPI/O. — 19703D02

**PPS-4 PROCESSOR MODULE.** Contains PPS-4 CPU, clock, two PPS-4 RAMS (256 x 4-bit data storage) and two GPI/Os (24 discrete inputs plus 24 discrete outputs). — 20102D02

**PPS-8 PROCESSOR MODULE.** Contains PPS-8 CPU, clock, two 256 x 8 RAMS, two Parallel Data Controllers (PDC) providing four parallel 8-bit data paths and a Direct Memory Access Controller (DMAC). — 20180D07

## Memory Evaluation Modules

**PPS-8 RAM MODULE.** Contains eight (256 x 8) PPS-8 RAMs that provide 2K x 8 data storage. May also be configured as 2K x 8 read/write instruction storage for ROM emulation. — 20180D01

**PPS-4 RAM MODULE.** Contains eight PPS-4 RAMs (256 x 4-bit) that provides 2K x 4-bit data storage. May also be configured as 1K x 8 read/write instruction storage for ROM emulation. — 20102D17

**PPS PROM MODULE.** Contains sockets and interface logic for sixteen 256 x 8 PROMs. Provides up to 4K x 8 bytes of data memory or instruction memory. — 20102D63

**PPS ROM MODULE.** Contains sockets and interface logic for eight A05XX or A52XX ROM devices. Provides up to 8K x 8 bytes of instruction memory or 16K x 4 bytes of data memory. — 20102D19

**PPS BUS-TO-TTL INTERFACE MODULE.** Provides two bus interface devices and 30 fanout buffers for interfacing the PPS system to core memory for nonvolatile data storage of TTL RAMs for ROM emulation. — 20102D27

## Input/Output Evaluation Modules

**GPI/O MODULE.** Contains four GPI/O devices and TTL input and output buffers. Provides 48 TTL buffered discrete inputs plus 48 TTL buffered discrete outputs. — 20102D36

**UNIVERSAL PROTOTYPING MODULE.** Allows the user to readily interconnect a variety of devices during product development and evaluation. The module board consists of a 5 x 7 inch plug-in circuit card compatible with PPS System Evaluation and Development Modules. Delivered with three Burndy 42-pin sockets and 200 wire wrap pins. — 20102D55

# Rockwell Microcomputers - Design/Development Aids (con't)

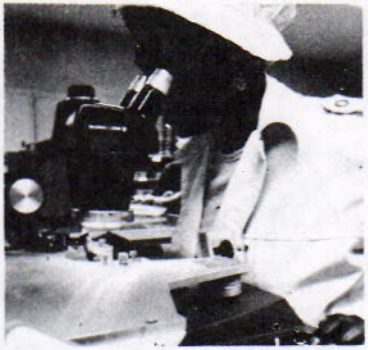
## Software Packages

| | Part Number |
|---|---|
| **PPS-8 CROSS ASSEMBLER - FORTRAN IV.** Programs to convert PPS-8 assembly language to microprocessor machine code. Assembly language is fully symbolic and symbol cross-referencing is provided together with diagnostics of programming errors. Special assembler features are provided to enable efficient use of unique architectural features of the PPS microprocessors. | 19703D20* |
| **PPS-8 SIMULATOR - FORTRAN IV.** Programs to functionally simulate execution of PPS-8 programs. Simulators are interpretive and provide bit-for-bit duplication of microprocessor instruction executing timing, register contents, etc. Direct user control over execution conditions; RAM/register contents, interrupts, I/O data, etc., is provided. | 19703D21* |
| **PPS-4 CROSS ASSEMBLER - FORTRAN IV.** Programs to convert PPS-4 assembly language to microprocessor machine code. Assembly language is fully symbolic and symbol cross-referencing is provided together with diagnostics of programming errors. Special assembler features are provided to enable efficient use of unique architectural features of the PPS microprocessors. | 19703D25* |
| **PPS-4/1 CROSS ASSEMBLER - FORTRAN IV.** Programs to convert PPS-4/1 assembly language to microprocessor machine code. Assembly language is fully symbolic and symbol cross-referencing is provided together with diagnostics of programming errors. Special assembler features are provided to enable efficient use of unique architectural features of the PPS microprocessors. | 19703D51* |

**Each package contains an output format program and is designed to run on 24-bit or greater word length computers.*

## Documentation

| | Part Number |
|---|---|
| **PPS-4 PROGRAMMER'S REFERENCE MANUAL.** Provides a complete description of the PPS-4 microcomputer system as it relates to program development and instruction set usage. This manual is written for designers with little, or no programming background, and explains how to write assembly language programs for the PPS-4 and how to implement those programs in the end product. *Price $5* | 29400N31 |
| **PPS-4 MICROCOMPUTER BASIC DEVICE MANUAL.** Provides a detailed description of each device in the PPS-4 Parallel Processing System family of MOS/LSI chips. The manual includes block diagram analysis of the circuits, pin-outs timing and interface requirements and general characteristics required for system design. *Price $5* | 29003N40 |
| **PPS-4 PROGRAM LIBRARY.** A reference document comprising a compilation of subroutines, initialization procedures and supportive examples for PPS-4 program development. *Price $5* | 29400N33 |
| **PPS-4 TYMSHARE TYMCOM-X SYSTEM OPERATING MANUAL.** This manual provides instructions and reference data to assist designers in the development of computer-aided design (CAD) programs using the TYMCOM-X Systems for PPS-4 Parallel Processing Systems. *Price $5* | 29002N20 |
| **PPS-4 GENERAL ELECTRIC INFORMATION SERVICES OPERATING MANUAL.** This manual provides instructions and reference data to assist designers in the development of computer-aided design (CAD) programs using the General Electric Information Services System for PPS-4 Parallel Processing Systems. *Price $5* | 29004N20 |
| **PPS-8 GENERAL ELECTRIC INFORMATION SERVICES OPERATING MANUAL.** As above, but for PPS-8 Parallel Processing Systems. *Price $5* | 29800N30 |
| **PPS-8 PROGRAMMER'S REFERENCE MANUAL.** Provides a complete description of the PPS-8 Microcomputer System as it relates to program development and instruction set usage. This manual is written for designers with little, or no programming background, and explains how to write assembly language programs for the PPS-8 and how to implement those programs in the end product. *Price $5* | 29800N32 |
| **PPS-8 MICROCOMPUTER BASIC DEVICES MANUAL.** Provides a detailed description of each device in the PPS-8 Parallel Processing System family of MOS/LSI chips. The manual includes block diagram analysis of the circuits, pin-outs, timing and interface requirements and general characteristics required for system design. *Price $5* | 20164N40 |
| **PPS-8 PROGRAM LIBRARY.** A reference document comprising a compilation of subroutines and initialization procedures for PPS-8 program development. *Price $5* | 29800N40 |
| **PPS MP ASSEMULATOR OPERATOR's MANUAL.** This manual provides a detailed description of, and operating procedures for, the PPS MP Assemulator, an invaluable aid to programmers, and equipment designers developing systems using the PPS-8 Parallel Processing System family of devices. *Price $5* | 29800N36 |
| **PPS ELECTRICAL AND MECHANICAL SPECIFICATIONS MANUAL.** This manual describes all physical and electrical specifications of the PPS Family of Parallel Processing System devices. This manual is essential for designers concerned with operating voltages, frequency limits, timing criteria and pin-out allocations in PPS-4 or PPS-8 systems. *Price $5* | 29480N10 |
| **PPS-4/1 OPERATOR'S MANUAL FOR PPS-MP UNIVERSAL ASSEMULATOR.** This manual provides a detailed description of, and operating procedures for the PPS-MP Assemulator when developing systems using the PPS-4/1 family of devices. *Price $5* | 29400N37 |
| **MM76 SERIES MICROCOMPUTER PROGRAMMING MANUAL.** Provides a complete guide to program development for the MM76 series of PPS-4/1 microcomputers, and is written for designers who have little or no programming background. *Price $5* | 29410N44 |
| **MM77, MM78 SERIES MICROCOMPUTER PROGRAMMING MANUAL.** As above, but for the MM77, MM78 series of PPS-4/1 microcomputers. *Price $5* | 29410N38 |
| **XPO-1 USER'S MANUAL.** Full details tell you everything you need to develop PPS-4/1 programs with the XPO-1. *Price $5* | 29410N45 |



## You Can Depend on Rockwell for Microcomputer Circuits and Subassemblies That Match Your Most Demanding Specifications

Rockwell has a 40,000,000-plus annual LSI chip production capacity, covering both PMOS and NMOS products . . . And Rockwell is now delivering thousands of microcomputer devices and modules to meet the production schedules of manufacturers of consumer products and games, automobiles, telephones, commercial and military equipment . . . . . Rockwell, with corporate sales approaching six billion dollars and whose production responsibilities has included programs like NASA's Space Shuttle has the resources and the motivation to meet your microcomputer specifications and requirements . . .



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# PPS

PPS-4/1 One-Chip
Microcomputers

**DOCUMENT NO. 29000 D35**
**P/N A76XX AND A76XXE**

# PARALLEL PROCESSING SYSTEM (PPS)
# DATA SHEET

***PPS-4/1 One-Chip Microcomputer Family***

# MM76 and MM76E

## one-chip microcomputer systems



## SUMMARY

The Rockwell MM76 and MM76E one-chip microcomputers fit the needs of Equipment Designers seeking low-cost systems capable of performing functions in the range of medium complexity. They are distinguished from competitive microprocessors by superior I/O capability, and by other functional features.

The MM76 and MM76E are pin and instruction-set compatible. The MM76E has larger Program Memory (ROM) capacity, making it an easy design step-up if end-product requirements are increased during development based on the MM76.

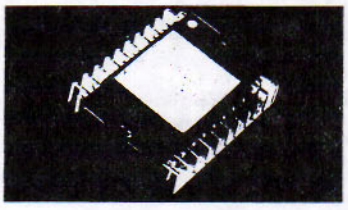
On single LSI chips, the MM76 and MM76E provide complete 4-bit parallel processing systems — versatile Central Processing Unit (CPU), Instruction Decode, one Program Save Register, Program Memory (ROM), Data Memory (RAM), Program Counter (P), Data Address register (B), 10 I/O discrete Drivers/Receivers, two 4-bit parallel I/O channels, two 4-bit parallel Input channels, a Serial I/O port, Interrupt and Control logic, and a self-contained four-phase Clock Generator circuit.

Both microcomputers provide Data Memory (RAM) capacities of 48 4-bit words. Their Program Memory (ROM) capacities are:

| | ROM 8-Bit Bytes | RAM 4-Bit Bytes |
|---|---|---|
| MM76 | 640 | 48 |
| MM76E | 1024 | 48 |

In addition to stand-alone applications, the MM76 and MM76E can be directly included in other multi-chip systems as dedicated controllers or in other functions. Also, two or more MM76 and/or MM76E one-chip microcomputers can be directly combined to perform parallel processing or control operations. In the design of families of end-products, a total range of features can be originally designed so that increasingly higher levels of performance can be produced by low-cost wiring changes and chip additions, minimizing design costs and production inventories.

To facilitate system and program development, Rockwell provides powerful development aids — see under "Features" at right. Typically, a Rockwell-trained Designer can complete an MM76 program in less than four weeks; an MM76E in about four weeks.




**MM76 and MM76E Pin Configuration**

## FEATURES

- MM76 — 640 8-bit bytes of program memory
- MM76E — 1024 8-bit bytes of program memory
- 48 4-bit data words (192 bits)
- Clocked simultaneous serial input/output capability
- Externally controlled serial input/output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and four working registers
- 31 input/output ports
- Large instruction set — over 50 instructions
- Multifunction instructions increase throughput
- Single power supply operation (15 volts ±5%)
- Low power (75 milliwatts typical, 125 milliwatts max)
- Powerful development aids:
  - General Electric Software Assembler
  - Evaluation Module 19703D43-6
  - PPS Universal Assemulator with PPS-4/1 Personality Board for Program and Hardware Development
  - XPO-1 System Development Microcomputer
  - Development Circuit (P/N A7698 for both MM76 and MM76E) provides address and data lines so that Program Memory can be in external PROM or RAM for emulation purposes.
  - Scheduled and Special Training Courses
  - International Applications Engineering Support



**Specifications subject to change without notice**
**Rev. 4, August, 1978**

## FUNCTIONAL DESCRIPTION

### PROGRAM COUNTER (P) and SA REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

### PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides the storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

### INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

### DATA ADDRESS REGISTER (B)

The Data Address Register is 6 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM and the discrete input/output ports are addressed by the 4 bits in BL and the 2 bits in BU.

A number of multifunction instructions simultaneously modify B Upper and cause B Lower to be automatically incremented or decremented and tested for overflow or underflow.

### ACCUMULATOR and ARITHMETIC LOGIC UNIT (A, ALU, and C)

The primary working register in the MM76 is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform either binary or decimal arithmetic. Constants may be loaded into the Accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data.

### CLOCK CONTROL (VC, CLKIN, EXCLK, and OSCILLATOR)

The internal Oscillator and Clock circuit generates a four-Phase A $\overline{B}$ clock signal used for all internal logic functions. The A $\overline{B}$ clock terms are also brought out so external logic can be synchronized. The clock frequency is a nominal 80 kHz ±50%. When precise timing is required, a reference frequency may be input at CLKIN.

### DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 48 4-bit words. Data memory can be used to buffer input or output values, hold intermediate results, or be used as a register for timers, counters, comparators, etc.

### A BUFFER

The contents of the Accumulator or 4 of the bits from the 16 x 8 Decode Matrix may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or the Decode Matrix, or until the power is turned off.

### B BUFFER

The 4-bit B Buffer functions the same as the A Buffer except it outputs the other 4 bits of the 16 x 8 Decode Matrix. The A and B Buffers combined provide the full eight outputs for the Decode Matrix.

### CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port PI1 through PI4 will be loaded into the contents of the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

### CHANNEL 2 INPUT PORTS (PI5 through PI8)

The inverted state of the inputs at parallel input ports PI5 thru PI8 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 3 time) so that asynchronous input signals may be used.

### CHANNEL A I/O PORTS (RI01 through RI04)

The four parallel input/output ports RI01 thru RI04 provide a masked input capability and an output from either the 16 x 8 Decode Matrix or directly from the Accumulator.

### CHANNEL B I/O PORTS (RI05 through RI08)

The four parallel input/output ports of Channel B function the same as the four ports of Channel A. Together, they provide an 8-bit parallel output.

### CONDITIONAL INTERRUPTS (INT0 and INT1)

The conditional interrupts INT0 and INT1 may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized.

### DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O9)

There are ten discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized so that asynchronous input signals may be used.

### 16 X 8 DECODE MATRIX

The Decode Matrix provides a means of decoding the contents of the Accumulator to provide an 8-bit output suitable for driving various displays or other external devices. The user may define any code desired. The Development Circuit version of the MM76 has a BCD to seven segment conversion provided. Accumulator contents of 0 thru F produce 0 thru 9, A, -, P, d, E and blank respectively. The carry flip-flop controls one independent output line.

### S REGISTER – SERIAL INPUT/OUTPUT – SHIFT COUNTER

The S Register is a 4-bit serial-in/serial-out, parallel exchange, register which is used as either an auxiliary storage register or buffer for the simultaneous serial input/output functions. The shift rate can be controlled either internally or externally.

## PPS-4/1 MM76 AND MM76E INSTRUCTION SET

**RAM Addressing Instructions**

| | |
|---|---|
| XAB | Exchange A with BL |
| LBA | Load BL from A |
| LB | Load BU=0, BL=Immediate |
| EOB | Exclusive OR BU |
| LBL | Load B Long |
| INCB | Increment B |
| DECB | Decrement B |

**Bit Manipulation Instructions**

| | |
|---|---|
| SB | Set Bit |
| RB | Reset Bit |
| SKBF | Skip on Bit False |

**Register to Register Instructions**

| | |
|---|---|
| XAS | Exchange A and S |
| LSA | Load S from A |

**Register Memory Instructions**

| | |
|---|---|
| L | Load A from Memory |
| X | Exchange A and Memory |
| XDSK | Exchange A with Memory. Decrement BL and Skip if BL Counts to 15 |
| XNSK | Exchange A with Memory. Increment BL and Skip if BL Counts to 0 |

**Arithmetic Instructions**

| | |
|---|---|
| A | Add Memory to A |
| AC | Add Memory with Carry to A |
| ACSK | Add Memory with Carry to A and Skip on No Carry-out |
| ASK | Add Memory to A and Skip if No Carry Overflow |
| DC | Decimal Correction |
| COM | Complement A |
| RC | Reset Carry |
| SC | Set Carry |
| SKNC | Skip on No Carry |
| LAI | Load A with Immediate Field |
| AISK | Add Immediate and Skip on No Carry-out |

**Logical Comparison Instructions**

| | |
|---|---|
| SKMEA | Skip if Memory Equals A |
| SKBEI | Skip if BL Equals Immediate Field |
| SKAEI | Skip if A Equals Immediate Field |

**Input/Output Instructions**

| | |
|---|---|
| SOS | Set Output Selected |
| ROS | Reset Output Selected |
| SKISL | Skip on Input Selected Low |
| IBM | Input Channel B ANDed with A |
| OB | Output from A to Channel B |
| IAM | Input Channel A ANDed with A |
| OA | Output from A to Channel A |
| IOS | Serial Input/Output |
| I1 | Input Channel 1 |
| I2C | Input Channel 2 and Complement |
| INT1H | Skip if INT1 Input is Low |
| DIN1 | Skip if INT1 Flip-flop is Reset |
| INT0L | Skip if INT0 Input is High |
| DIN0 | Skip if INT0 Flip-flop is Reset |
| SEG1 | Decoder Matrix Output to Channel A |
| SEG2 | Decoder Matrix Output to Channel B |

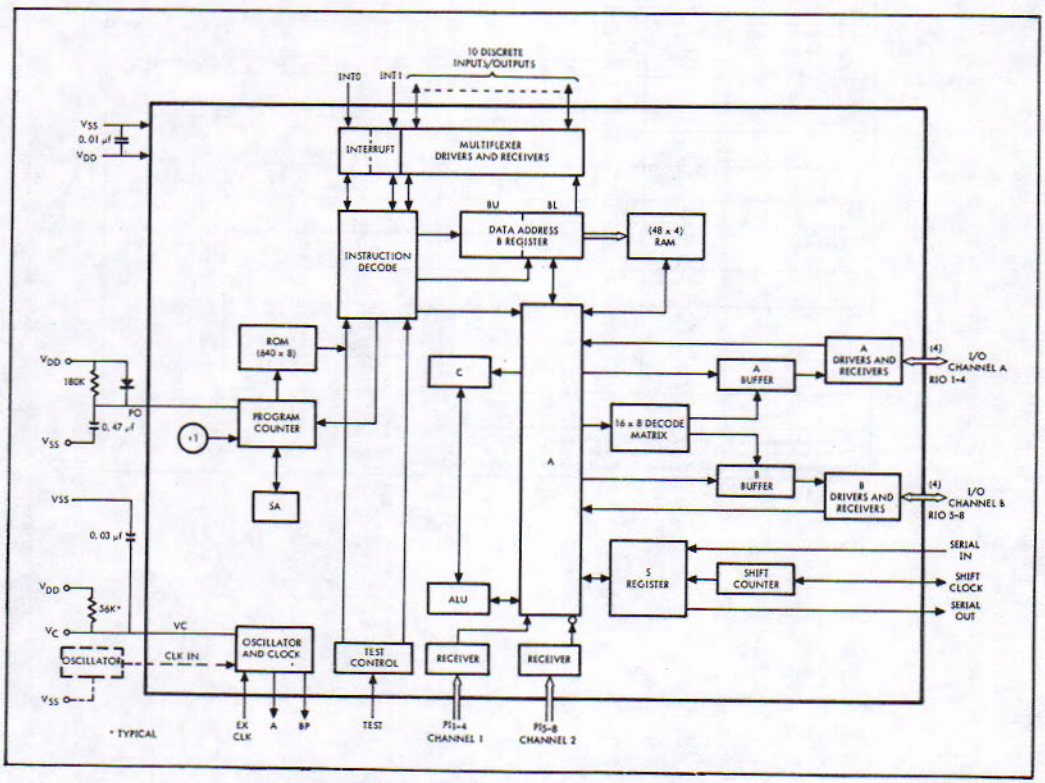
**Conditional Transfer Instructions**

| | |
|---|---|
| TC | Transfer on Carry Set |
| TNC | Transfer on No Carry Set |
| TLC | Transfer Long on Carry Set |
| TLNC | Transfer Long on No Carry Set |
| TBF | Transfer on Bit in Memory False |
| TBT | Transfer on Bit in Memory True |
| TLBF | Transfer Long on Bit in Memory False |
| TLBT | Transfer Long on Bit in Memory True |
| TE | Transfer on A = Memory |
| TNE | Transfer on A ≠ Memory |
| TLE | Transfer Long on A = Memory |
| TLNE | Transfer Long on A ≠ Memory |
| TIH | Transfer if Input High |
| TIL | Transfer if Input Low |
| TLIH | Transfer Long if Input High |
| TLIL | Transfer Long if Input Low |

**ROM Addressing Instructions**

| | |
|---|---|
| RT | Return from Subroutine |
| RTSK | Return and Skip |
| T | Transfer on Page |
| NOP | No Operation |
| TL | Transfer Long |
| TM | Transfer and Mark |
| TML | Transfer and Mark Long |






PPS-4/1 MM76 and MM76E System Block Diagram

# SPECIFICATIONS

## OPERATING CHARACTERISTICS

**Supply Voltage:**

VDD = 15 Volts ±5%
(Logic "1" = most negative voltage $V_{IL}$ and $V_{OL}$.)

VSS = 0 Volts (Gnd.)
(Logic "0" = most positive voltage $V_{IH}$ and $V_{OH}$.)

**System Operating Frequencies:**

80 kHz ±50% with external resistor

**Device Power Consumption:**

75 mw, typical

**Input Capacitance:**

<5 pf

**Input Leakage:**

<10 μa

**Open Drain Driver Leakage (R OFF):**

≤10 μa at -30 Volts

**Operating Ambient Temperature (TA):**

0°C to 70°C (TA = 25°C unless otherwise specified.)

**Storage Temperature:**

-55°C to 120°C

## ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 volts.

Maximum positive voltage on any pin +0.3 volts.

| INPUT/OUTPUT | SYMBOL | LIMITS (VSS = 0) MIN | TYP | MAX | LIMITS (VSS = +5V) MIN | TYP | MAX | TIMING (SAMPLE/GOOD) | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| Supply Current (Average) for VDD | IDD | | 5 ma | 8 ma | | 5 ma | 8 ma | | VDD = -15.75V T = 25°C |
| Discrete I/O's | $V_{IH}$ | -1.0V | | | +4.0V | | | φ34 | |
| DI/O 0-DI/O 9 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| DI/O 0-5 | RON | | | 500 ohms | | | 500 ohms | φ2* | 3.0 ma max. |
| DI/O 6-9 | RON | | | 400 ohms | | | 400 ohms | | |
| Channel 1 Input | $V_{IH}$ | -1.5V | | | +3.5V | | | φ1 | |
| PI1-PI4 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| Channel 2 Input | $V_{IH}$ | -1.5V | | | +3.5V | | | φ3 | |
| PI5-PI8 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| I/O Channel A | $V_{IH}$ | -1.5V | | | +3.5V | | | φ3 | |
| RI/O1-RI/O4 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 250 ohms | | | 250 ohms | φ2* | 6.0 ma max. |
| I/O Channel B | $V_{IH}$ | -1.5V | | | +3.5V | | | φ3 | |
| RI/O5-RI/O8 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 250 ohms | | | 250 ohms | φ2* | 6.0 ma max. |
| DATA I | $V_{IH}$ | -1.0V | | | +4.0V | | | φ4 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| DATA O | RON | | | 500 ohms | | | 500 ohms | φ4** | 3.0 ma max. |
| INT0 | $V_{IH}$ | -1.5V | | | +3.5V | | | φ3 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| INT1 | $V_{IH}$ | -1.5V | | | +3.5V | | | φ1 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| Clock | $V_{OH}$ | -1.0V | | | +4.0V | | | -5.0V | CL = 50 pf (max) |
| A, BP, ($\overline{B}$) | $V_{OL}$ | | | -10.0V | | | -5.0V | | |
| EXCLK | $V_{IH}$ | -1.5V | | | +3.5V | | | -4.0V | F max. = 80 kHz |
| | $V_{IL}$ | | | -9.0V | | | -4.0V | | |
| CLK IN | $V_{IH}$ | -1.0V | | | +4.0V | | | | |
| | $V_{IL}$ | | | -10.0** | | | -5.0V | | |
| Shift Clock | $V_{IH}$ | -1.0V | | | +4.0V | | | φ34 | |
| Clock | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 500 ohms | | | 500 ohms | φ4** | 2.0 ma max. |
| VC*** | $V_{IH}$ | | | | | | | | 56K ±5% |
| | $V_{IL}$ | | | | | | | | |
| FO | $V_{IH}$ | -2.0V | | | +3.0V | | | | Special circuit |
| | $V_{IL}$ | | | -6.0V | | | -1.0V | | |

*State established by φ2 (minimum impedance after φ4).
**Same as above except φ4 minimum at φ2 of next cycle.
***Connect VC to VDD through a resistor: 56KΩ for 80 KHz or 47KΩ for 100 KHz

DOCUMENT NO. 29000 D37
P/N A75XX

Rockwell

# PARALLEL PROCESSING SYSTEM (PPS)
# DATA SHEET

***PPS-4/1 One-Chip Microcomputer Family***

# MM75

## one-chip microcomputer system



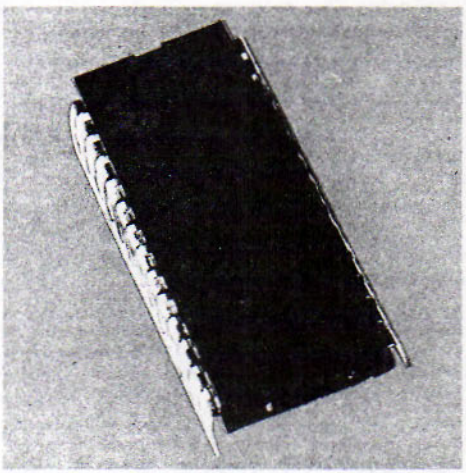
## SUMMARY

The Rockwell MM75 one-chip microcomputer is primarily designed to fit the lowest cost requirements of equipment designers. But in addition to cost advantage, it provides system functions not presently available in competitive microprocessors.

On a single LSI chip, the MM75 provides a complete 4-bit parallel microcomputer system — versatile Central Processing Unit (CPU), Instruction Decode, One Program Save register, Program Memory (ROM), Data Memory (RAM), Program Counter (P), Data Address Register (B), nine input/output discrete drivers/receivers, two 4-bit parallel input/output channels, one 4-bit parallel input channel, Interrupt and Control logic, and a self-contained Clock Generator circuit.

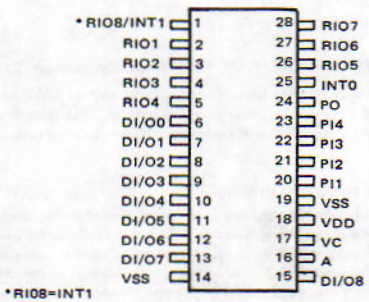
In addition to stand-alone system applications, the MM75 can be directly included in other multi-chip systems as a dedicated slave controller.

To facilitate system and program development, Rockwell provides powerful development aids — see under "Features" at right. Typically, a Rockwell trained designer can complete an MM75 program in about 4 weeks. The MM75 has the same instruction set as the MM76. Therefore the MM76 development circuit is used to support MM75 prototype and program development.



## FEATURES

- 640 8-bit bytes of program memory (5120 bits)
- 48 4-bit data words (192 bits)
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and four working registers
- 22 input/output ports
- Large instruction set — over 50 instructions
- Multifunction instructions increase throughput
- Single power supply operation (15 volts ±5%)
- Low power (75 milliwatts typical, 125 milliwatts max)
- 28-pin, dual-in-line package
- Powerful development aids:
  - General Electric Software Assembler
  - Evaluation Module 19703D43-6
  - PPS Universal Assemulator with PPS-4/1 Personality Board for Program and Hardware Development
  - XPO-1 System Development Microcomputer
  - Development Circuit (P/N A7698) provides address and data lines so that the Program Memory can be in external PROM or RAM for emulating the MM75.
  - Scheduled and Special Training Courses
  - International Applications Engineering Support




**PPS-4/1 MM75 Pin Configuration**



Specifications subject to change without notice
Rev. 2, August, 1978

## FUNCTIONAL DESCRIPTION

### PROGRAM COUNTER (P) and SA REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

### PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides the storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

### INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

### DATA ADDRESS REGISTER (B)

The Data Address Register is 6 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM and the discrete input/output ports are addressed by the 4 bits in BL and the 2 bits in BU.

A number of multifunction instructions simultaneously modify B Upper and cause B Lower to be automatically incremented or decremented and tested for overflow or underflow.

### S REGISTER

The S Register is a 4-bit register which is used as a working register or an auxiliary storage register to the Accumulator. It can be used as a temporary storage register executing the XAS instruction.

### ACCUMULATOR and ARITHMETIC LOGIC UNIT (A, ALU, and C)

The primary working register in the MM75 is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform either binary or decimal arithmetic. Constants may be loaded into the Accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel input or output data.

### CLOCK CONTROL (VC, OSCILLATOR)

The internal Oscillator and Clock circuit generates a four-Phase clock signal used for all internal logic functions. The A clock term is also brought out so external logic can be synchronized. The clock frequency is a nominal 80 kHz ±50%.

### DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 48 4-bit words. Data memory can be used to buffer input or output values, hold intermediate results, or be used as a register for timers, counters, comparators, etc.

### A BUFFER

The contents of the Accumulator or 4 of the bits from the 16 x 8 Decode Matrix may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or the Decode Matrix, or until the power is turned off.

### B BUFFER

The 4-bit B Buffer functions the same as the A Buffer except it outputs the other 4 bits of the 16 x 8 Decode Matrix. The A and B Buffers combined provide the full eight outputs for the Decode Matrix.

### CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port PI1 through PI4 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

### CHANNEL A I/O PORTS (RI01 through RI04)

The four parallel input/output ports RI01 thru RI04 provide a masked input capability and an output from either the 16 x 8 Decode Matrix or directly from the Accumulator.

### CHANNEL B I/O PORTS (RI05 through RI08)

The four parallel input/output ports of Channel B function the same as the four ports of Channel A. Together, they provide an 8-bit parallel output. RI08 also has the capability to be used as a conditional interrupt (INT1).

### CONDITIONAL INTERRUPTS (INT0 and OPTIONAL INT1)

The conditional interrupts INT0 and RI08 (INT1) may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized with INT0 sampled at phase 3 and RI08 sampled at phase 1.

The conditional interrupts (edge detect) input lines in the PPS-4/1 family are very useful. Because of pinpoint limitation, the INT1 is incorporated in the RI08 line. The RI08 line can be used in two ways as part of the parallel I/O Channel B or as the INT1 line. When used as an interrupt line, RI08 will respond to the INT1H and DIN1 commands. When used as part of the bidirectional I/O Channel B, it is controlled with the IBM, OB and the SEG2 instructions.

### DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O8)

There are nine discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized so that asynchronous input signals may be used.

### 16 X 8 DECODE MATRIX

The Decode Matrix provides a means of decoding the contents of the Accumulator to provide an 8-bit output suitable for driving various displays or other external devices. The user may define any code desired. The Development Circuit version of the MM76 has a BCD to seven segment conversion provided. Accumulator contents of 0 thru F produce 0 thru 9, A, -, P, d, E and blank respectively. The carry flip-flop controls one independent output line.

## PPS-4/1 MM75 INSTRUCTION SET

**RAM Addressing Instructions**

| | |
|---|---|
| XAB | Exchange A with BL |
| LBA | Load BL from A |
| LB | Load BU=0, BL=Immediate |
| EOB | Exclusive OR BU |
| LBL | Load B Long |
| INCB | Increment B |
| DECB | Decrement B |

**Bit Manipulation Instructions**

| | |
|---|---|
| SB | Set Bit |
| RB | Reset Bit |
| SKBF | Skip on Bit False |

**Register to Register Instructions**

| | |
|---|---|
| XAS | Exchange A and S |
| LSA | Load S from A |

**Register Memory Instructions**

| | |
|---|---|
| L | Load A from Memory |
| X | Exchange A and Memory |
| XDSK | Exchange A with Memory. Decrement BL and Skip if BL Counts to 15 |
| XNSK | Exchange A with Memory. Increment BL and Skip if BL Counts to 0 |

**Arithmetic Instructions**

| | |
|---|---|
| A | Add Memory to A |
| AC | Add Memory with Carry to A |
| ACSK | Add Memory with Carry to A and Skip on No Carry-out |
| ASK | Add Memory to A and Skip on no Carry-out |
| DC | Decimal Correction |
| COM | Complement A |
| RC | Reset Carry |
| SC | Set Carry |
| SKNC | Skip on No Carry |
| LAI | Load A with Immediate Field |
| AISK | Add Immediate and Skip on No Carry-out |

**Logical Comparison Instructions**

| | |
|---|---|
| SKMEA | Skip if Memory Equals A |
| SKBEI | Skip if BL Equals Immediate Field |
| SKAEI | Skip if A Equals Immediate Field |

**Input/Output Instructions**

| | |
|---|---|
| SOS | Set Output Selected |
| ROS | Reset Output Selected |
| SKISL | Skip on Input Selected Low |
| IBM | Input Channel B ANDed with A |
| OB | Output from A to Channel B |
| IAM | Input Channel A ANDed with A |
| OA | Output from A to Channel A |
| I1 | Input Channel 1 |
| INT1H | Skip if INT1 Input (RI08) is Low |
| DIN1 | Skip if INT1 Flip-flop is Reset |
| INT0L | Skip if INT0 Input is High |
| DIN0 | Skip if INT0 Flip-flop is Reset |
| SEG1 | Decoder Matrix to Channel A |
| SEG2 | Decoder Matrix to Channel B |

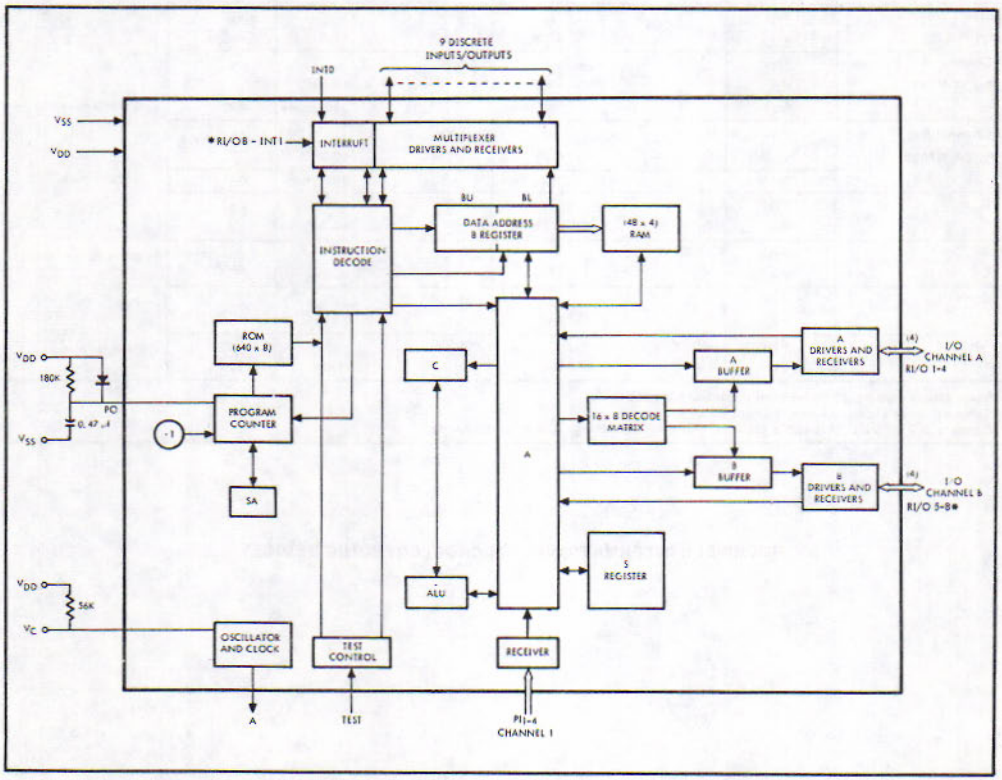
**Conditional Transfer Instructions**

| | |
|---|---|
| TC | Transfer on Carry Set |
| TNC | Transfer on No Carry Set |
| TLC | Transfer Long on Carry Set |
| TLNC | Transfer Long on No Carry Set |
| TBF | Transfer on Bit in Memory False |
| TBT | Transfer on Bit in Memory True |
| TLBF | Transfer Long on Bit in Memory False |
| TLBT | Transfer Long on Bit in Memory True |
| TE | Transfer on A = Memory |
| TNE | Transfer on A ≠ Memory |
| TLE | Transfer Long on A = Memory |
| TLNE | Transfer Long on A ≠ Memory |
| TIH | Transfer if Input High |
| TIL | Transfer if Input Low |
| TLIH | Transfer Long if Input High |
| TLIL | Transfer Long if Input Low |

**ROM Addressing Instructions**

| | |
|---|---|
| RT | Return from Subroutine |
| RTSK | Return and Skip |
| T | Transfer on Page |
| NOP | No Operation |
| TL | Transfer Long |
| TM | Transfer and Mark |
| TML | Transfer and Mark Long |






PPS-4/1 MM75 System Block Diagram

## SPECIFICATIONS

### OPERATING CHARACTERISTICS

Supply Voltage:

VDD = 15 Volts ±5%
(Logic "1" = most negative voltage $V_{IL}$ and $V_{OL}$.)

VSS = 0 Volts (Gnd.)
(Logic "0" = most positive voltage $V_{IH}$ and $V_{OH}$.)

System Operating Frequencies:

80 kHz ±50% with external resistor

Device Power Consumption:

75 mw, typical

Input Capacitance:

<5 pf

Input Leakage:

<10 μa

Open Drain Driver Leakage (R OFF):

≤10 μa at -30 Volts

Operating Ambient Temperature (TA):

0°C to 70°C (TA = 25°C unless otherwise specified.)

Storage Temperature:

-55°C to 120°C

### ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 volts.

Maximum positive voltage on any pin +0.3 volts.

| INPUT/OUTPUT | SYMBOL | LIMITS (VSS = 0) MIN | TYP | MAX | LIMITS (VSS = +5V) MIN | TYP | MAX | TIMING (SAMPLE/ GOOD) | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| Supply Current (Average) for VDD | IDD | | 5 ma | 8 ma | | 5 ma | 8 ma | | VDD = -15.75V T = 25°C |
| Discrete I/O's | $V_{IH}$ | -1.0V | | | +4.0V | | | φ34 | |
| DI/O 0-DI/O 8 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| DI/O 0-5 | RON | | | 500 ohms | | | 500 ohms | φ2* | 3.0 ma max. |
| DI/O 6-8 | RON | | | 400 ohms | | | 400 ohms | | |
| Channel 1 Input | $V_{IH}$ | -1.5V | | | +3.5V | | | φ1 | |
| PI1-PI4 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| I/O Channel A | $V_{IH}$ | -1.5V | | | +3.5V | | | φ3 | |
| RI/O1-RI/O4 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 250 ohms | | | 250 ohms | φ2* | 6.0 ma max. |
| I/O Channel B | $V_{IH}$ | -1.5V | | | +3.5V | | | φ3 | |
| RI/O5-RI/O8 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 250 ohms | | | 250 ohms | φ2* | 6.0 ma max. |
| INT0 | $V_{IH}$ | -1.5V | | | +3.5V | | | φ3 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| Clock | $V_{OH}$ | -1.0V | | | +4.0V | | | -5.0V | CL = 50 pf (max) |
| A | $V_{OL}$ | | | -10.0V | | | -5.0V | | |
| VC*** | $V_{IH}$ | | | | | | | | 56K ±5% |
| | $V_{IL}$ | | | | | | | | |
| PO | $V_{IH}$ | -2.0V | | | +3.0V | | | | Special circuit |
| | $V_{IL}$ | | | -6.0V | | | -1.0V | | |

*State established by φ2 (minimum impedance after φ4).
**Same as above except φ4 minimum at φ2 of next cycle.
*** Connect VC to VDD through a resistor: 56KΩ for 80KHz or 47KΩ for 100 KHz.

DOCUMENT NO. 29000 D46
P/N A79XX

Rockwell

# PARALLEL PROCESSING SYSTEM (PPS)
# DATA SHEET

***PPS-4/1 One-Chip Microcomputer Family***

# MM76C

**one-chip microcomputer with high speed counter**



## SUMMARY

The Rockwell MM76C one-chip microcomputer is a complete 4-bit parallel processing system — CPU, ROM, RAM, I/O. It features a programmable 16-bit, 1-MHz-input, high-speed up/down counter which can be configured in 14 different modes.

The functional versatility and economics of the Rockwell MM76 family of one-chip microcomputers are made easily available to Designers through the commonality of their instruction sets. Designing with the MM76C involves only two new instructions, but these are based on existing codes within the identical instruction sets of the MM76 and MM76E.

For the MM76C, the functions of MM76 instructions SEG 1 and SEG 2 are combined into a single SEG 1 instruction that outputs 8 bits from the Decode Matrix into Channel A and Channel B. MM76C instruction SEG 2 is new, but it uses the MM76 operating code. The new MM76C SEG 2 instruction initiates the Counter Mode of operation. When in the Counter Mode, four of the I/O instructions perform additional functions which are used to program the MM76C to perform a variety of counter/shift register operations.

The 14 different Counter Modes available to the MM76C designer are detailed in the Counter Operation table. Basic Counter Mode configurations are:

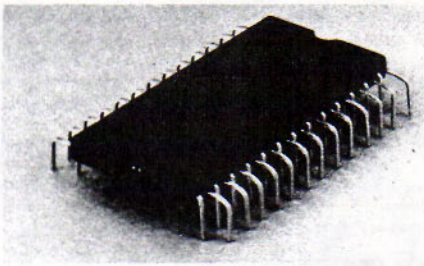
- One 16-bit counter and associated data holding registers
- Two 8-bit counters and associated data holding registers
- Two 8-bit counters with one 8-bit data holding register and one 8-bit shift register

The MM76C 4-bit parallel processing system provides a versatile Central Processing Unit (CPU), Instruction Decode, One Program Save Register, Program Memory (ROM), Data Memory (RAM), Program Counter (P), Data Address Register (B), ten I/O discrete Drivers Receivers, two 4-bit parallel I/O channels, A Serial I/O port, Interrupt and Control logic, and a clock circuit which will accept external clock inputs or generate the clock internally and provide a clock signal output for synchronization.

In addition to stand-alone applications, the MM76C can be directly included in other multi-chip systems as a dedicated controller. Also, two or more MM76C and/or MM76 one-chip microcomputers can be directly combined to perform parallel processing or control operations. In the design of families of end-products, a total range of features can be originally designed so that increasingly higher levels of performance can be produced by low-cost wiring changes and chip additions, minimizing design costs and production inventories.

The 14 modes in which the counters can operate makes this device especially adaptable to use in Motor Control and Scale applications. Other excellent applications are: Frequency Counters, Timers, Synthesizers, Digital-to-Analog Converters, Analog-to-Digital Converters, and Open or Closed Loop Control Systems.

To facilitate system and program development, Rockwell provides powerful development aids — see under "Features."



## FEATURES

- High Speed Counter with the following features:
  - Programmable to function as one 16-bit counter or as two independent 8-bit counters
  - Operates in two input modes: Event input up/down and quadrature input up/down
  - Count up or down at up to 1 MHz rate under external control
  - Multiple programmable operating modes
  - Automatic preset operation
  - Serial 8-bit input/output option
- 37 input/output lines
- 640 8-bit bytes of program memory
- 48 4-bit data words (192 bits)
- Clocked simultaneous serial input/output capability
- Externally controlled serial input/output capability
- Two interrupt request input lines
- TTL and CMOS Interface compatibility
- Arithmetic logic unit and four working registers
- Three modes of clock operation (external crystal input for precision clock frequency)
- Large instruction set — over 50 instructions
- Multifunction instructions to increase throughput
- Single power, supply operation (15 volts ±5%)
- Low power (200 milliwatts typical)
- Powerful development aids:
  - General Electric Software Cross Assembler
  - PPS Universal Assemulator with PPS-4/1 Personality Modules for Program and Hardware Development
  - XPO-1 System Development Microcomputer
  - Development Circuit (P/N A7999) provides address and data lines so that Program Memory can be in external PROM or RAM for emulation purposes
  - Scheduled and Special Training Courses
  - International Applications Engineering Support



Specifications subject to change without notice
Rev. 1, August, 1978

## FUNCTIONAL DESCRIPTION

### PROGRAM COUNTER (P) and SA REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

### PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides the storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

### INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers. arithmetic operations, other processing functions and input/output operations.

### DATA ADDRESS REGISTER (B)

The Data Address Register is 6 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM and the discrete input/output ports are addressed by the 4 bits in BL and the 2 bits in BU.

A number of multifunction instructions simultaneously modify B Upper and cause B Lower to be automatically incremented or decremented and tested for overflow or underflow.

### ACCUMULATOR and ARITHMETIC LOGIC UNIT (A, ALU, and C)

The primary working register in the MM76 is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform either binary or decimal arithmetic. Constants may be loaded into the Accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data.

### DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 48 4-bit words. Data memory can be used to buffer input or output values, hold intermediate results, or be used as a register for timers, counters, comparators, etc.

### A BUFFER and B BUFFER

The contents of the Accumulator or 8 bits from the 16 x 8 Decode Matrix may be output for control, display, or data transfer functions through the A and B Buffers. The A and B Buffers hold the data for output until new data is received from the accumulator or the Decode Matrix, or until the power is turned off.

### CHANNEL 1 INPUT PORTS (PI1-PI4)

The parallel input port PI1 through PI4 will be loaded into the contents of the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

### CHANNEL 2 INPUT PORTS (PI5-PI8)

The inverted state of the inputs at parallel input ports PI5 thru PI8 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 3 time) so that asynchronous input signals may be used.

### CHANNEL A I/O PORTS (RI/O1-RI/O4)

The four parallel input/output ports RI/O1 thru RI/O4 provide a masked input capability and an output from either the 16 x 8 Decode Matrix or directly from the Accumulator.

### CHANNEL B I/O PORTS (RI/O5-RI/O8)

The four parallel input/output ports of Channel B function the same as the four ports of Channel A. Together, they provide an 8-bit parallel output.

### CONDITIONAL INTERRUPTS (INT0 and INT1)

The conditional interrupts INT0 and INT1 may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized.

### DISCRETE INPUT/OUTPUT PORTS (DI/O0-DI/O9)

There are ten discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized so that asynchronous input signals may be used.

### 16 X 8 DECODE MATRIX

The Decode Matrix provides a means of decoding the contents of the Accumulator to provide an 8-bit output suitable for driving various displays or other external devices. The user may define any code desired. The Development Circuit version of the MM76C has a BCD to seven segment conversion provided. Accumulator contents of 0 thru F produce 0 thru 9, A, -, P, d, E and blank respectively. The carry flip-flop controls one independent output line.

### S REGISTER – SERIAL INPUT/OUTPUT – SHIFT COUNTER

The S Register is a 4-bit serial-in/serial-out, parallel exchange, register which is used as either an auxiliary storage register or buffer for the simultaneous serial input/output functions. The shift rate can be controlled either internally or externally.

### CLOCK CONTROL, (XTLIN, XTLOUT, XPWR, and OSCILLATOR)

The MM76C has three selectable modes of clock operation. These modes are:

1. A, BP Mode (Slave). In this mode the MM76C accepts A and BP clock inputs from an external source.
2. Internal Oscillator Mode. In this mode the MM76C generates the A and BPclocks for its own use and also outputs them for use in synchronizing other devices. Provides a 100 kHz ±40% clock.
3. Crystal Driven Mode. This mode allows an external crystal to drive the MM76C clock circuits and is used where precision timing is required. Designed to interface a color TV 3.57 MHz crystal which is divided down to produce a 89 kHz clock.

### HIGH SPEED COUNTER CIRCUITS

#### Control Flip-Flops

The Control Flip-Flops (CR1, CR2, and CR3), in combination with the Control Register, set up the logic to control counter operation. The initial SEG 2 instruction sets the Control Flip-Flops to the Counter Mode which starts counter operation.

### Control Register

The Control Register is a 4-bit register, which combined with the Control Flip-Flops, sets up the logic to control the function and configuration of the Upper and Lower Counters and associated Data Registers. The control word is shifted into the Control Register through the external input C/DI, either from an external source or the output from the S Register.

### Lower Counter and Input Logic

The Input Logic network, under control of the Control Register, controls the inputs to the least significant digit (LSD) position of the Lower Counter. The Lower Counter is an 8-bit bi-directional, high speed counter capable of accepting event inputs at 1 MHz rates. Under program control the data (count) in the Lower Counter can be parallel transferred to the Lower Data Register without disturbing or interrupting the Lower Counter. In addition, the Lower Counter may be logically connected in series with the Upper Counter to form a 16-bit counter.

The Lower Counter can operate in either of two input modes designated Event input and Quadrature input. When in the Event mode the Input Logic sets the Lower Counter to count on the leading edge of each positive going pulse input at PC1, and can count at up to 1 MHz rates. The counter will count up or down depending on the input at PC2. When in the Quadrature mode the Input Logic accepts and decodes the phase relationship of two similar signals, one of which is input at PC1 and the other input at PC2. These two signals are out of phase by 90 degrees and the counter will count up or down depending on which signal is leading. In the Quadrature mode the counter counts each transition of both inputs, and can count at up to 250 kHz on each input.

### Upper Counter

The Upper Counter is an 8-bit, bi-directional counter which may be preset with data from the Upper Data Register. The Upper Counter, under program control, will accept event input from the Lower Counter carry out or from an external input at a frequency not exceeding one-half the clock frequency. As with the Lower Counter, the data in the Upper Counter can be parallel transferred to the Upper Data Register without disturbing or interrupting the Upper Counter.

The ability to be preset to any desired data allows the Upper Counter to generate an overflow or carry out after any predetermined number of event inputs. When in this mode the Upper Counter will automatically be preset with the same value after each overflow.

### Lower Data Register

The Lower Data Register is an 8-bit latching register which will accept and hold data from the Lower Counter under program control. Data in the Lower Data Register can be transferred to the Accumulator 4 bits at a time under program control. Data latched into the Lower Data Register is retained until new data is parallel transferred in from the Lower Counter or until a new power on sequence is initiated.

### Upper Data Register

The Upper Data Register is similar to Lower Data Register but has two additional functions. The Upper Data Register can parallel transfer its data to the Upper Counter as well as receive data from the Upper Counter. In addition, under program control the Upper Data Register can function as an 8-bit shift register and receive data from an external source via the CD/I input using the SCC/D shift clock.

Data in the Upper Data Register may be shifted out through the Upper Carry Flip-Flop to CA16/D output. As with the Lower Data Register, the data in the Upper Data Register can transfer to the Accumulator 4-bits at a time under program control.



**DESCRIPTION OF THE 14 MODES OF COUNTER OPERATION**

| Mode | Control Reg. 8 | 4 | 2 | 1 | One 16-Bit Ctr | Two 8-Bit Ctr's | UDR is Shift Reg. | Lwr Ctr Input | Upr Ctr Input | Reset By:* Lwr | Reset By:* Upr | Preset Upr Ctr | Up/Down Control Lwr | Up/Down Control Upr | Enable Input Lwr | Enable Input Upr |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | X | | | Q | LC | (1)(2) | (1)(2) | (3) | QPR | LC | U | U |
| 2 | 0 | 0 | 0 | 1 | X | | | Q | LC | (1)(2) | | (3) (4) | QPR | LC | U | U |
| 3 | 0 | 0 | 1 | 0 | X | | | E | LC | (1) (2) | (1) (2) | (3) | PC2 | LC | U | U |
| 4 | 0 | 0 | 1 | 1 | X | | | E | LC | (1) (2) | | (3) (4) | PC2 | LC | U | U |
| 5 | 0 | 1 | 0 | X | X** | | X | Q | | (1) (2) | | | QPR | | U | |
| 6 | 0 | 1 | 1 | X | X** | | X | E | | (1) (2) | | | PC2 | | U | |
| 7 | 1 | 0 | 0 | 0 | | X | | Q | E | (1) | (2) | (3) | QPR | DOWN | U | U |
| 8 | 1 | 0 | 0 | 1 | | X | | Q | E | (1) | | (3) (4) | QPR | DOWN | U | |
| 9 | 1 | 0 | 1 | 0 | | X | | E | E | (1) | (2) | (3) | PC2 | DOWN | U | U |
| 10 | 1 | 0 | 1 | 1 | | X | | E | E | (1) | | (3) (4) | PC2 | DOWN | U | U |
| 11 | 1 | 1 | 0 | 0 | | X | | Q | E | (1) | (2) | (3) | QPR | UP | U | U |
| 12 | 1 | 1 | 0 | 1 | | X | | Q | E | (1) | | (3) (4) | QPR | UP | U | |
| 13 | 1 | 1 | 1 | 0 | | X | | E | E | (1) | (2) | (3) | PC2 | UP | U | U |
| 14 | 1 | 1 | 1 | 1 | | X | | E | E | (1) | | (3) (4) | PC2 | UP | U | U |

*Both Lower and Upper Counters and Data Registers are reset by POI, and Control Register is forced to Mode 1.
**In Modes 5 and 6, since the UDR is functioning as a Serial Shift Register, only the LC can be read. If UC needs to be read, exit Mode 5 or 6 and enter Mode 1, 2, 3, or 4.
***IAM (CR1 + CR2) resets UDR.
(1) = (Inst. IAM) CR1
(2) = (Inst. IAM) CR2
(3) = (Inst. IBM) (CR1 + CR2)
(4) = Automatic Preset, (UDR → UC)

UDR = Upper Data Register
Q = Quadrature Input
E = Event Input
LCC = Carry from Lower Counter

UCC = Carry from Upper Counter
D = Down (count down)
U = Up (count up)
QPR = Quadrature phase relationship

## SPECIFICATIONS

**52-PIN IN-LINE SOCKET**

Burndy P/N: DILE-52P1
Burndy Corp., 931 S. Douglas
El Segundo, Calif. 90245

**OPERATING CHARACTERISTICS**

VDD = -15 Volts ±5%
(Logic "1" = most negative voltage $V_{IL}$ and $V_{OL}$)

VSS = 0 Volts (GND)
(Logic "0" = most positive voltage $V_{IH}$ and $V_{OH}$)

System Operating Frequencies:
100 kHz ±40% (internal clock)

Device Power Consumption:
200 mw, typical , INT, EXT, 250 mw, typical, XTAL

Input Capacitance:
<5 pf

Input Leakage:
<10 μa

Open Drain Driver Leakage (R OFF):
≤10 μa at -30 Volts

Operating Ambient Temperature (TA):
0°C to 70°C (TA = 25°C unless otherwise specified)

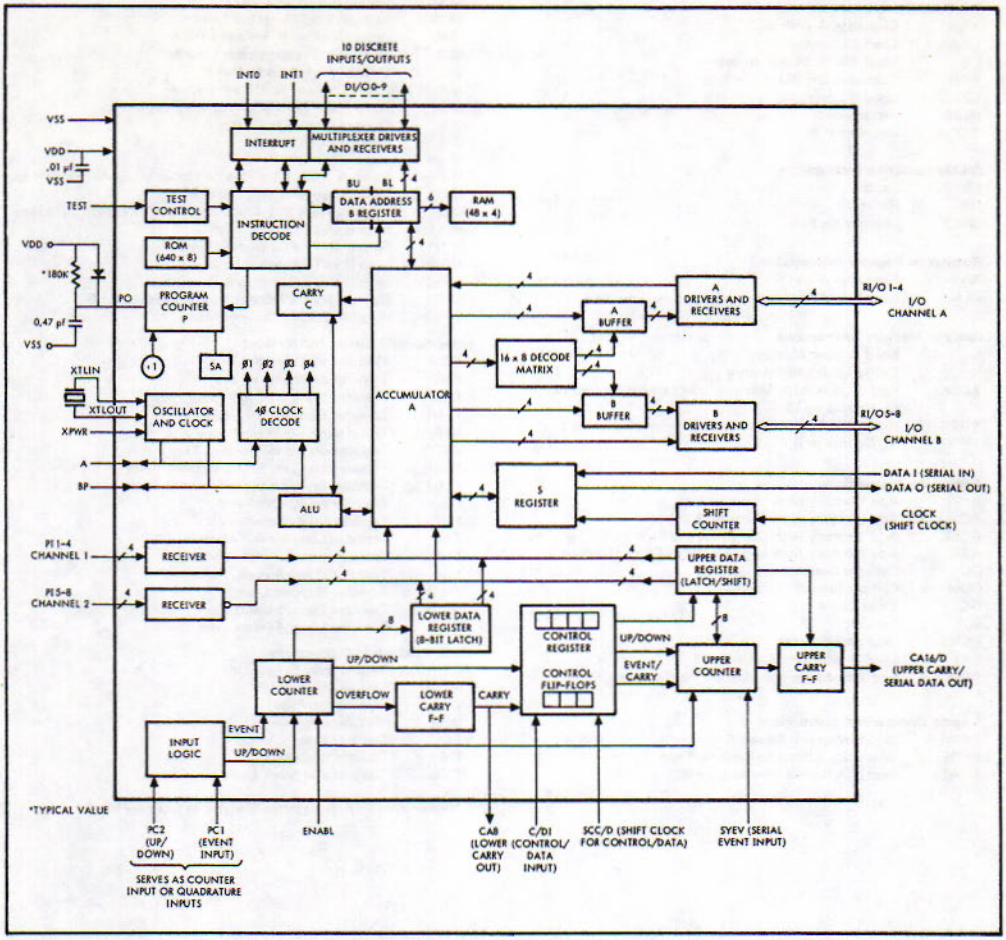
Storage Temperature:
-55°C to 120°C

**ABSOLUTE MAXIMUM VOLTAGE RATINGS**
**(with respect to VSS)**

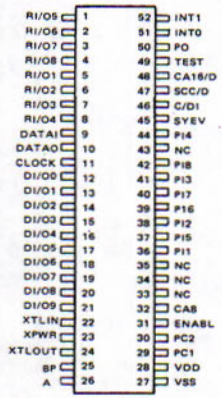
Maximum negative voltage on any pin -30 volts.
Maximum positive voltage on any pin +0.3 volt.

| Input/Output | Symbol | Limits (VSS = 0) Min | Typ | Max | Limits (VSS = +5V) Min | Typ | Max | Timing (Sample/ Good) | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply Current (Average) for VDD | $I_{DD}$ | | 12 ma (INT)<br>16 ma (XTAL) | | | | | | VDD = -15.75V<br>T = 25°C |
| Discrete I/O's<br>DI/O 0-DI/O 9 | $V_{IH}$<br>$V_{IL}$ | -1.0V | | -4.2V | +4.0V | | +0.8V | Ø3 & Ø4 | |
| DI/O 0-5 | $R_{ON}$ | | | 500 ohms | | | 500 ohms | Ø2* | 3.0 ma max. |
| DI/O 6-9 | $R_{ON}$ | | | 400 ohms | | | 400 ohms | | |
| Channel 1 Input<br>PI1-PI4 | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +3.5V | | +0.8V | Ø1 | |
| Channel 2 Input<br>PI5-PI8 | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +3.5V | | +0.8V | Ø3 | |
| I/O Channel A<br>RI/O1-RI/O4 | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +3.5V | | +0.8V | Ø3 | |
| | $R_{ON}$ | * | | 250 ohms | | | 250 ohms | Ø2* | 6.0 ma max. |
| I/O Channel B<br>RI/O5-RI/O8 | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +3.5V | | +0.8V | Ø3 | |
| | $R_{ON}$ | | | 250 ohms | | | 250 ohms | Ø2* | 6.0 ma max. |
| DATAI | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +3.5V | | +0.8V | Ø4 | |
| DATAO | $R_{ON}$ | | | 500 ohms | | | 500 ohms | Ø4** | 3.0 ma max. |
| INT0 | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +3.5V | | +0.8V | Ø3 | |
| INT1 | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +3.5V | | +0.8V | Ø1 | |
| Clock<br>A, BP, ($\overline{B}$) | $V_{OH}$<br>$V_{OL}$ | -1.0V | | -10.0V | +4.0V | | -5.0V | -5.0V | CL ≠ 50 pf (max) |
| XPWR | $V_{IH}$<br>$V_{IL}$ | VSS | | VDD | VSS | | VDD | | |
| XTLIN, XTLOUT | $V_{IH}$<br>$V_{IL}$ | | | | | | | | Crystal<br>3.579 MHz |
| Shift Clock<br>CLOCK | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +3.5V | | +0.8V | Ø3 & Ø4 | |
| | $R_{ON}$ | | | 500 ohms | | | 500 ohms | Ø4** | 2.0 ma max. |
| PO | $V_{IH}$<br>$V_{IL}$ | -2.0V | | -6.0V | +3.0V | | -1.0V | | Special circuit |
| PC1 | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +4.5V | | +0.8V | DC | |
| PC2 | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +4.5V | | +0.8V | DC | |
| CA8 LOWER CARRY OUT | $R_{ON}$ | | | 500 ohms | | | 500 ohms | DC | |
| CA16/D UPPER CARRY SERIAL DATA OUT | $R_{ON}$ | | | 500 ohms | | | 500 ohms | Ø3 & Ø4 | |
| SYEV SERIAL EVENT INPUT | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +3.5V | | +0.8V | Ø3 | |
| SCC/D SHIFT CLOCK CONTROL/DATA | $V_{IH}$<br>$V_{IL}$ | -1.0V | | -10.0V | +4.0V | | +0.8V | Ø3 & Ø4 | |
| C/DI CONTROL/DATA INPUT | $V_{IH}$<br>$V_{IL}$ | -1.0V | | -10.0V | +4.0V | | +0.8V | Ø3 | |
| ENABL | $V_{IH}$<br>$V_{IL}$ | -1.5V | | -4.2V | +3.5V | | +0.8V | DC | |

*State established by Ø2 (minimum impedance after Ø4)
**Same as above except Ø4 minimum at Ø2 of next cycle.




**PPS-4/1 MM76C Block Diagram**




**MM76C Pin Configuration**

## PPS-4/1 MM76C INSTRUCTION SET

**RAM Addressing Instructions**

| | |
|---|---|
| XAB | Exchange A with BL |
| LBA | Load BL from A |
| LB | Load BU=0, BL= immediate |
| EOB | Exclusive OR BU |
| LBL | Load B Long |
| INCB | Increment B |
| DECB | Decrement B |

**Bit Manipulation Instructions**

| | |
|---|---|
| SB | Set Bit |
| RB | Reset Bit |
| SKBF | Skip on Bit False |

**Register to Register Instructions**

| | |
|---|---|
| XAS | Exchange A and S |
| LSA | Load S from A |

**Register Memory Instructions**

| | |
|---|---|
| L | Load A from Memory |
| X | Exchange A and Memory |
| XDSK | Exchange A with Memory. Decrement BL and Skip if BL Counts to 15 |
| XNSK | Exchange A with Memory. Increment BL and Skip if BL Counts to 0 |

**Arithmetic Instructions**

| | |
|---|---|
| A | Add Memory to A |
| AC | Add Memory with Carry to A |
| ACSK | Add Memory with Carry to A and Skip on No Carry-out |
| ASK | Add Memory to A and Skip if No Carry Overflow |
| DC | Decimal Correction |
| COM | Complement A |
| RC | Reset Carry |
| SC | Set Carry |
| SKNC | Skip on No Carry |
| LAI | Load A with Immediate Field |
| AISK | Add Immediate and Skip on No Carry-out |

**Logical Comparison Instructions**

| | |
|---|---|
| SKMEA | Skip if Memory Equals A |
| SKBEI | Skip if BL Equals Immediate Field |
| SKAEI | Skip if A Equals Immediate Field |

**Input/Output Instructions**

| | |
|---|---|
| SOS | Set Output Selected |
| ROS | Reset Output Selected |
| SKISL | Skip on Input Selected Low |
| IBM | Input Channel B ANDed with A |
| *IBM | Same Plus Presets Upper Counter |
| OB | Output from A to Buffer B |
| IAM | Input Channel A ANDed with A |
| *IAM | Same Plus Clears Appropriate Counters |
| OA | Output from A to Buffer A |
| IOS | Serial Input/Output |
| I1 | Input Channel 1 |
| *I1 | Load A from LS 4 bits of Upper or Lower Data Reg. |
| I2C | Input Channel 2 and Complement |
| *I2C | Load A from MS 4 bits of Upper or Lower Data Reg. |
| INT1H | Skip if INT1 Input is High |
| DIN1 | Skip if INT1 Flip-flop is Reset |
| INT0L | Skip if INT0 Input is Low |
| DIN0 | Skip if INT0 Flip-flop is Reset |
| SEG1 | Decode Matrix Output to Channels A and B |
| *SEG2 | Puts MM76C in Counter Mode |

**Conditional Transfer Instructions**

| | |
|---|---|
| TC | Transfer on Carry Set |
| TNC | Transfer on No Carry Set |
| TLC | Transfer Long on Carry Set |
| TLNC | Transfer Long on No Carry Set |
| TBF | Transfer on Bit in Memory False |
| TBT | Transfer on Bit in Memory True |
| TLBF | Transfer Long on Bit in Memory False |
| TLBT | Transfer Long on Bit in Memory True |
| TE | Transfer on A = Memory |
| TNE | Transfer on A ≠ Memory |
| TLE | Transfer Long on A = Memory |
| TLNE | Transfer Long on A ≠ Memory |
| TIH | Transfer if Input High |
| TIL | Transfer if Input Low |
| TLIH | Transfer Long if Input High |
| TLIL | Transfer Long if Input Low |

**ROM Addressing Instructions**

| | |
|---|---|
| RT | Return from Subroutine |
| RTSK | Return and Skip |
| T | Transfer on Page |
| NOP | No Operation |
| TL | Transfer Long |
| TM | Transfer and Mark |
| TML | Transfer and Mark Long |

*Instruction Functions when MM76C in Counter Mode.

DOCUMENT NO. 29000 D49
P/N B76XX AND B86XX

Rockwell

# PARALLEL PROCESSING SYSTEM (PPS)

## DATA SHEET

*PPS-4/1 One-Chip Microcomputer Family*

# MM76L and MM76EL

## low-voltage, low power one-chip microcomputer systems




### SUMMARY

The Rockwell MM76L and MM76EL microcomputers are complete 4-bit parallel processing systems. Both the MM76L and MM76EL are low voltage (6.5 to 11 volt range), very low power (15 milliwatts typical) versions of the well known MM76 one-chip microcomputer. All of the microcomputers in the family of MM76 microcomputers fit the needs of Equipment Designers seeking low-cost systems capable of performing functions in the range of medium complexity. However, the MM76L and MM76EL are especially desirable where low-cost battery operation as the primary or backup power source is required, or where power consumption or heat dissipation is a consideration, or where portability is required. The entire MM76 family of microcomputers is distinguished from competitive microprocessors by superior I/O capability, and by other functional features identified on this page.

The MM76L and MM76EL are pin and instruction-set compatible. The MM76EL has larger Program Memory (ROM) capacity, making it an easy design step-up if end-product requirements are increased during development based on the MM76L.

On single LSI chips, both the MM76L and MM76EL provide complete systems consisting of the following functional areas: a versatile Central Processing Unit (CPU), Instruction Decode, one Program Save Register, Program Memory (ROM), Data Memory (RAM), Program Counter (P), Data Address Register (B), 10 I/O discrete Drivers/Receivers, two 4-bit parallel I/O channels, two 4-bit parallel input channels, a Serial I/O port, Interrupt and Control logic, and a self-contained four-phase Clock Generator circuit.

The Data Memory (RAM) and Program Memory (ROM) capacities are:

| | ROM | RAM |
|---|---|---|
| MM76L | 640 x 8 | 48 x 4 |
| MM76EL | 1024 x 8 | 48 x 4 |

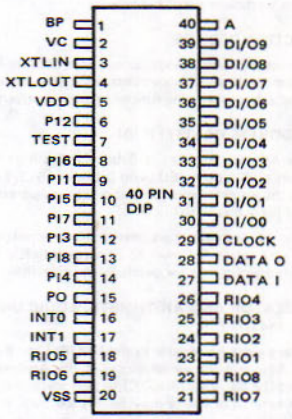
In addition to stand-alone applications, the MM76L and MM76EL can be directly included in other multi-chip systems as dedicated controllers or in other functions. Also, two or more MM76L and/or MM76EL microcomputers can be directly combined to perform parallel processing or control operations. In the design of families of end-products, a total range of features can be designed so that increasingly higher levels of performance can be produced by low-cost wiring changes and chip additions, minimizing design costs and production inventories.

The MM76L and MM76EL are available in commercial and industrial versions. These versions differ only in their operating temperature ranges, as follows:

$0^{\circ}C$ to $+70^{\circ}C$ (Commercial): MM76L and MM76EL
$-40^{\circ}C$ to $+85^{\circ}C$ (Industrial): MM76L-2 and MM76EL-2


### NEW ELECTRICAL FEATURES

- Battery Compatible (-6.5 to -11.0 volt operation)
- Low Power – 15 milliwatts nominal @ -8.5 volts
- 4 Clock Modes including external crystal
- Low Impedance Drivers
  - DI/O – less than 100 ohm @ 10 ma
  - RIO – less than 250 ohm @ 6 ma
- Mask Programmed Pull-downs on Outputs, (five values)
- Mask Programmed Pull-downs on Inputs




**MM76L and MM76EL Pin Configuration**

### FUNCTIONAL FEATURES

- Software compatible with MM76 and MM76E
- Standard 40-pin Dual-In-Line (DIP) package
- MM76L – 640 8-bit bytes of program memory
- MM76EL – 1024 8-bit bytes of program memory
- 48 4-bit words (192 bits) of data memory
- Clocked simultaneous serial input/output capability
- Externally controlled serial input/output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and four working registers
- 31 input/output ports
- Large instruction set – over 50 instructions
- Multifunction instructions increase throughput
- Single power supply operation (-8.5 volts -2.5, +2.0 volts)
- Low power (15 milliwatts typical, 25 milliwatts max)
- Powerful development aids:
  - General Electric Software Assembler
  - Evaluation Module 19703D43-6
  - PPS Universal Assemulator with PPS-4/1 Personality Board for Program and Hardware Development
  - Development Circuit (P/N B7698 for both MM76L and MM76EL) provides address and data lines so that Program Memory can be in external PROM for emulation purposes.
  - Scheduled and Special Training Courses
  - International Applications Engineering Support



Specifications subject to change without notice
Rev. 1, August, 1978

## FUNCTIONAL DESCRIPTION

### PROGRAM COUNTER (P) and SA REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

### PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides the storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

### INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

### DATA ADDRESS REGISTER (B)

The Data Address Register is 6 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM and the discrete input/output ports are addressed by the 4 bits in BL and the 2 bits in BU.

A number of multifunction instructions simultaneously modify B Upper and cause B Lower to be automatically incremented or decremented and tested for overflow or underflow.

### ACCUMULATOR AND ARITHMETIC LOGIC UNIT (A, ALU, and C)

The primary working register in the MM76 is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform either binary or decimal arithmetic. Constants may be loaded into the Accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data.

### DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 48 4-bit words. Data memory can be used to buffer input or output values, hold intermediate results, or be used as a register for timers, counters, comparators, etc.

### CLOCK CONTROL (VC, XTLIN, XTLOUT, A, and BP)

The internal Oscillator and Clock circuit generates a four-phase A BP clock signal used for all internal logic functions. The A BP clock terms are also brought out so external logic can be synchronized. The clock for the MM76L and MM76EL can be selected to operate in one of four modes as shown by the table below. These options are selected by control voltages applied to the VC and XTLIN pins.

### A BUFFER

The contents of the Accumulator or 4 of the bits from the 16 x 8 Decode Matrix may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or the Decode Matrix, or until the power is turned off.

### B BUFFER

The 4-bit B Buffer functions the same as the A Buffer except it outputs the other 4 bits of the 16 x 8 Decode Matrix. The A and B Buffers combined provide the full eight outputs for the Decode Matrix.

### CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port PI1 through PI4 will be loaded into the contents of the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

### CHANNEL 2 INPUT PORTS (PI5 through PI8)

The inverted state of the inputs at parallel input ports PI5 thru PI8 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 3 time) so that asynchronous input signals may be used.

### CHANNEL A I/O PORTS (RI01 through RI04)

The four parallel input/output ports RI01 thru RI04 provide a masked input capability and an output from either the 16 x 8 Decode Matrix or directly from the Accumulator.

### CHANNEL B I/O PORTS (RI05 through RI08)

The four parallel input/output ports of Channel B function the same as the four ports of Channel A. Together, they provide an 8-bit parallel output.

### CONDITIONAL INTERRUPTS (INT0 and INT1)

The conditional interrupts INT0 and INT1 may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized.

### DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O9)

There are ten discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized so that asynchronous input signals may be used.

### 16 X 8 DECODE MATRIX

The Decode Matrix provides a means of decoding and contents of the Accumulator to provide an 8-bit output suitable for driving various displays or other external devices. The user may define any code desired. The Development Circuit version of the MM76 has a BCD to seven segment conversion provided. Accumulator contents of 0 thru F produce 0 thru 9, A, -, P, d, E and blank respectively. The carry flip-flop controls one independent output line.

### S REGISTER – SERIAL INPUT/OUTPUT – SHIFT COUNTER

The S register is a 4-bit serial-in/serial-out, parallel exchange, register which is used as either an auxiliary storage register or buffer for the simultaneous serial input/output functions. The shift rate can be controlled either internally or externally.

| Mode | Pins | | | | | Frequency |
|---|---|---|---|---|---|---|
| | $V_C$ | XTLIN | XTLOUT | A I/O | BP I/O | |
| INTERNAL | *$V_C$ | VSS | – | OUT | OUT | 100 kHz ±30% @ 8.5V |
| EXTERNAL | GRD | CLOCK | – | OUT | OUT | 400 – 800 kHz @ 8.0V |
| CRYSTAL | GRD | XTAL | XTAL | OUT | OUT | ≈800 kHz @ 8.0V |
| SLAVE | $V_{DD}$ | $V_{DD}$ | – | IN | IN | 100 kHz – 50 kHz @ 8.5V |

*Can be adjusted to vary frequency – Normally set to $V_{DD}$

## PPS-4/1 MM76E AND MM76EL INSTRUCTION SET

**RAM Addressing Instructions**

| | |
|---|---|
| XAB | Exchange A with BL |
| LBA | Load BL from A |
| LB | Load BU=0, BL=Immediate |
| EOB | Exclusive OR BU |
| LBL | Load B Long |
| INCB | Increment B |
| DECB | Decrement B |

**Bit Manipulation Instructions**

| | |
|---|---|
| SB | Set Bit |
| RB | Reset Bit |
| SKBF | Skip on Bit False |

**Register to Register Instructions**

| | |
|---|---|
| XAS | Exchange A and S |
| LSA | Load S from A |

**Register Memory Instructions**

| | |
|---|---|
| L | Load A from Memory |
| X | Exchange A and Memory |
| XDSK | Exchange A with Memory. Decrement BL and Skip if BL Counts to 15 |
| XNSK | Exchange A with Memory. Increment BL and Skip if BL Counts to 0 |

**Arithmetic Instructions**

| | |
|---|---|
| A | Add Memory to A |
| AC | Add Memory with Carry to A |
| ACSK | Add Memory with Carry to A and Skip on No Carry-out |
| ASK | Add Memory to A and Skip if No Carry Overflow |
| DC | Decimal Correction |
| COM | Complement A |
| RC | Reset Carry |
| SC | Set Carry |
| SKNC | Skip on No Carry |
| LAI | Load A with Immediate Field |
| AISK | Add Immediate and Skip on No Carry-out |

**Logical Comparison Instructions**

| | |
|---|---|
| SKMEA | Skip if Memory Equals A |
| SKBEI | Skip if BL Equals Immediate Field |
| SKAEI | Skip if A Equals Immediate Field |

**Input/Output Instructions**

| | |
|---|---|
| SOS | Set Output Selected |
| ROS | Reset Output Selected |
| SKISL | Skip on Input Selected Low |
| IBM | Input Channel B ANDed with A |
| OB | Output from A to Channel B |
| IAM | Input Channel A ANDed with A |
| OA | Output from A to Channel A |
| IOS | Serial Input/Output |
| I1 | Input Channel 1 |
| I2C | Input Channel 2 and Complement |
| INT1H | Skip if INT1 Input is Low |
| DIN1 | Skip if INT1 Flip-flop is Reset |
| INT0L | Skip if INT0 Input is High |
| DIN0 | Skip if INT0 Flip-flop is Reset |
| SEG1 | Decoder Matrix Output to Channel A |
| SEG2 | Decoder Matrix Output to Channel B |

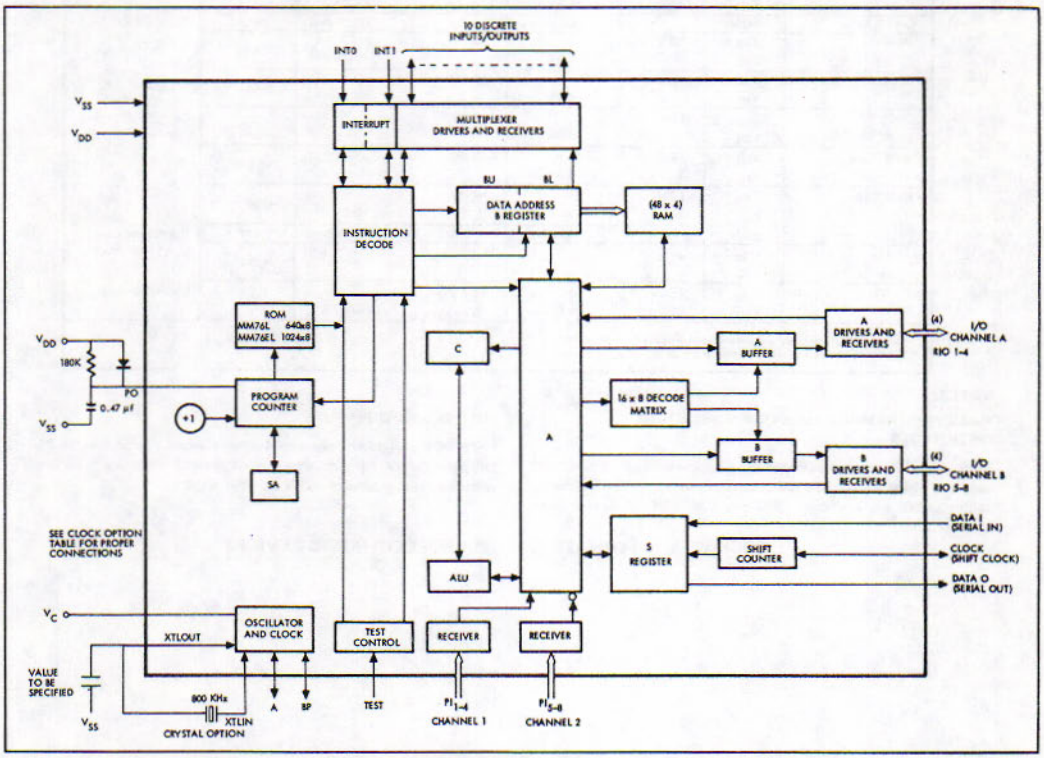
**Conditional Transfer Instructions**

| | |
|---|---|
| TC | Transfer on Carry Set |
| TNC | Transfer on No Carry Set |
| TLC | Transfer Long on Carry Set |
| TLNC | Transfer Long on No Carry Set |
| TBF | Transfer on Bit in Memory False |
| TBT | Transfer on Bit in Memory True |
| TLBF | Transfer Long on Bit in Memory False |
| TLBT | Transfer Long on Bit in Memory True |
| TE | Transfer on A = Memory |
| TNE | Transfer on A ≠ Memory |
| TLE | Transfer Long on A = Memory |
| TLNE | Transfer Long on A ≠ Memory |
| TIH | Transfer if Input High |
| TIL | Transfer if Input Low |
| TLIH | Transfer Long if Input High |
| TLIL | Transfer Long if Input Low |

**ROM Addressing Instructions**

| | |
|---|---|
| RT | Return from Subroutine |
| RTSK | Return and Skip |
| T | Transfer on Page |
| NOP | No Operation |
| TL | Transfer Long |
| TM | Transfer and Mark |
| TML | Transfer and Mark Long |






**PPS-4/1 MM76L and MM76EL System Block Diagram**

## SPECIFICATIONS

### OPERATING CHARACTERISTICS

Supply Voltage:

$V_{DD}$ = -8.5 Volts -2.5, +2.0 Volts
(Logic "1" = most negative voltage $V_{IL}$ and $V_{OL}$.)

$V_{SS}$ = 0 Volts (Gnd.)
(Logic "0" = most positive voltage $V_{IH}$ and $V_{OH}$.)

System Operating Frequencies:

(1) Internal: 100 kHz Nominal at $V_{DD}$ = -8.5V

(2) External 800 kHz Crystal: 100 kHz

Device Power Consumption: 15 mw, typical

Input Capacitance: <5 pf

Input Leakage: <10 $\mu$a

Open Drain Driver Leakage (R OFF): <10 $\mu$a at -30 Volts

Operating Ambient Temperature ($T_A$)

0°C to +70°C (Commercial): MM76L and MM76EL
-40°C to +85°C (Industrial): MM76L-2 and MM76EL-2

Storage Temperature: -55°C to 120°C

### ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 volts.

Maximum positive voltage on any pin +0.3 volts.

### TEST CONDITIONS: $V_{DD}$ = -8.5V, $T_A$ = 25°C

| INPUT/OUTPUT | SYMBOL | LIMITS (VSS = 0) MIN | TYP | MAX | LIMITS (VSS = +5V) MIN | TYP | MAX | TIMING (SAMPLE/ GOOD) | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| Supply Current (Average) for VDD | IDD | | 1.75 ma | 3 ma | | 1.75 ma | 3 ma | | |
| Discrete I/O's DI/O 0-9 | $V_{IH}$ | -1.0V | | | +4.0V | | | ϕ34 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 100 ohms | | | 100 ohms | ϕ2* | 10.0 ma max. |
| Channel 1 Input PI1-PI4 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ1 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| Channel 2 Input PI5-PI8 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ3 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| I/O Channel A RIO1-RIO4 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ4 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 250 ohms | | | 250 ohms | ϕ2* | 6.0 ma max. |
| I/O Channel B RIO5-RIO8 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ4 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 250 ohms | | | 250 ohms | ϕ2* | 6.0 ma max. |
| DATA I | $V_{IH}$ | -1.0V | | | +4.0V | | | ϕ4 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| DATA O | RON | | | 500 ohms | | | 500 ohms | ϕ4** | 3.0 ma max. |
| INT0 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ3 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| INT1 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ1 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| Clock A, BP, ($\overline{B}$) | $V_{OH}$ | -1.0V | | | +4.0V | | | | CL = 50 pf (max) |
| | $V_{OL}$ | | | -5.0V | | | 0V | | |
| XTLIN | $V_{IH}$ | -1.0V | | | +3.5V | | | -4.0V | |
| | $V_{IL}$ | | | -6.0V | | | -1.0V | | |
| Shift Clock | $V_{IH}$ | -1.0V | | | +4.0V | | | ϕ34 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 500 ohms | | | 500 ohms | ϕ4** | 2.0 ma max. |
| VC | $V_{IH}$ | | | | | | | | V = 11.0V max. |
| | $V_{IL}$ | | | | | | | | |
| PO | $V_{IH}$ | -2.5V | | | +2.5V | | | | Special circuit |
| | $V_{IL}$ | | | -5.0V | | | 0V | | |

*State established by ϕ2 (minimum impedance after ϕ4).
**Same as above except ϕ4 minimum at ϕ2 of next cycle.

**NOTES:**

### MASK PROGRAMMED PULL-DOWN RESISTORS ON OUTPUTS

Resistor pull-downs are available as an option on all RIO and DI/O outputs. These pull-downs are connected to $V_{DD}$. The following vaules ± 25% are available: 3K, 5K, 10K, 15K, 25K, and Open Circuit.

### PULL-DOWNS ON INPUTS

MOS FET pull-downs are also available as an option on the PI, INT, and DATA I inputs. The output current is 50 $\mu$a ± 25 $\mu$a with the input grounded and $V_{DD}$ at -8.5 volts.

Rockwell

# PARALLEL PROCESSING SYSTEM (PPS)
## DATA SHEET

*PPS-4/1 One-Chip Microcomputer Family*

# MM77 and MM78

**one-chip microcomputer systems**



## SUMMARY

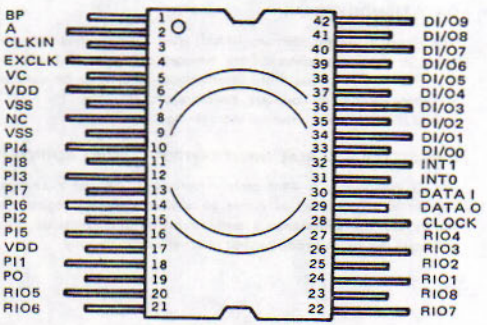
The Rockwell MM77 and MM78 one-chip microcomputers are pin and instruction-set compatible systems designed to economically implement a wide variety of equipment. Their large instruction set is augmented by powerful multi-function instructions. 31 I/O ports further identify the power of these systems. Serial I/O capability, which can be clocked simultaneously or externally controlled, extend their power.

On single LSI chips, the MM77 and MM78 provide complete 4-bit parallel processing systems — Central Processing Unit (CPU), Program Memory (ROM), Data Memory (RAM), Program Counter (P), Instruction Decode, two Program Save registers, Data Address register (B), 10 I/O discrete drivers/receivers, two 4-bit parallel I/O channels, two 4-bit parallel input channels, a serial input/output port, interrupt and control logic, and a self-contained four-phase clock generator circuit.

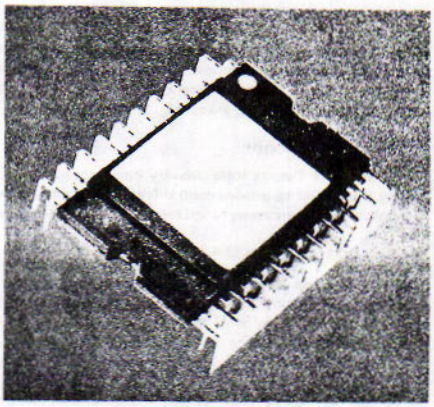
| | ROM 8-Bit Bytes | RAM 4-Bit Bytes |
|---|---|---|
| MM77 | 1344 | 96 |
| MM78 | 2048 | 128 |

In addition to stand-alone system applications, both microcomputers can be directly interfaced with other multi-chip systems as dedicated slave controllers or for other purposes. Also, two or more MM77 and/or MM78 systems can be directly combined to perform parallel processing or control operations.

To facilitate system and program development, Rockwell provides powerful development aids — see under "Features" at right. Typically, a trained programmer can complete an MM77 program in about six weeks and an MM78 program in about eight weeks.




PPS-4/1 MM77 and MM78 Pin Configuration



## FEATURES

- MM77 — 1344 8-bit bytes of program memory and 96 4-bit data words
- MM78 — 2048 8-bit bytes of program memory and 128 4-bit data words
- Clocked simultaneous serial input/output capability
- Externally controlled serial input/output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Arithmetic logic unit and six working registers
- Two-level subroutine nesting
- 31 input/output ports
- Easy circuit level testing by user
- Large Instruction set — over 50 instructions
- Multifunction instructions increase throughput
- Single power supply operation (15 volts ±5%)
- Low power (75 milliwatts typical, 125 milliwatts max)
- Powerful development aids:
  - General Electric Software Assembler
  - Evaluation Module 19703D43-7
  - PPS Universal Assemulator 19703D13 with PPS-4/1 Personality Board 19703D40-7 for Program and Hardware Development
  - Development Circuits provide address and data lines so that Program Memory can be in external PROM or RAM for emulation purposes. MM77 Development Circuit is P/N A7798; MM78 is P/N A7898.
  - Scheduled and Special Training Courses
  - International Applications Engineering Support



Specifications subject to change without notice
Rev. 4 October, 1978

## FUNCTIONAL DESCRIPTION

### PROGRAM COUNTER (P), SA REGISTER, and SB REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

The SB Register provides a second hardware stack register so that two levels of subroutines may be nested in the microcomputer.

### PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides the storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

### INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

### DATA ADDRESS REGISTER (B)

The Data Address Register is 7 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM are addressed by all 7 bits and the discrete input/output ports are addressed by the 4 bits in BL when the value in BU is between 0 and 3.

A number of multifunction instructions simultaneously modify B Upper and cause B Lower to be automatically incremented or decremented and tested for overflow or underflow.

### ACCUMULATOR and ARITHMETIC LOGIC UNIT (A, ALU, AND C)

The Primary working register in the MM77 and MM78 is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform binary arithmetic. By means of software routines, decimal arithmetic can be performed. Constants may be loaded into the Accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data.

### A BUFFER

The contents of the Accumulator may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or until the power is turned off.

### X BUFFER

The X Buffer comprises four latches which will output the last bit pattern loaded until either a new Output X Register command is executed or power is turned off.

### X REGISTER

The X Register is an auxiliary register which may be used as temporary storage for 4 bits of data without reference to data memory. The X Register is also used as a data path to the X Buffer output register and from receiver inputs.

### CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port P11 through P14 will be added to the contents of the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

### CHANNEL 2 INPUT PORTS (PI5 through PI8)

The inverted state of the inputs at parallel input ports PI5 thru PI8 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 3 time) so that asynchronous input signals may be used.

### CHANNEL A I/O PORTS (RI01 through RI04)

The contents of the Accumulator may be output for control or data transfer purposes through the A Buffer. The A Buffer will hold the data output until new data is output or power is turned off.

### CHANNEL X I/O PORTS (R105 through R108)

The four parallel input/output ports of Channel X function as described in X Buffer and X Register paragraphs.

### CONDITIONAL INTERRUPTS (INT0 and INT1)

The conditional interrupts INT0 and INT1 may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized with INT0 sampled at phase 3 and INT1 sampled at phase 1.

### DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O9)

There are ten discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized so that asynchronous input signals may be used.

### CLOCK CONTROL (VC, CLKIN, EXCLK, and OSCILLATOR)

The internal Oscillator and Clock circuit generates a four-Phase A $\bar{B}$ clock signal used for all internal logic functions. The A $\bar{B}$ clock terms are also brought out so external logic can be synchronized. The clock frequency is a nominal 80 kHz ±50%. When precise timing is required, a reference frequency may be input at CLKIN.

### DATA MEMORY (RAM)

The Random Access Memory (RAM) used for data memory contains 96 4-bit characters. Data memory can be used to buffer input or output values, hold intermediate results, or be used as a register for timers, counters, comparators, etc., when the MM77 or MM78 is used as a universal logic element.

### S REGISTER – SERIAL INPUT/OUTPUT – SHIFT COUNTER

The S Register is a 4-bit serial-in/serial-out, parallel exchange, register which is used as either an auxiliary storage register or buffer for the simultaneous serial input/output functions. The shift rate can be controlled either internally or externally.

## PPS-4/1 MM77 AND MM78 INSTRUCTION SET

**RAM Addressing Instructions**

| | |
|---|---|
| XAB | Exchange A with BL |
| LBA | Load BL from A |
| LB | Load BL, BU → O |
| EOB | Exclusive OR BU |
| LBL | Load B Long |
| INCB | Increment B |
| DECB | Decrement B |
| SAG | Special Address Generation |

**Bit Manipulation Instructions**

| | |
|---|---|
| SB | Set Bit |
| RB | Reset Bit |
| SKBF | Skip on Bit False |

**Register to Register Instructions**

| | |
|---|---|
| LXA | Load X from A |
| XAS | Exchange A and S |
| XAX | Exchange A and X |

**Arithmetic Instructions**

| | |
|---|---|
| A | Add Memory to A |
| AC | Add Memory with Carry to A |
| ACSK | Add Memory with Carry to A and Skip on Carry-out |
| DC | Decimal Correction |
| COM | Complement A |
| RC | Reset Carry |
| SC | Set Carry |
| SKNC | Skip on No Carry |
| LAI | Load A with Immediate Field |
| AISK | Add Immediate and Skip on No Carry-out |

**ROM Addressing Instructions**

| | |
|---|---|
| RT | Return from Subroutine |
| RTSK | Return and Skip |
| T | Transfer on Page |
| NOP | No Operation |
| TL | Transfer Long |
| TLB | Transfer Long Banked |
| TM | Transfer and Mark |
| TML | Transfer and Mark Long |
| TMLB | Transfer and Mark Long Banked |

**Logical Comparison Instructions**

| | |
|---|---|
| SKMEA | Skip if Memory Equals A |
| SKBEI | Skip if BL Equals Immediate Field |
| SKAEI | Skip if A Equals Immediate Field |
| TAB | Table Look Up |

**Input/Output Instructions**

| | |
|---|---|
| SOS | Set Output Selected |
| ROS | Reset Output Selected |
| SKISL | Skip on Input Selected Low |
| IX | Input X from RIO 5-8 |
| OX | Output X to RIO 5-8 |
| IOA | Input A Receivers to A and output A to RIO 1-4 |
| IOS | Serial Input/Output |
| I1SK | Input Channel 1. Add to A, Skip if No Carry |
| I2C | Input Channel 2 and Complement |
| INT1L | Skip if INT1 Input is Low |
| INT0H | Skip if INT0 Input is High |

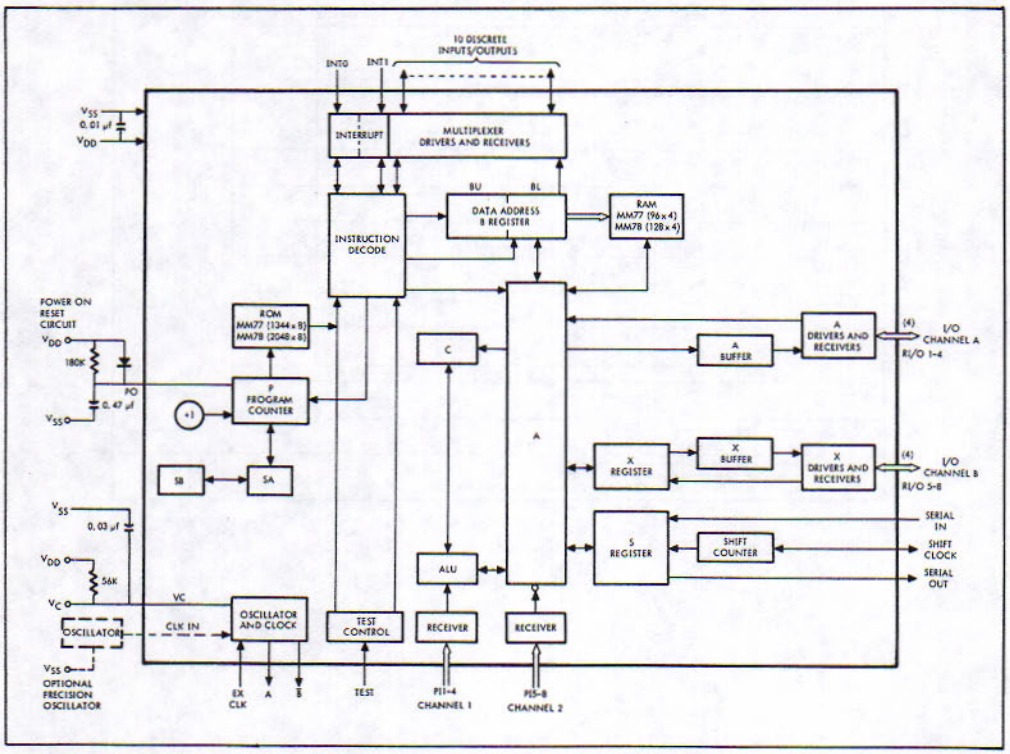
**Conditional Transfer Instructions**

| | |
|---|---|
| TC | Transfer on Carry Set |
| TNC | Transfer on No Carry Set |
| TLC | Transfer Long on Carry Set |
| TLNC | Transfer Long on No Carry Set |
| TBF | Transfer on Bit in Memory False |
| TBT | Transfer on Bit in Memory True |
| TLBF | Transfer Long on Bit in Memory False |
| TLBT | Transfer Long on Bit in Memory True |
| TE | Transfer on A = Memory |
| TNE | Transfer on A ≠ Memory |
| TLE | Transfer Long on A = Memory |
| TLNE | Transfer Long on A ≠ Memory |
| TIH | Transfer if Input High |
| TIL | Transfer if Input Low |
| TLIH | Transfer Long if Input High |
| TLIL | Transfer Long if Input Low |

**Register Memory Instructions**

| | |
|---|---|
| L | Load A from Memory |
| X | Exchange A and Memory |
| XDSK | Exchange A with Memory. Decrement BL and Skip if BL Counts to 15 |
| XNSK | Exchange A with Memory. Increment BL and Skip if BL Counts to 0 |






PPS-4/1 MM77 and MM78 System Block Diagram

# SPECIFICATIONS

## OPERATING CHARACTERISTICS

Supply Voltage:

VDD = 15 Volts ±5%
(Logic "1" = most negative voltage $V_{IL}$ and $V_{OL}$.)

VSS = 0 Volts (Gnd.)
(Logic "0" = most positive voltage $V_{IH}$ and $V_{OH}$.)

System Operating Frequencies:

80 kHz ±50% with external resistor

Device Power Consumption:

75 mw, typical

Input Capacitance:

<5 pf

Input Leakage:

<10 μa

Open Drain Driver Leakage (R OFF):

≤10 μa at -30 Volts

Operating Ambient Temperature (TA):

0°C to 70°C (TA = 25°C unless otherwise specified.)

Storage Temperature:

-55°C to 120°C

## ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 volts.

Maximum positive voltage on any pin +0.3 volts.

| FUNCTION | SYMBOL | LIMITS (VSS = 0) MIN | TYP | MAX | LIMITS (VSS = +5V) MIN | TYP | MAX | TIMING (SAMPLE/ GOOD) | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| Supply Current (Average) for VDD | IDD | | 5 ma | 8 ma | | 5 ma | 8 ma | | VDD = -15.75V T = 25°C |
| Discrete I/O's | $V_{IH}$ | -1.0V | | | +4.0V | | | ϕ3 | |
| DI/O 0-DI/O 9 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 500 ohms | | | 500 ohms | ϕ2* | 3.0 ma max. |
| Channel 1 Input | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ1 | |
| PI1-PI4 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| Channel 2 Input | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ3 | |
| PI5-PI8 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| I/O Channel A | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ3 | |
| RI/O1-RI/O4 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 500 ohms | | | 500 ohms | ϕ2* | 3.0 ma max. |
| I/O Channel X | $V_{IH}$ | -1.0V | | | +4.0V | | | Not sync. Must be stable at ϕ1 and 2. | |
| RI/O5-RI/O8 | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 500 ohms | | | 500 ohms | ϕ2* | 3.0 ma max. |
| DATA I | $V_{IH}$ | -1.0V | | | +4.0V | | | ϕ4 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| DATA O | RON | | | | | | | ϕ4** | |
| INT0 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ3 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| INT1 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ1 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| Clock | $V_{OH}$ | -1.0V | | | +4.0V | | | | CL = 50 pf (max.) |
| A, BP, ($\bar{B}$) | $V_{OL}$ | | | -10.0V | | | -5.0V | | |
| EXCLK | $V_{IH}$ | -1.5V | | | +3.5V | | | STRAP | F max = 80 kHz |
| | $V_{IL}$ | | | -7.0V | | | -2.0V | | |
| CLK IN | $V_{IH}$ | -1.0V | | | +4.0V | | | | |
| | $V_{IL}$ | | | -10.0V | | | -5.0V | | |
| Shift Clock | $V_{IH}$ | -1.0V | | | +4.0V | | | ϕ34 | |
| Clock | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 500 ohms | | | 500 ohms | ϕ4** | 2.0 ma max. |
| VC*** | $V_{IH}$ | | | | | | | | 56K ±5% |
| | $V_{IL}$ | | | | | | | | |
| PO | $V_{IH}$ | -2.0V | | | +3.0V | | | | Special circuit |
| | $V_{IL}$ | | | -6.0V | | | -1.0V | | |

*State established by ϕ2 (minimum impedance after ϕ4).
**Same as above except ϕ4 minimum at ϕ2 of next cycle.
***Connect VC to VDD through a resistor: 56KΩ for 80 kHz or 47KΩ for 100 kHz

DOCUMENT NO. 29000 D57
P/N B77XX AND B78XX

Rockwell

# PARALLEL PROCESSING SYSTEM (PPS)
## DATA SHEET

*PPS-4/1 One-Chip Microcomputer Family*

# MM77L and MM78L

**low-voltage, low power one-chip microcomputer systems**



## SUMMARY

The Rockwell MM77L and MM78L microcomputers are complete 4-bit parallel processing systems. Both the MM77L and MM78L are low voltage (6.5 to 11 volt range), very low power (15 milliwatts typical) versions of the well known PPS-4/1 one-chip microcomputer. All of the microcomputers in the family of PPS-4/1 microcomputers fit the needs of Equipment Designers seeking low-cost systems capable of performing functions in the range of medium complexity. However, the MM77L and MM78L are especially desirable where low-cost battery operation as the primary or backup power source is required, or where power consumption or heat dissipation is a consideration, or where portability is required. The entire PPS-4/1 family of microcomputers is distinguished from competitive microprocessors by superior I/O capability, and by other functional features identified on this page.

The MM77L and MM78L are pin and instruction-set compatible. The MM78L has larger Program Memory (ROM) capacity, making it an easy design step-up if end-product requirements are increased during development based on the MM77L.

On single LSI chips both the MM77L and MM78L provide complete systems consisting of the following functional areas: a versatile Central Processing Unit (CPU), Instruction Decode, two Program Save Registers, Program Memory (ROM), Data Memory (RAM), Program Counter (P), Data Address Register (B), 10 I/O discrete Drivers/Receivers, two 4-bit parallel I/O channels, two 4-bit parallel input channels, a Serial I/O port, Interrupt and Control logic, and a self-contained four-phase Clock Generator circuit.

The Data Memory (RAM) and Program Memory (ROM capacities are:

| | ROM | RAM |
|---|---|---|
| MM77L | 1536 x 8 | 96 x 4 |
| MM78L | 2048 x 8 | 128 x 4 |

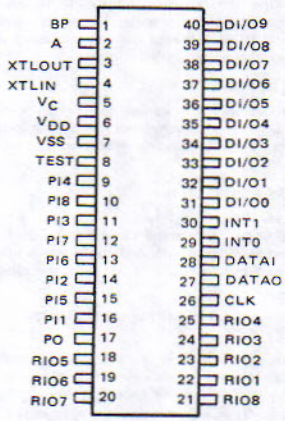
In addition to stand-alone applications, the MM77L and MM78L can be directly included in other multi-chip systems as dedicated controllers or in other functions. Also two or more MM77L and/or MM78L microcomputers can be directly combined to perform parallel processing or control operations. In the design of families of end-products, a total range of features can be designed so that increasingly higher levels of performance can be produced by low-cost wiring changes and chip additions, minimizing design costs and production inventories.

The MM77L and MM78L are available in commercial and industrial versions. These versions differ only in their operating temperature ranges, as follows:

$0^{\circ}$C to $+70^{\circ}$C (Commercial): MM77L and MM78L
$-40^{\circ}$C to $+85^{\circ}$C (Industrial): MM77L-2 and MM78L-2

## NEW ELECTRICAL FEATURES

- Battery Compatible (-6.5 to -11.0 volt operation)
- Low Power 15 milliwatts nominal @ -8.5 volts
- 4 Clock Modes including external crystal
- Low Impedance Drivers
  DI/O less than 100 ohm @ 10 ma
  RIO less than 250 ohm @ 6 ma
- Mask Programmed pull-down Resistors on Outputs
- Mask Programmed Enhancement FET pull-downs on Inputs




**MM77L and MM78L Pin Configuration**

## FUNCTIONAL FEATURES

- Software compatible with MM77 and MM78
- Standard 40-pin Dual-In-Line (DIP) package
- MM77L – 1536 8-bit bytes of program memory
- MM78L – 2048 8-bit bytes of program memory
- 96 4-bit words (384 bits) of data memory for MM77L
- 128 4-bit words (512 bits) of data memory for MM78L
- Serial input/output capability
- Two interrupt request input lines
- TTL and CMOS compatible
- Six working registers
- 31 input/output ports
- Large instruction set – over 50 instructions
- Multifunction instructions increase throughput
- Single power supply operation (-8.5 volts, -2.5, +2.0 volts)
- Low power (15 milliwatts typical)
- Powerful development aids:
  - Evaluation Module PE01-D002 or -D003
  - PPS Univeral Assemulator 19703D13 with PPS-4/1 Personality Board 19703D40 with Adapter Module for Program and Hardware Development
  - Development Circuit (P/N B7898 for both MM77L and MM78L) provides address and data lines so that Program Memory can be in external PROM or RAM for emulation purposes.
  - Scheduled and Special Training Courses
  - International Applications Engineering Support



Specifications subject to change without notice
October 1978

## FUNCTIONAL DESCRIPTION

### PROGRAM COUNTER (P) and SA REGISTER

The Program Counter contains the ROM address of the next program instruction. The address in the P Register is automatically incremented each cycle time during normal operation to address the next instruction. In addition, instructions are available to alter the address in the P Register as necessary to fetch an instruction from any address in program memory.

The SA Register is a "save" register which saves the incremented value of current address in the P Register during subroutine execution. This provides a means of returning from a subroutine directly to the next instruction after the subroutine call.

The SB Register provides a second hardware stack register so that two levels of subroutines may be nested in the microcomputer.

### PROGRAM MEMORY – READ ONLY MEMORY (ROM)

The ROM provides the storage for instructions and constants required to operate the microcomputer. Under control of the Program Counter the ROM will read out the addressed instruction which is to be decoded and executed.

### INSTRUCTION DECODE

The Instruction Decode logic circuitry interprets the instructions pulled from ROM to provide control for data transfers, arithmetic operations, other processing functions and input/output operations.

### DATA ADDRESS REGISTER (B)

The Data Address Register is 7 bits in length and is made up of two segments, B Upper (BU) and B Lower (BL). Data locations in RAM are addressed by all 7 bits and the discrete input/output ports are addressed by the 4 bits in BL when the value in BU is between 0 and 3.

### ACCUMULATOR and ARITHMETIC LOGIC UNIT (A, ALU, AND C)

The Primary working register in the MM77L and MM78L is the Accumulator (A). It is the Accumulator which ties with the Arithmetic Logic Unit (ALU) and the Carry flip-flop (C) to perform binary arithmetic. By means of software routines, decimal arithmetic can be performed. Constants may be loaded into the accumulator from the read only memory or variable data may be loaded from, or exchanged with the random access memory (RAM) under control of the Data Address Register (B). The Accumulator is also the primary path for 4-bit parallel or serial input or output data.

### DATA MEMORY (RAM)

The Random Access Memory (RAM) data memory can be used to buffer input or output values, hold intermediate results, or be used as a register for timers, counters, comparators, etc.

### CLOCK CONTROL (VC, XTLIN, XTLOUT, A, and BP)

The internal Oscillator and Clock circuit generates a four-phase A BP clock signal used for all internal logic functions. The A and BP clock terms are also brought out so external logic can be synchronized. The clock for the MM77L and MM78L can be selected to operate in one of four modes as shown by the table below. These options are selected by control voltages applied to the VC and XTLIN pins.

### A BUFFER

The contents of the Accumulator may be output for control, display, or data transfer functions through the A Buffer. The A Buffer holds the data for output until new data is received from the Accumulator or until the power is turned off.

### X BUFFER

The X Buffer is a 4-bit latch that will output the last bit pattern loaded until either a new Output X Register command is executed or power is turned off.

### CHANNEL 1 INPUT PORTS (PI1 through PI4)

The parallel input port PI1 through PI4 will be loaded into the contents of the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 1 time) so that asynchronous input signals may be used.

### CHANNEL 2 INPUT PORTS (PI5 through PI8)

The inverted state of the inputs at parallel input ports PI5 thru PI8 will be loaded into the Accumulator upon command. The receivers are TTL compatible and are synchronized (phase 3 time) so that asynchronous input signals may be used.

### CHANNEL A I/O PORTS (RI01 through RI04)

The contents of the Accumulator may be output for control or data transfer purposes through the A Buffer. The A Buffer will hold the data output until new data is output or power is turned off.

### CHANNEL X I/O PORTS (RI05 through RI08)

The four parallel input/output ports of Channel X function as described in X Buffer and X Register paragraphs.

### CONDITIONAL INTERRUPTS (INT0 and INT1)

The conditional interrupts INT0 and INT1 may be used to detect external signals and set internal control flip-flops. The receivers are TTL compatible and synchronized.

### DISCRETE INPUT/OUTPUT PORTS (DI/O0 through DI/O9)

There are ten discrete input or output lines each of which can be controlled individually under program control. The receivers are fully synchronized to that asynchronous input signals may be used.

### X REGISTER

The X Register is an auxiliary register which may be used as temporary storage for 4 bits of data without reference to data memory. The X Register is also used as a data path to the X Buffer output register and from receiver inputs.

### S REGISTER – SERIAL INPUT/OUTPUT – SHIFT COUNTER

The S register is a 4-bit serial-in/serial-out, parallel exchange, register which is used as either an auxiliary storage register or buffer for the simultaneous serial input/output functions. The shift rate can be controlled either internally or externally.

| Mode | Pins | | | | | Frequency |
|---|---|---|---|---|---|---|
| | VC | XTLIN | XTLOUT | A | BP | |
| INTERNAL | *$V_C$ | VSS | – | OUT | OUT | 100 kHz ±30% @ -8.5V |
| EXTERNAL | VSS | CLOCK | – | OUT | OUT | 400 – 800 kHz @ -8.0V |
| CRYSTAL | VSS | XTAL | XTAL | OUT | OUT | 800 kHz @ -8.0V |
| SLAVE | $V_{DD}$ | $V_{DD}$ | – | IN | IN | 100 kHz – 50 kHz @ -8.5V |

*Can be adjusted to vary frequency – Normally set to $V_{DD}$

## PPS-4/1 MM77L AND MM78L INSTRUCTION SET

**RAM Addressing Instructions**

| | |
|---|---|
| XAB | Exchange A with BL |
| LBA | Load BL from A |
| LB | Load BL, BU → O |
| EOB | Exclusive OR BU |
| LBL | Load B Long |
| INCB | Increment B |
| DECB | Decrement B |
| SAG | Special Address Generation |

**Bit Manipulation Instructions**

| | |
|---|---|
| SB | Set Bit |
| RB | Reset Bit |
| SKBF | Skip on Bit False |

**Register to Register Instructions**

| | |
|---|---|
| LXA | Load X from A |
| XAS | Exchange A and S |
| XAX | Exchange A and X |

**Arithmetic Instructions**

| | |
|---|---|
| A | Add Memory to A |
| AC | Add Memory with Carry to A |
| ACSK | Add Memory with Carry to A and Skip on Carry-out |
| DC | Decimal Correction |
| COM | Complement A |
| RC | Reset Carry |
| SC | Set Carry |
| SKNC | Skip on No Carry |
| LAI | Load A with Immediate Field |
| AISK | Add Immediate and Skip on No Carry-out |

**ROM Addressing Instructions**

| | |
|---|---|
| RT | Return from Subroutine |
| RTSK | Return and Skip |
| T | Transfer on Page |
| NOP | No Operation |
| TL | Transfer Long |
| TLB | Transfer Long Banked |
| TM | Transfer and Mark |
| TML | Transfer and Mark Long |
| TMLB | Transfer and Mark Long Banked |

**Logical Comparison Instructions**

| | |
|---|---|
| SKMEA | Skip if Memory Equals A |
| SKBEI | Skip if BL Equals Immediate Field |
| SKAEI | Skip if A Equals Immediate Field |
| TAB | Table Look Up |

**Input/Output Instructions**

| | |
|---|---|
| SOS | Set Output Selected |
| ROS | Reset Output Selected |
| SKISL | Skip on Input Selected Low |
| IX | Input X from RIO 5-8 |
| OX | Output X to RIO 5-8 |
| IOA | Input A Receivers to A and output A to RIO 1-4 |
| IOS | Serial Input/Output |
| I1SK | Input Channel 1, Add to A, Skip if No Carry |
| I2C | Input Channel 2 and Complement |
| INT1L | Skip if INT1 Input is Low |
| INT0H | Skip if INT0 Input is High |

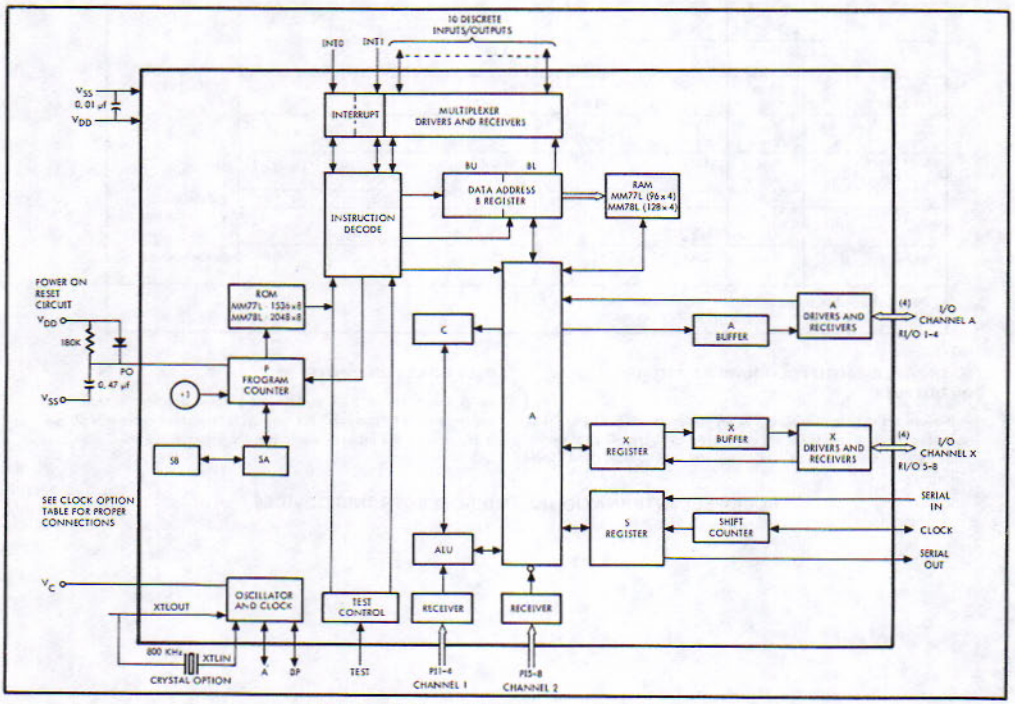
**Conditional Transfer Instructions**

| | |
|---|---|
| TC | Transfer on Carry Set |
| TNC | Transfer on No Carry Set |
| TLC | Transfer Long on Carry Set |
| TLNC | Transfer Long on No Carry Set |
| TBF | Transfer on Bit in Memory False |
| TBT | Transfer on Bit in Memory True |
| TLBF | Transfer Long on Bit in Memory False |
| TLBT | Transfer Long on Bit in Memory True |
| TE | Transfer on A = Memory |
| TNE | Transfer on A ≠ Memory |
| TLE | Transfer Long on A = Memory |
| TLNE | Transfer Long on A ≠ Memory |
| TIH | Transfer if Input High |
| TIL | Transfer if Input Low |
| TLIH | Transfer Long if Input High |
| TLIL | Transfer Long if Input Low |

**Register Memory Instructions**

| | |
|---|---|
| L | Load A from Memory |
| X | Exchange A and Memory |
| XDSK | Exchange A with Memory, Decrement BL and Skip if BL Counts to 15 |
| XNSK | Exchange A with Memory, Increment BL and Skip if BL Counts to 0 |






PPS-4/1 MM77L and MM78L System Block Diagram

## SPECIFICATIONS

### OPERATING CHARACTERISTICS

Supply Voltage:

$V_{DD}$ = -8.5 Volts -2.5, +2.0 Volts
(Logic "1" = most negative voltage $V_{IL}$ and $V_{OL}$.)

$V_{SS}$ = 0 Volts (Gnd.)
(Logic "0" = most positive voltage $V_{IH}$ and $V_{OH}$.)

System Operating Frequencies:

(1) Internal: 100 kHz Nominal at $V_{DD}$ = -8.5V

(2) External 800 kHz Crystal: 100 kHz

Device Power Consumption: 15 mw, typical

Input Capacitance: <5 pf

Input Leakage: <10 μa

Open Drain Driver Leakage (R OFF): <10 μa at -30 Volts

Operating Ambient Temperature ($T_A$)

0°C to +70°C (Commercial): MM77L and MM78L
-40°C to +85°C (Industrial): MM77L-2 and MM78L-2

Storage Temperature: -55°C to 120°C

### ABSOLUTE MAXIMUM VOLTAGE RATINGS (with respect to VSS)

Maximum negative voltage on any pin -30 volts.

Maximum positive voltage on any pin +0.3 volts.

### TEST CONDITIONS: $V_{DD}$ = -8.5V, $T_A$ = 25°C

| INPUT/OUTPUT | SYMBOL | LIMITS (VSS = 0) MIN | TYP | MAX | LIMITS (VSS = +5V) MIN | TYP | MAX | TIMING (SAMPLE/GOOD) | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|
| Supply Current (Average) for VDD | IDD | | 1.75 ma | 3 ma | | 1.75 ma | 3 ma | | |
| Discrete I/O's DI/O 0-9 | $V_{IH}$ | -1.0V | | | +4.0V | | | ϕ3, ϕ4 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 100 ohms | | | 100 ohms | ϕ2* | 10.0 ma max. |
| Channel 1 Input PI1-PI4 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ1 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| Channel 2 Input PI5-PI8 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ3 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| I/O Channel A RIO1-RIO4 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ4 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 250 ohms | | | 250 ohms | ϕ2* | 6.0 ma max. |
| I/O Channel B RIO5-RIO8 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ4 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 250 ohms | | | 250 ohms | ϕ2* | 6.0 ma max. |
| DATA I | $V_{IH}$ | -1.0V | | | +4.0V | | | ϕ4 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| DATA O | RON | | | 500 ohms | | | 500 ohms | ϕ4** | 3.0 ma max. |
| INT0 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ3 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| INT1 | $V_{IH}$ | -1.5V | | | +3.5V | | | ϕ1 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| Clock A, BP | $V_{OH}$ | -1.0V | | | +4.0V | | | | CL = 50 pf (max) |
| | $V_{OL}$ | | | -5.0V | | | 0V | | |
| XTLIN | $V_{IH}$ | -1.0V | | | +3.5V | | | -4.0V | |
| | $V_{IL}$ | | | -6.0V | | | -1.0V | | |
| Shift Clock | $V_{IH}$ | -1.0V | | | +4.0V | | | ϕ3, ϕ4 | |
| | $V_{IL}$ | | | -4.2V | | | +0.8V | | |
| | RON | | | 500 ohms | | | 500 ohms | ϕ4** | 2.0 ma max. |
| VC | $V_{IH}$ | | | | | | | | V = 11.0V max. |
| | $V_{IL}$ | | | | | | | | |
| PO | $V_{IH}$ | -2.5V | | | +2.5V | | | | Special circuit |
| | $V_{IL}$ | | | -5.0V | | | 0V | | |

*State established by ϕ2 (minimum impedance after ϕ4).
**Same as above except ϕ4 minimum at ϕ2 of next cycle.

**NOTES:**

### MASK PROGRAMMED PULL-DOWN RESISTORS ON OUTPUTS

Pull-down resistors are available as an option on all RIO and DI/O outputs. These pull-downs are connected to $V_{DD}$. The following values ±25% are available: 3K, 5K, 10K, 15K, 25K, and Open Circuit.

### PULL-DOWNS ON INPUTS

MOS enhancement FET pull-downs are also available as an option on the PI, INT, and DATA I inputs. The output current is 50 μa ±25 μa with the input grounded and $V_{DD}$ at -8.5 volts.

DOCUMENT NO. 29410 N21
NOVEMBER 1977

Rockwell

PARALLEL PROCESSING SYSTEM (PPS)

APPLICATION NOTE

# SERIAL COMMUNICATIONS PROTOCOL FOR MULTIPLE PPS-4/1 SYSTEMS

A simple communications protocol can be implemented between two PPS-4/1 microprocessors using only five interface lines. In order to prevent both units from attempting to transmit simultaneously, one processor must be designated as the Master and the other as the Slave. The Master initiates all communication. The Slave responds to commands and inquiries from the Master.

## COMMUNICATIONS BUS

The Communications Bus consists of the Serial Channel lines — Serial Data Out (DATAO), Serial Data In (DATAI) and CLOCK — and two bi-directional handshake lines (DI/O). One of the handshake lines will be used to transmit the Data Ready control signal (DR), the other will be used to transmit the Xmit Acknowledge control signal (XA). The connection of these lines is shown in the Serial Communication Block Diagram.

The normal (inactive) state of the handshake lines is low (driver off), which results in a "wired-OR" arrangement that allows either processor to "raise" the line by turning on its output driver.

## COMMUNICATIONS PHASES

Communications are normally conducted in two phases. During the Command Transmission Phase, the Master transmits a command or inquiry to the Slave. During the Data Transmission Phase, the Slave responds by transmitting one or more data words. The general sequence of events for each phase is described in the text to follow, and illustrated by the accompanying timing diagram.

### Command Transmission Phase

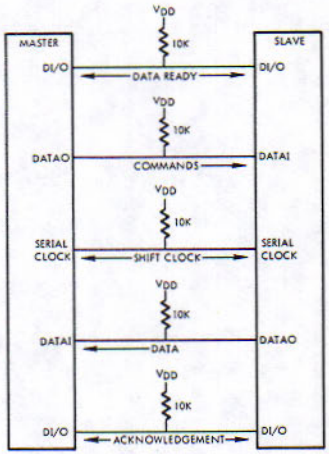
The sequence is:

1. Both handshake lines are low, indicating a "clear to send" condition.
2. Master transmits the command code to Slave via the Serial Channel. Eight cycles are needed to transmit four bits.
3. Master raises DR.
4. Slave senses DR high, saves command in RAM buffer and raises XA.
5. Master senses XA high, and drops DR.
6. Slave senses DR low, and drops XA.
7. Slave decodes command and performs required function.

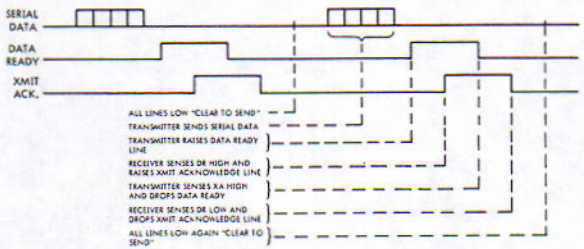
### Data Transmission Phase

The sequence is:

1. Both handshake lines are low, indicating a "clear to send" condition.
2. Slave transmits data to Master via the Serial Channel. Eight cycles are needed to transmit four bits.
3. Slave raises DR.
4. Master senses DR high, saves data in RAM buffer and raises XA.
5. Slave senses XA high, and drops DR.
6. Master senses DR low, and drops XA.
7. Slave senses XA low, and steps 2 through 6 are repeated for the required number of data words, including a four-bit checksum value. In the event of a checksum error, Master will transmit a new command and the entire process will be repeated.




PPS-4/1 SERIAL COMMUNICATION BLOCK DIAGRAM




SERIAL DATA HANDSHAKE TIMING DIAGRAM



Rockwell Microelectronic Devices
P. O. Box 3669
Anaheim, Calif. 92803

DOCUMENT NO. 29410 N22
JANUARY 1978

Rockwell

PARALLEL PROCESSING SYSTEM (PPS)

APPLICATION NOTE

# PPS-4/1 PROTOTYPING WITH 2708 PROM'S

Rockwell offers development circuit devices to support the prototyping of the PPS-4/1 Family of single-chip microcomputers. Such devices are available for the MM76, MM77 and MM78 series in both 52-pin quad in line packages (A7698, A7798 and A7898, respectively) and 64-pin dual in line packages (A7699, A7799 and A7899, respectively).

Each development circuit device is functionally identical to its production unit counterpart, except that the ROM portion of the chip has been replaced by circuits that interface to external memories for emulation purposes.

This application note describes a simple, practical approach to system prototyping using the above circuits with 2708 PROM.

## CIRCUIT DESIGN

Figure 1 shows the wiring required to directly interface a PPS-4/1 development circuit to 2708 PROM's. The MM77 52-pin device, the A7798, is used in this example, but with proper consideration of pinout differences a similar implementation can be used for any of the development circuit devices in the Family.

Since six of the eleven PROM address lines are timeshared with instruction data lines, the address (P1 - P11) is latched with the rising edge of the A clock (end of $\phi 2$) to provide a stable address to PROM throughout the cycle. The PROM Chip Select signal, $\overline{CS}$, is generated by decoding the most significant address bit P11, during $\phi 3$ and $\phi 4$. Figure 2 shows the timing waveforms before (2a) and after (2b) the address is latched.

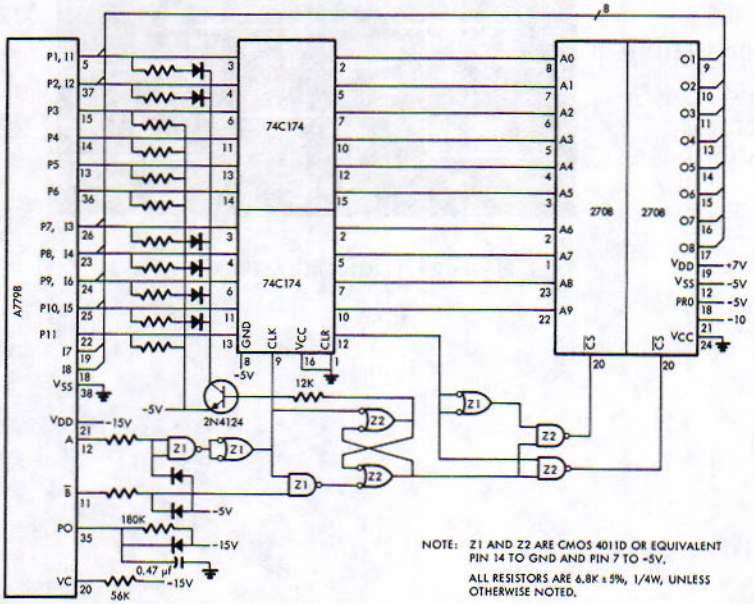
The pull-down resistors on shared address lines are floated during the chip select period to reduce loading effects on outputs of the selected PROM.

## PROGRAMMING CONSIDERATIONS

In programming a PROM for use with the circuit shown, it should be noted that the input data (I1-I8) must be low true (negative logic). That is FF ($V_O$ @ 2708 pins O1-O8 = H) is interpreted as 00, ED is interpreted as 12, and so on. Therefore, the bit pattern to be programmed must be inverted for assembled codes for proper instruction execution by the A7798.

Most PROM Programmers on the market are designed to permit this type of inversion with either a switch or a set of program patches. If the PPS-MP Universal Assemulator PROM Programmer is being used to program 2708 PROM's, make the following program patches:

| Data Memory Location | Is | S/B for Inversion |
|---|---|---|
| 45E | 00 | FF |
| 685 | 40 | 61 |
| 71F | 00 | 61 |
| 720 | A2 | 5D |




NOTE: Z1 AND Z2 ARE CMOS 4011D OR EQUIVALENT PIN 14 TO GND AND PIN 7 TO -5V.

ALL RESISTORS ARE 6.8K ± 5%, 1/4W, UNLESS OTHERWISE NOTED.

Figure 1. PPS-4/1 DEVELOPMENT CIRCUIT DEVICE A7798 WITH 2708 PROM



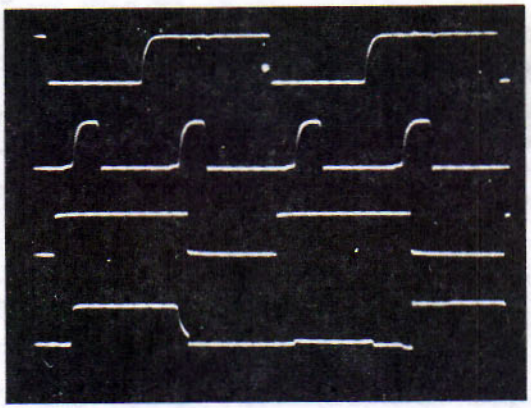
Rockwell Microelectronic Devices
P.O. Box 3669
Anaheim, Calif. 92803

A CLOCK (A)

B CLOCK ($\overline{B}$)

CHIP SELECT ($\overline{CS}$)

ADDRESS OUT
OF A7798 (P1)



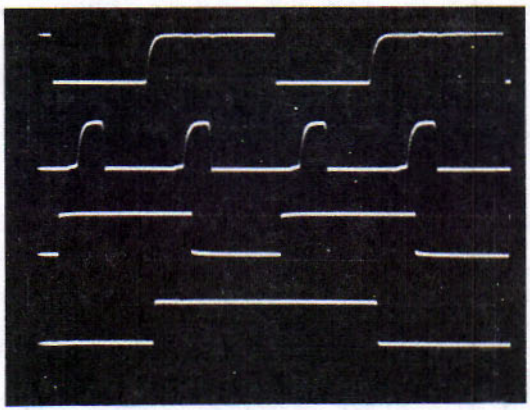
(2a.)

A CLOCK (A)

B CLOCK ($\overline{B}$)

CHIP SELECT ($\overline{CS}$)

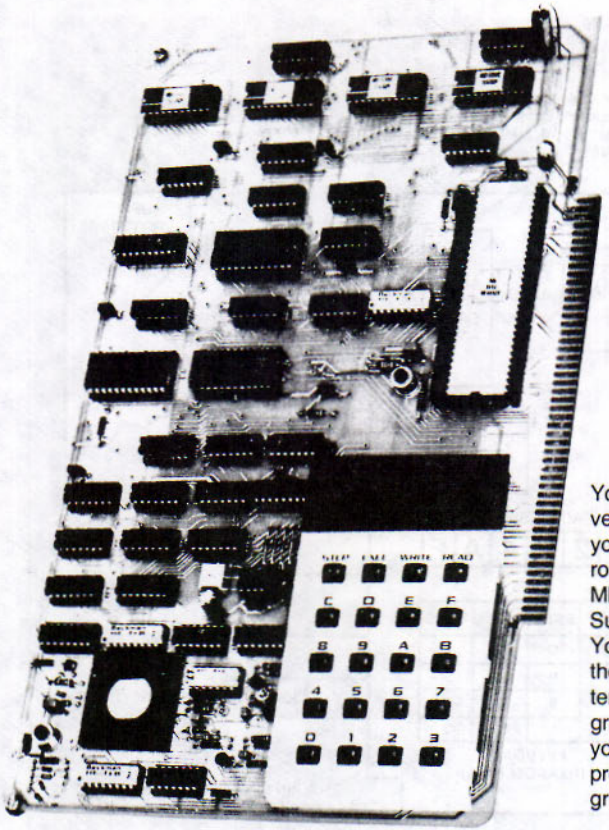
ADDRESS
LATCHED (A0)



(2b.)

Figure 2. TIMING DIAGRAM

NOW . . . with a Rockwell $495 XPO-I System Development Microcomputer You Can Customize a $3 PPS-4/1 Microcomputer for Your Million Dollar Product . . .



# XPO-I

PPS-4/1
SYSTEM DEVELOPMENT
MICROCOMPUTER

PPS PMOS PRODUCTS

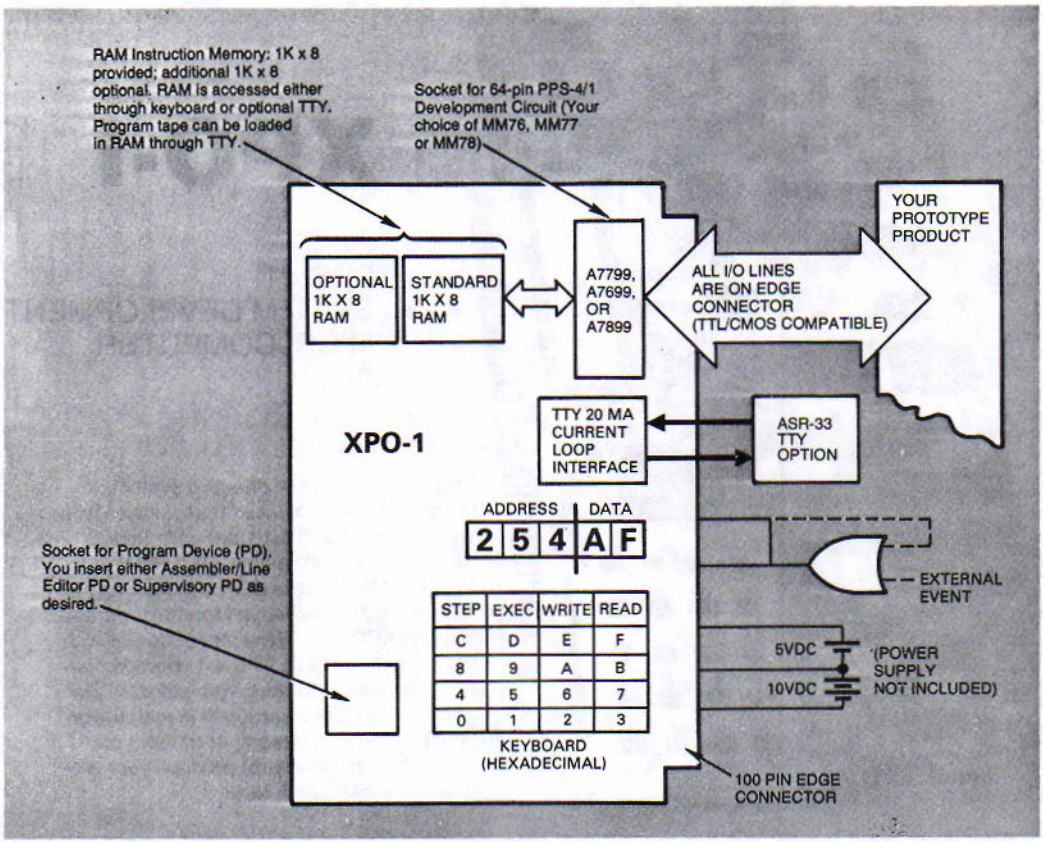
You buy XPO-1 as an effective system development microcomputer. It's furnished with your choice of a PPS-4/1 one-chip microcomputer Development Circuit (MM76, MM77 or MM78) and a device containing the Supervisory (Utility/Debug/Monitor) program. You use XPO-1 to: 1) familiarize yourself with the capabilities of the PPS-4/1 microcomputer; 2) develop and debug your software program; 3) exercise this program in real time on your prototype equipment; 4) modify your program as necessary; 5) produce your program as a ROM mask tape.

## XPO-I — Self-Contained, Tested

One PC board: CPU, RAM, I/O, clock, keyboard, display; tested, ready to use; supplied with XPO-I Instruction Manual, PPS-4/1 Programmer's Manual and PPS-4/1 Product Description.

**Rockwell International**

# This XPO-I Functional Diagram Shows You the Power of the PPS-4/1 System Development Microcomputer . . .




## Three XPO-I Models Currently Available

| XPO-I MODEL | INCLUDED SYSTEM DEVELOPMENT DEVICES | PRICE, EACH |
|---|---|---|
| XPO-I/76 | MM76 Development Circuit (A7699), Supervisory PD (A7800) | $495 |
| XPO-I/77 | MM77 Development Circuit (A7799), Supervisory PD (A7800) | $495 |
| XPO-I/78 | MM78 Development Circuit (A7899), Supervisory PD (A7800) | $495 |

| PART NUMBER | SYSTEM DEVELOPMENT DEVICES | PRICE, EACH |
|---|---|---|
| A7699 | MM76 Development Circuit | $ 45 |
| A7799 | MM77 Development Circuit | $ 55 |
| A7899 | MM78 Development Circuit | $ 65 |
| A7806 | MM76 Assembler/Editor Program Device (PD) | $100 |
| A7807 | MM77 and MM78 Assembler/Editor PD | $100 |
| A7800 | Universal PPS-4/1 Supervisory PD | $ 50 |

(NOTES: PPS-4/1 Development Circuits are identical to production versions, but have no ROM. Special internal leads connect to external instruction memory (RAM). Program Devices (PD) are specially programmed PPS-4/1 microcomputers. You need buy only one XPO-I model to get the board for all three PPS-4 families. You can quickly see what additional devices you must purchase for other families.)

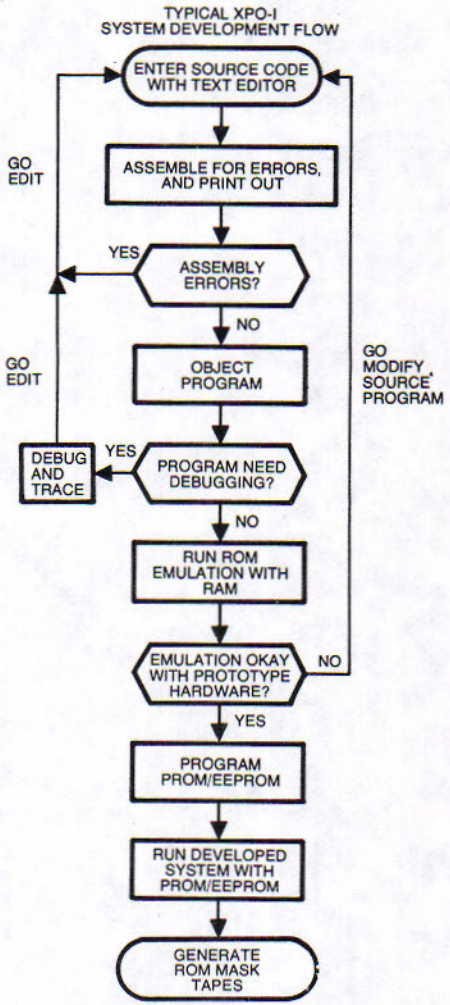
## XPO-I Has Powerful System Development Functions:

## Supervisory (Utility/Debug/ Monitor) Program

By providing this program in the ROM of a PPS-4/1 one-chip microcomputer, the following functions are controlled: *Keyboard and display control:* for most operations, the display shows current address in hexadecimal code and data contained at the indicated address. *TTY control:* including reading, punching and verifying binary tapes. *Program Execution:* sets up to 12 addressed breakpoints and allows single step or real time program execution; displays and alters Data RAM, Instruction RAM and CPU registers; allows program execution to continue from breakpoint.

## Assembler/Line Editor Program

Again, by providing this program in a PPS-4/1 ROM, a large number of functions are effectively controlled: controls the TTY and RAMs during assembly and edit; allows symbolic source and provides a binary object output; accepts up to seven character symbols (1K bytes in Symbol Table with optional expansion to 2K bytes); during edit, you can copy, delete, or insert changes or additions on a line basis.




MICROMODEM
MODULES

MICROMODEM
MODULES

DOCUMENT NO. 81800M01
REVISION 2, JAN. 1979

PART NUMBER
R24

Rockwell

**MODEM PRODUCTS**
**PRODUCT PREVIEW**

# R24 2400 BPS Modular Modem

## INTRODUCTION

The Rockwell R24 is a high-performance synchronous 2400 bps DPSK modem. Utilizing MOS/LSI technology, the R24 consists of three modular building blocks. It is innovatively designed to enable its economic integration by system designers in a broad range of communication, computer, and control equipment.

Having Bell 201 B/C and CCITT V.26 compatibility, the modular R24 offers the user sufficient flexibility to customize a 2400 bps modem to his specific packaging and functional requirements. With a minimum amount of interface circuitry, the modem can be configured for operation on dedicated lines or on the general switched network.

## MODULE VERSATILITY

The versatility of the R24 design is achieved by dividing the modem's functions into three modules. Each module is encased in a plastic package which can be plugged into standard connectors or can be wave soldered on one or more printed circuit boards. The pin spacing is on 100 mil. centers.

## R24 MODEM EVALUATION

To facilitate evaluation and design-in of the R24 modem for new and existing equipment designs, Rockwell has packaged the three modules with interfacing circuitry on an R24 Modem Evaluation Board (R24MEB) -- see right. Supplied with complete Applications Notes, the R24MEB can be easily combined with terminal systems for real-time performance evaluation.

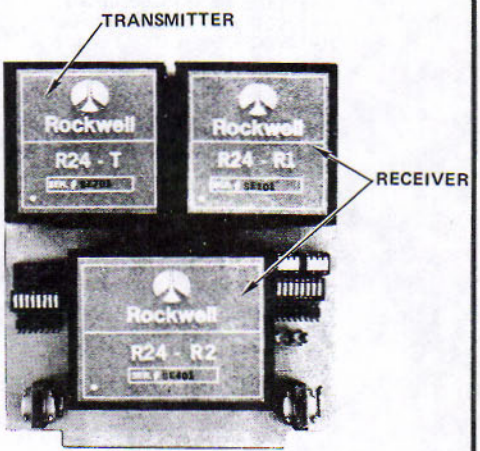
### MODULE DIMENSIONS

| | W | L | H | PINS |
|---|---|---|---|---|
| R24-TRANSMITTER | 2-3/4" | 2-3/4" | 1/2" | 39 pins |
| R24-R1 RECEIVER | 2-3/4" | 2-3/4" | 1/2" | 15 pins |
| R24-R2 RECEIVER | 2-3/4" | 3-1/2" | 1/2" | 31 pins |

(Metric Equivalents: 2-3/4": 69.85 mm; 1/2": 12.70 mm; 3-1/2": 88.90 mm)

## FEATURES/BENEFITS

- LSI high density; low power
- 2400/1200 bps modes
- Transmitter-Differential phase modulation
- Receiver-Coherent phase detection
- Bell 201 B/C, CCITT V.26 compatible
- CCITT A/B and U.S. phase options
- Operating modes:
  - Half duplex (2 wire)
  - Full duplex (4 wire)
- Outstanding performance over unconditioned lines
- LSTTL/CMOS compatible digital interface
- Fixed compromise equalizer
- V.27 compatible scrambler/descrambler
- Answer-back tone generation
- Clear-to-send delay options
- New sync option provides rapid resynchronize
- Maximum power consumption approximately 3 watts
- Total module area less than 25 sq. in.



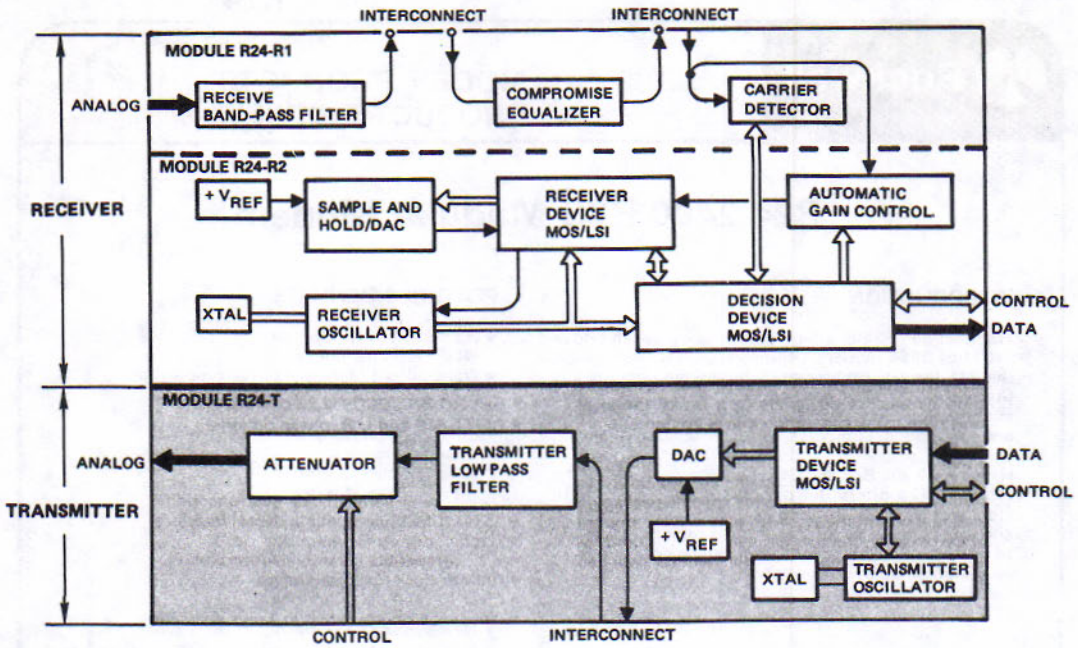

R24 MODEM EVALUATION BOARD (R24MEB)





Specifications subject to change without notice

## R24 FUNCTIONAL DIAGRAM




### POWER SUPPLIES:

+5VDC ± 5% at 100ma (max.)
+12VDC ± 5% at 75 ma (max.)
−12VDC ± 5% at 125ma (max.)

### ENVIRONMENTAL SPECIFICATIONS

Operating temperature: 0°C to 60°C
Storage temperature: −40°C to +80°C
Relative humidity: to 95% (non-condensing)

For more information contact your local Rockwell Representative or Regional Office, or Telecom/Subsystem Marketing, Rockwell Microelectronic Devices, P.O. Box 3669, Anaheim, CA 92803. TWX 910-591-1698. Telephone: (714) 632-5535.

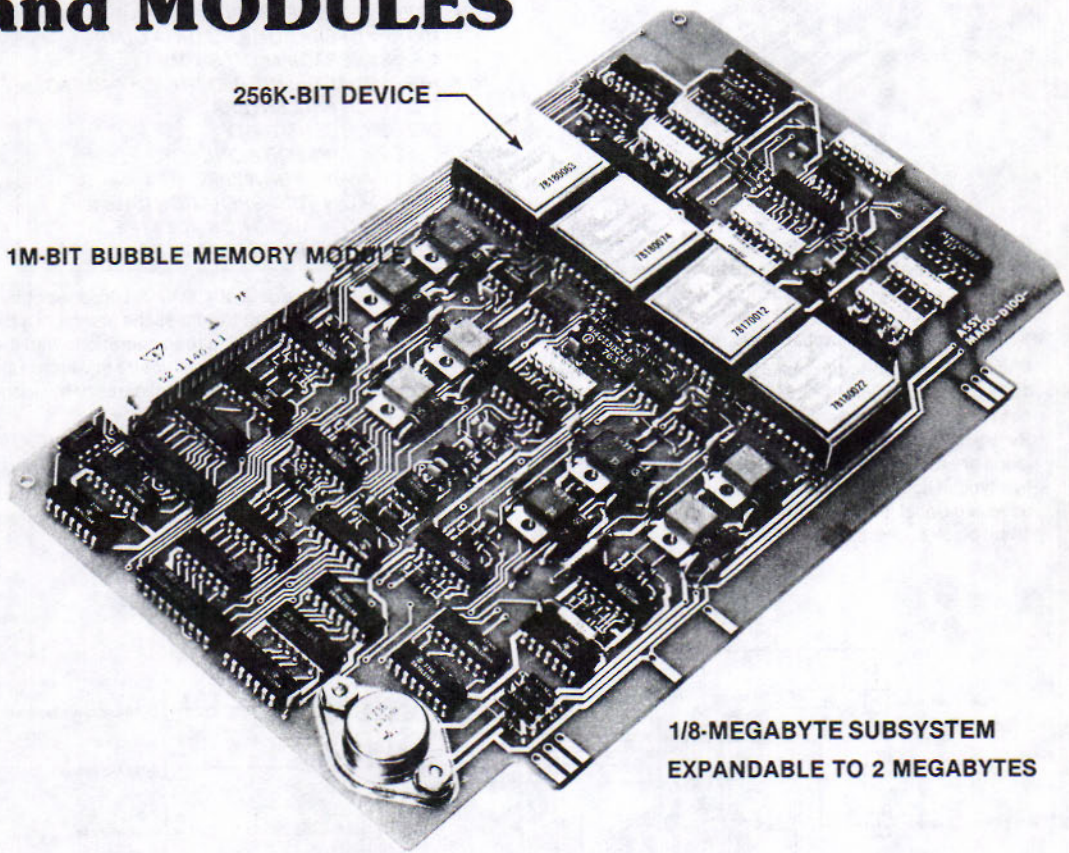
Rockwell International

BUBBLE
MEMORY
PRODUCTS

## the future in memories is here now . . .

# Rockwell

# BUBBLE MEMORY DEVICES and MODULES




**1/8-MEGABYTE SUBSYSTEM**
**EXPANDABLE TO 2 MEGABYTES**

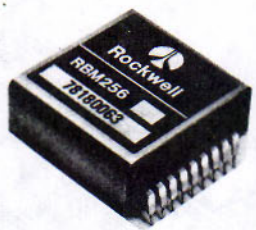
BUBBLE MEMORY PRODUCTS

The characteristics of bubble memory systems ideally suit them as auxiliary memory for microprocessor-based equipment and as primary memory for recorder-type applications. Solid-state reliability, per-bit cost and low access times also qualify


non-volatile bubble memories to fill the "gap" between semiconductor RAMs and bulk storage systems (especially fixed and moving head disks and tapes) in computers. Rockwell International has committed resources to a bubble memory business dedicated to providing you with technological leadership and volume production.

Rockwell International

# 256K-BIT block-access BUBBLE MEMORY DEVICE




- *REPLICATE/READ BLOCK ARCHITECTURE*
- *1025 BLOCKS OF 260 BITS*
- *150 KHz OPERATION AND DATA OUTPUT*
- *< 4 mS AVERAGE ACCESS TIME*
- *18-PIN DUAL-IN-LINE WIDE-TRACK PACKAGE: 0.1 INCH PIN CENTERS*
- *DETECTOR SENSITIVITY:*
  *> 2.2 mV/mA FOR A ONE*
  *< 1.0 mV/mA FOR A ZERO*
- *– 10°C TO + 70°C OPERATION (case temp.)*
- *– 50°C TO + 100°C NON-VOLATILE, NON-OPERATING STORAGE*

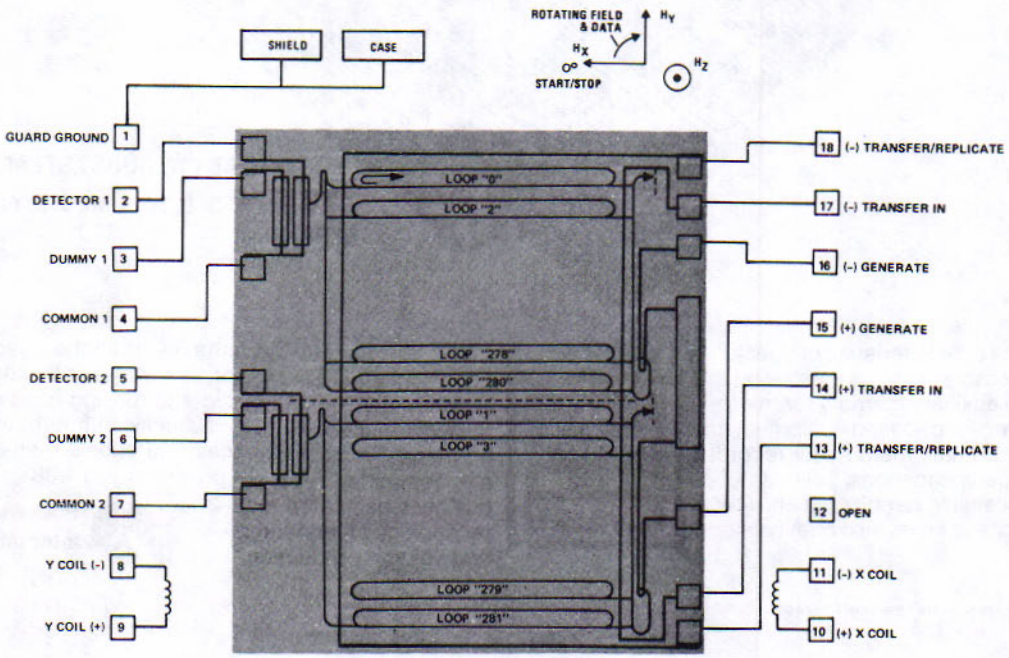
The Rockwell RBM256 bubble memory device stores 266,500 bits of data. It represents the latest advances in materials, architecture and packaging. Its reliability has been engineered on the basis of accelerated test data accumulated over a number of years.

The RBM256 is composed of 282 loops, each containing 1025 bubble positions. The device operates with a 260-bit data block, thus using only 260 of the available 282 loops. Binary data are stored in 256 loops and the remaining four loops are available to hold system "housekeeping" bits. In a typical application where eight RBM256 devices are used in parallel, the extra bits may be used to provide a 16-bit block address header and a 16-bit CRCC word suffix.

The RBM256 transfers data at 150 KHz, taking less than four milliseconds (average) to access the first bit of a block. Throughput is preserved during read operations with the device's replicate/read block architecture in which bubbles read at the detectors are actually duplicates of the loop-resident bubbles.

Packaged in a 18-pin, molded plastic DIP, the RBM256 occupies only 1.2 in. x 1.2 in. It consumes only 820 mW of power and offers the advantage of – 10°C to + 70°C case temperature operation. Non-operating, non-volatile storage range is – 50°C to + 100°C.

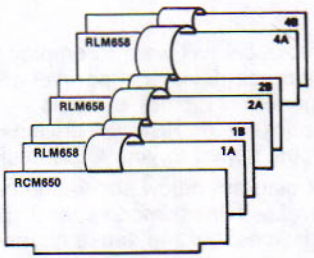


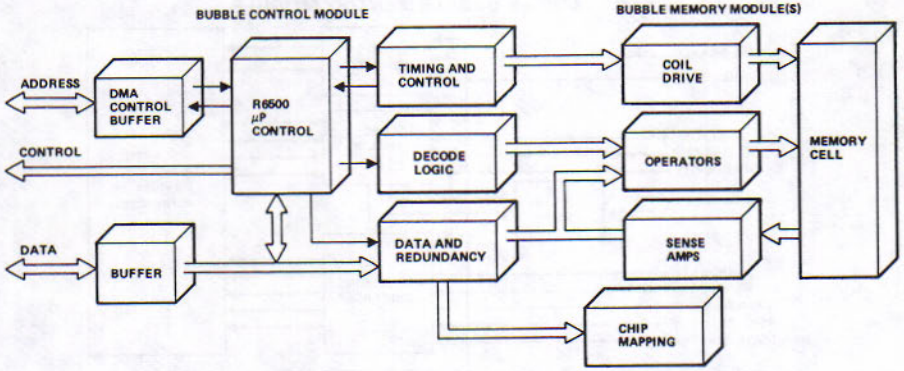


# BUBBLE MEMORY SYSTEM APPLICATIONS

As you can see from the preceeding pages, Rockwell's bubble memory products make it easy to get your development programs up and running, quickly and efficiently

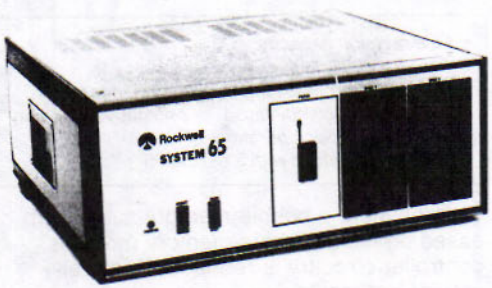
The RCM650 Bubble Memory Controller and the RLM658 Linear Module are designed to form a cost-effective subsystem. The RCM650 Controller supports up to 16 RLM658 Modules, so your system capacity can be readily expanded up to 2 megabytes.




## BUBBLE MEMORY DEVELOPMENT SYSTEM

Rockwell offers you an easy way to get bubble memories up and running in your development lab. It's done by ordering a ¼-megabyte bubble memory subsystem option (one RCM650 Controller and two RLM658 Linear Storage Modules) installed in a SYSTEM 65 microcomputer development system. By coupling the versatility of SYSTEM 65 with the reliability of bubble memory storage, your bubble memory development can begin immediately.




Rockwell's SYSTEM 65 is one of the industry's most powerful microcomputer development systems. Based on the popular R6502 CPU, it comes standard with such features as two mini-floppy disk drives and 16K bytes of static RAM (both totally user-dedicated), plus ROM-resident debug, monitor, symbolic text editor and two-pass assembler programs.

SYSTEM 65 includes six vacant slots for adding additional memory and I/O modules, but with an auxiliary card cage you can expand to the full 2-megabyte bubble memory subsystem capability.

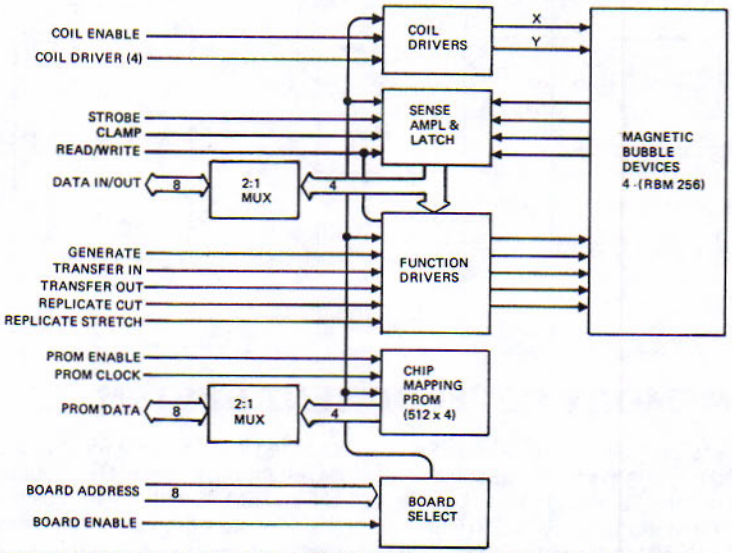
# BUBBLE MEMORY LINEAR MODULES

Since most users will want to employ bubble memory storage devices in parallel configurations — generally nibbles or bytes — Rockwell offers to package its RBM256 devices in linear modules best suited to your OEM design.

The block diagram below shows the elements of a generalized linear module, and shows not only the devices, but the sense channels, coil drivers and operator logic (transfer, replicate and generator pulses) needed to support them.

The chip-mapping PROM retains redundancy information (good- and bad-loop maps) for the module's devices. The system controller uses this PROM information to skew and deskew the block data streams. This method ensures minimum difficulty during incoming inspection, system development and "shmooing".

**LINEAR BUBBLE MEMORY MODULE**




## 1-MEGABIT LINEAR BUBBLE MEMORY MODULE (RLM658)

The RLM658 is a pre-packaged linear module which provides one megabits of bubble memory storage, via four parallel RBM256 devices.

This module operates at 100 kilobytes per second and when used in conjunction with an appropriate controller, is compatible with Rockwell's SYSTEM 65 and many 6800 microcomputer development systems.

The RLM658 is designed to be used in combinations of two to 16 modules in a system environment providing from 256 kilobytes to 2 megabytes of storage.

- *One-megabit capacity*
- *Four RBM256 devices in parallel*
- *Designed for combining for byte-wide operation*
- *Designed for combining up to 2-megabyte capacity*
- *100-Kilobyte/Sec operation*
- *Totally compatible with SYSTEM 65*

To implement a bubble memory subsystem based on linear bubble memory modules, controller circuitry is required. Rockwell provides versatile approaches which are described inside this brochure.

# BUBBLE MEMORY CONTROLLER MODULES

Since each user's application is different, Rockwell firmly believes that the only practical approach to bubble memory control is to consider the unique requirements of each individual system. Especially in the design phase, off-the shelf controllers are restrictive.

Using the knowledge gained through years of applying programmable microprocessors to system solutions, Rockwell can produce the simplest, most cost-effective controller for your particular OEM application.

## BUBBLE MEMORY CONTROL MODULE (RCM650)

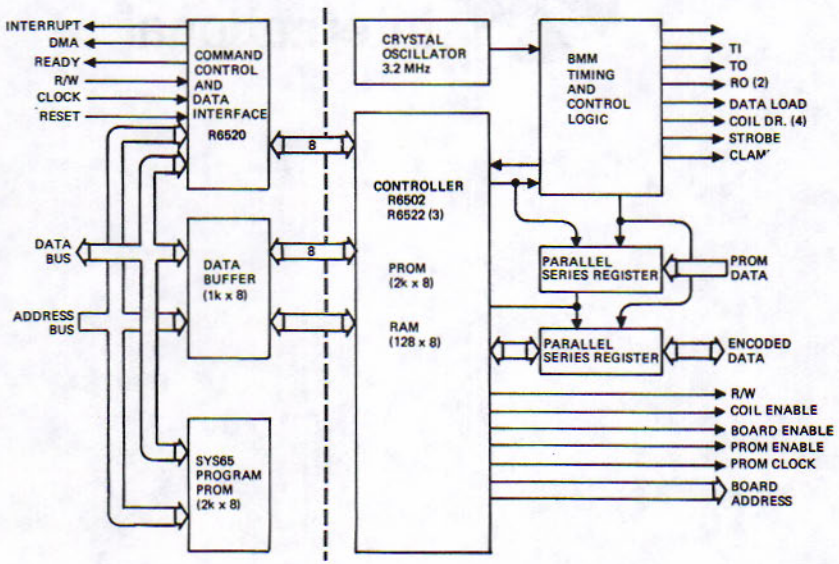
The RCM650 is designed to complement the one-megabit RLM658 linear module in SYSTEM 65 applications. It is totally software compatible with SYSTEM 65 and the 6502 microprocessor, and can control from one to 16 RLM658 modules.

The RCM650 block diagram below illustrates the two fundamental types of circuitry on the module. Circuits to the left of the dashed line are required for SYSTEM 65 compatibility. Circuits to the right of the dashed line are required to service the bubble memory.

- *Controller for one to 16 RLM658 modules*
- *Software compatible with SYSTEM 65 and 6502 microprocessor*
- *Bus compatible with SYSTEM 65*
- *Byte parallel operation in 256-byte blocks*



**BUBBLE MEMORY CONTROL MODULE**



# OPTIONS FOR OEM BUBBLE MEMORY SYSTEM DESIGN

Rockwell's philosophy is to provide system designers with bubble memory products that facilitate the design and evaluation of your memory subsystems.

The architecture and parameters of the RBM256 device were established after extensive discussions with system designers. The device specifications have won universal acceptance.

Availability of a self-contained development system like the SYSTEM 65 with bubble memory option was advocated by many system designers interested in compressing evaluation and design time. However, to provide the widest possible applications flexibility, Rockwell also supplies general and specific module approaches.

To assist you in achieving the unique topology, architecture, board size and bus structure you want for your equipment design, Rockwell has established an experienced Bubble Memory Design Team. You can tap this engineering support by contacting Rockwell International, Bubble Memory Products, D/822, RD45, P.O. Box 3669, Anaheim, CA 92803. Telephone: (714) 632-3321.

For information on prices, delivery and ordering of Rockwell Bubble Devices, Linear Bubble Memory Modules, Controller Modules or the RMS65 Development System, contact your local Rockwell Representative or the Rockwell Sales Office nearest you.



Rockwell International

DOCUMENT NO. D-RBM256
REV. 1, FEBRUARY 1979

PART NUMBER
**RBM256**

Rockwell

# BUBBLE MEMORY PRODUCTS DATA SHEET

## 256K-BIT BUBBLE MEMORY DEVICE

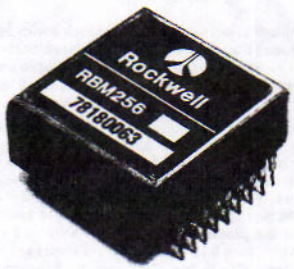
### OVERVIEW

The Rockwell RBM256 bubble memory device stores 266,500 bits of data. It represents the latest advances in materials, architecture and packaging. Its reliability has been engineered on the basis of accelerated test data accumulated over a number of years.

The RBM256 is composed of 282 loops, each containing 1025 bubble positions. The device operates with a 260-bit data block, thus using only 260 of the available 282 loops. In a typical application binary data are stored in 256 loops and the remaining four loops are available to hold system "house-keeping" bits. Where eight RBM256 devices are used in parallel, the extra bits may be used to provide a 16-bit block address header and a 16-bit CRCC suffix.

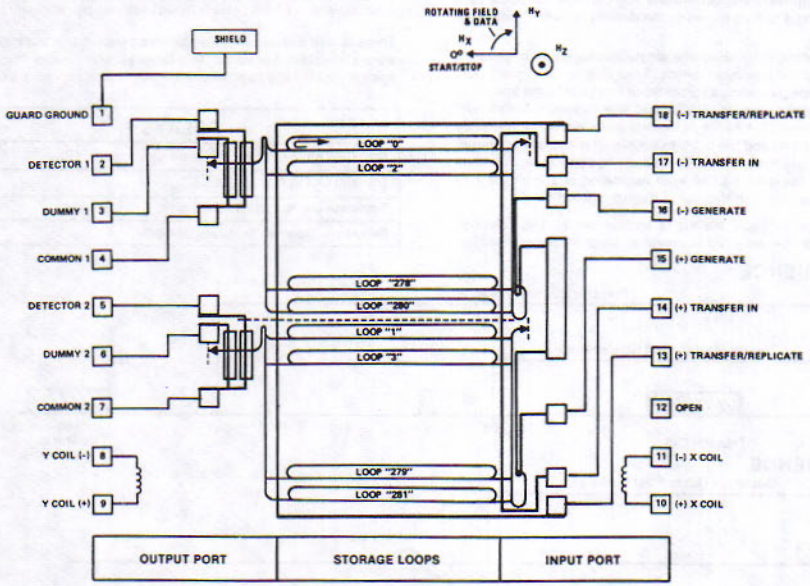
The RBM256 transfers data at 150 KHz, taking less than four milliseconds (average) to access the first bit of a block. Throughput is preserved during read operations with the device's replicate/read block architecture in which bubbles read at the detectors are actually duplicates of the loop-resident bubbles.

Packaged in an 18-pin, molded plastic DIP, the RBM256 occupies only 1.2 in. x 1.2 in. It consumes approximately one watt of power when operating; average power decreases dependent on duty cycle. The RBM256 offers – 10°C to + 70°C case temperature operation at 100 KHz and – 10°C to + 65°C case temperature operation at 150 KHz. Non-operating, non-volatile storage is – 50°C to + 100°C.




### FEATURES

- Replicate/read block architecture
- 1025 blocks of 260 bits
- 150 KHz operation
- < 4 mS average access time
- 18-pin dual-in-line wide-track package; 0.1 inch pin centers
- Detector sensitivity:
  > 2.2 mV/mA for a one
  < 1.0 mV/mA for a zero
- – 10°C to + 65°C operation @ 150 KHz (case temp.)
- – 10°C to + 70°C operation @ 100 KHz (case temp.)
- – 50°C to + 100°C non-volatile, non-operating storage



## FUNCTIONAL DESCRIPTION

The 256K-bit bubble device uses a block replicate access design, as shown in the architecture diagram. Data blocks are stored in the loops with the odd bits on one side of the die and the even bits on the other. A block is formed using the same relative bit position in each loop. Thus, there are as many blocks as bit/loops, and a block length equals the number of loops. Functionally the die is formed of three parts: a storage area composed of the loops, an output port composed of replicate/transfer switches and magnetoresistive detectors, and an input port composed of twin generators and a transfer-in switch. The loops are arranged as long, two bit wide recirculating registers. The ports are at half way points at either end of the loop. Surrounding the active area of the die is a guardrail composed so that bubbles can traverse only from the active area to the inactive area at the die edge.

Redundancy is utilized to increase yield and reduce device costs. 260 of the 282 minor loops are guaranteed to meet specifications. The host system must avoid writing bubbles into the bad loops and ignore any information read from them. Defective loops are identified during factory testing. A list of these is supplied with the device.

At the Output Port of the die, the loops are tangent to a series of replicate/transfer switches. When activated by the appropriate common current pulse, both the odd and even halves of a block of data are either replicated from or transferred out of the loops into a pair of read tracks. The valid information sites alternate with idle sites. The bubbles propagate along the read tracks to the detectors and then through the guardrail and out of the active die area. The number of steps from loop 0 to the detector (84 steps) and loop 1 to the detector (85 steps) differ by one. Thus, from the detectors continuous, interlaced data emerges.

Detection uses the magnetoresistive effect. The two sets of active and dummy detectors are connected in bridge configurations to give a high degree of noise cancellation. Each detector is composed of a 260 high stack of chevrons. In the detector, the "right circular cylindrical" domain is stretched into a "right elliptical cylindrical" domain that is the same width as a bubble, but as long as the 260 chevron stack. The flux from the stretched bubble interacts with the permalloy detector pattern and changes its resistance. The resistance change is translated into a difference signal by a current passing down the two identical detectors—the active detector containing the information (bubble or no bubble) and the dummy detector never containing a bubble. The dummy is placed in the adjacent chevron stack so that maximum matching occurs and any common mode noise is minimized. When a bubble moves to the dummy detector, that detector is not used.

A pair of generators, consisting of a single conductor path, generate serially blocks of data equal in length to the number of minor loops. The bubbles propagate along a pair of input tracks until the first bit in the block is opposite loop "0". On the odd side of the die, the second bit is opposite loop "1'. A series of transfer switches are activated by a single current pulse and the bubbles are simultaneously transferred into the appropriate minor loops. The remaining bubbles — odd numbered bits from the even half or even numbered bits from the odd half — are subsequently shifted out through the guard rail.

Within the device package, the die is surrounded by two orthogonally wound coils that are used to create an electronically generated magnetic flux that forces all of the bubbles to advance one position for each 360° rotation.

Two orthogonal coils, X and Y, are driven 90° out of phase with X leading Y to provide a clockwise rotating magnetic field in the plane of the bubble device. This results in circulation of the magnetic domains around the device circuit loops and into proper orientation with the device operator circuit elements enabling read, write, transfer-in and transfer-replicate functions to be performed. The coils may be driven either continuously (within prescribed operating conditions) or in a stop-start intermittent mode without data loss.

Both X and Y coils can be driven from a common voltage supply with either sine, trapezoid or triangle current wave forms. A triangle drive is recommended as being most consistent with digital switching drivers.

Coil drive and electrical load data are listed in the data tables for triangle drive operation with field rates of 100 KHz and 150 KHz. Operation at other frequencies will result in appropriate proportional change in drive voltage requirements, AC resistance, and power dissipation.

Basic non-volatility is created by the use of permanent magnets arranged so that their flux is perpendicular to the surface of the die. This flux satisfies the stability criteria that permits right circular cylindrical domains (bubbles) to exist. The permanent magnets are chosen with a temperature coefficient that matches the bubble die so that the bubbles have nearly constant diameter over the temperature range.

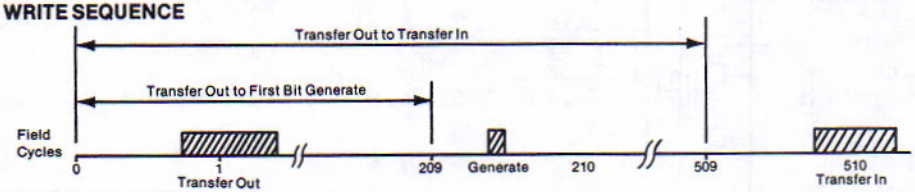
Non-volatility is guaranteed for data in the storage loops and the input port. Non-volatility of data in the output port is only assured during the uninterrupted completion of a block operation. Thus, an operation in the output port should not be interrupted. System timing should be arranged so that one complete rotational cycle is completed before a replication function is attempted.

The following shows the timing relationships between the different functions during the writing and reading of one block of data. The delays given are integral numbers of drive field cycles measured from the 0° drive field reference point just preceding the first function, to the 0° reference point just prior to the second function. Timing of a function within a field cycle is listed in the electrical characteristics.

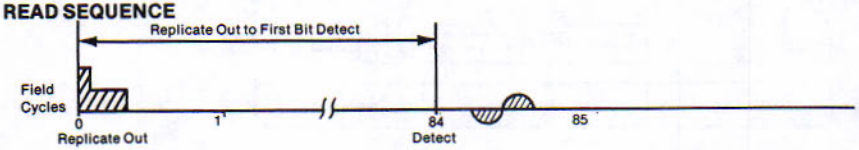
There is also a minimum delay between successive replicate-out and a transfer-out (or vice versa). This is necessary to insure that the major track is clear of any bubbles prior to the transfer or replicate function.

| DELAYS | |
|---|---|
| Transfer Out to First Bit Generate | 209 |
| Transfer Out to Transfer In | 509 |
| Replicate Out to First Bit Detect | 84 |
| Repetitive Transfer/Replicate Operator | 282 |

## WRITE SEQUENCE

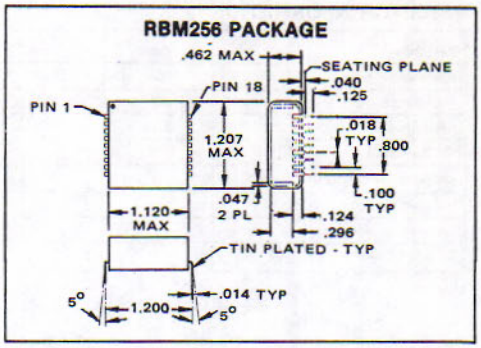



## READ SEQUENCE



## GENERAL PARAMETERS

Number of minor loops: 282
Useable minor loops: 260
Minor loop bits: 1,025
Useful chip bits: 266,500
Mounting footprint: (1.2 in)$^2$
Weight: 36 gm




## ABSOLUTE MAXIMUM RATINGS

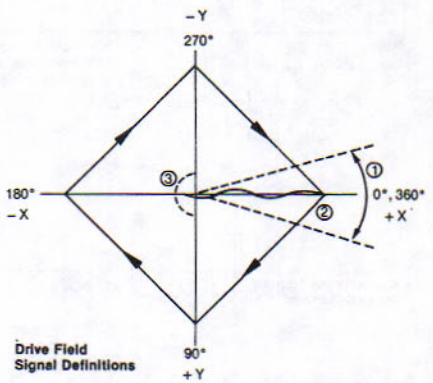
| Parameter | Min. | Typical | Max. | Units |
|---|---|---|---|---|
| Storage Temperature | −55 | | +125 | °C |
| Non-Volatile Storage Temperature | −50 | | +100 | °C |
| Operating Temperature (Case)<br>@ 100 KHz<br>@ 150 KHz | <br>−10<br>−10 | | <br>+70<br>+65 | <br>°C<br>°C |
| Generator Dissipation | | 20* | 60Δ | mW |
| Transfer-In Dissipation | | 0.75* | 200Δ | mW |
| Replicate/Transfer Dissipation | | 1.7* | 200Δ | mW |
| Detector Element Dissipation (4/Device) | | 35 | 150Δ | mW |
| Interelement Voltage | | | 100 | V |
| Relative Humidity | | | 95 | % |
| External Magnetic Fields | | | 50 | Oe |

*Normal operation averaged over a block transaction.
ΔContinuous long-term dissipation without damage.

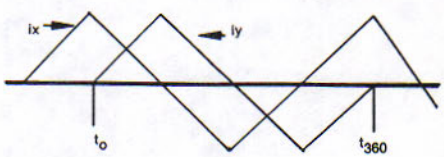
## DRIVE INFORMATION

| Parameter | Field Rate 100 KHz | Field Rate 150 KHz | Units |
|---|---|---|---|
| Start/Stop Direction ① | 0 ± 20 | 0 ± 20 | Deg. |
| Peak Drive Field ② | 55 ± 5 | 55 ± 5 | Oe |
| Stop Undershoot (Max) ③ | 1.0 | 1.0 | Oe |
| Coil Differential Voltage | 11 ± 0.4 | 16 ± 0.4 | V |
| Coil Power Loss | 0.72 | 0.90 | W |
| X-Coil | | | |
| Inductance | 44 ± 2 | 44 ± 2 | μH |
| DC Resistance | 3.9 | 3.9 | Ω |
| AC Resistance | 3.5 | 4.5 | Ω |
| Peak Current | 0.54 | 0.54 | A |
| Loss | 0.40 | 0.46 | W |
| Y-Coil | | | |
| Inductance | 38 ± 2 | 38 ± 2 | μH |
| DC Resistance | 1.6 | 1.6 | Ω |
| AC Resistance | 2.2 | 3.0 | Ω |
| Peak Current | 0.65 | 0.65 | A |
| Loss | 0.32 | 0.44 | W |
| Bias Field | 155 | 155 | Oe |
| Bias Margin (Min) | 8 | 8 | Oe |

**Note:** All values nominal unless otherwise specified



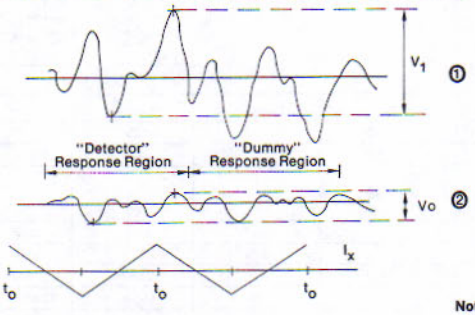

**Drive Field Signal Definitions**




BUBBLE MEMORY PRODUCTS

## DETECTOR INFORMATION

| Parameter | Min. | Nom. | Max. | Units |
|---|---|---|---|---|
| Resistance, Active | 1000 | 1200 | 1400 | Ω |
| Resistance, Dummy | 1000 | 1200 | 1400 | Ω |
| "1" Signal① | 2.1 | | | mV/mA |
| "0" Signal② | | | 1.0 | mV/mA |
| Detector Sensitivity | 1.1 | | | mV/mA |
| Induced Noise/Leg | | | 3.0 | mV |
| Differential Induced Noise | | | 0.5 | mV |
| Detector Current | | 5 | 8 | mA |




**Detector Signal Definitions**

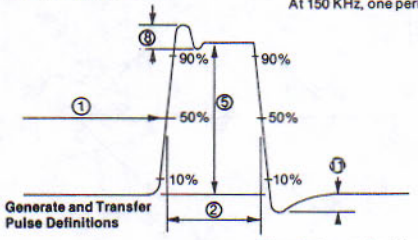
**Note:** Signal polarity shown for detector common at lower potential.

## OPERATOR INFORMATION

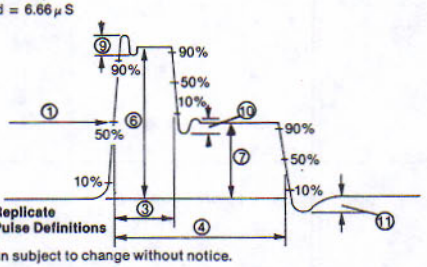
| Operator | Resistance (Ω) | Delay① (Deg.)* | Width (Deg.)* | Amplitude (mA) | Amplitude Deviation (mA) | Maximum Undershoot⑪ (mA) |
|---|---|---|---|---|---|---|
| Generator | 10 ± 1 | 120 ± 30 | 10 ± 5② | 200 ± 25⑤ | ± 28⑧ | 10 |
| Transfer In | 315 ± 30 | 280 ± 30 | 220 ± 20② | 25 ± 5⑤ | ± 2⑧ | 2 |
| Transfer Out | 330 ± 30 | 280 ± 30 | 220 ± 20② | 25 ± 5⑤ | ± 2⑧ | 2 |
| Cut | | 12.5 ± 7.5 | 15 ± 5③ | 100 ± 20⑥ | ± 5⑨ | 3 |
| Replicate | | | | | | |
| Xfer | | | 100 ± 20④ | 35 ± 7⑦ | ± 2⑩ | |

**Note:**
$t_{rise} \leq 100$ nS; $t_{fall} \leq 200$ nS

*360 degrees per period.
At 100 KHz, one period = 10 μS
At 150 KHz, one period = 6.66 μS




**Generate and Transfer Pulse Definitions**




**Replicate Pulse Definitions**

**Note:** Data contained herein subject to change without notice.

DOCUMENT NO. D-RLM658
DECEMBER 1978

PART NUMBER
RLM658

Rockwell

# BUBBLE MEMORY PRODUCTS DATA SHEET

## 1-Megabit Linear Bubble Memory Module

### OVERVIEW

The RLM658 is a pre-packaged "linear" module that provides one megabit of bubble memory storage, via four parallel RBM256 bubble memory devices.

The Module operates on 4 bit "nibbles" at 100 KHz and when used in conjunction with an appropriate controller, is compatible with Rockwell's SYSTEM 65 and many 6800 microcomputer development systems.

The RLM658 is designed to be used singly or in pairs to achieve byte-wide operation. Up to eight single modules or pairs of modules may be combined to provide capacities from 256 thousand to 2 million nibbles or bytes.

### GENERAL DESCRIPTION

The Module contains four 256K magnetic bubble devices using the block access design and organized as a 256K x 4 bit memory. All of the electronics necessary to operate the devices, sense amplifier, coil drivers, generator, and logic circuits are included on the Module. The four devices operate in parallel providing four bit wide data which is routed to 4 of 8 data interface lines, determined by a switch setting. The block length as seen at the output is 282 bits long, of which 260 are guaranteed valid. Typically, four are designated as address bits and 256 as data bits. The identity of the 22 defective loops is contained in a PROM resident on the Module.

The RLM658 is designed to be used in memory systems designed architectually to include storage modules and a controller module. Specifically, the RLM658 was designed as an option to the Rockwell SYSTEM 65 development system for the R6500 family of microprocessors. Since the bus structure of that system precludes communication between modules except through the bus circuitry, two different connectors are used:

- P1 is the standard edge connector for the bus and is used only for voltages and ground.
- P2 is used for bus timing, control, and data signals between the RLM658s and their controller.

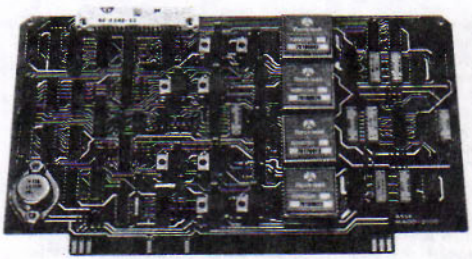
### APPLICATIONS

Designed for a wide range of commercial and industrial applications, the memory introduces a new family of small, efficient, solid-state secondary stores that exploit the many advantages of advanced bubble domain technology.

The memory provides all of the recognized benefits of bubble domain technology — small size and low power . . . high reliability due to the complete absence of moving parts . . . higher storage density than any other type of serial memory . . . and low per-bit cost due to both high storage density and amenability of the technology to automated batch production processing.

In addition, the memory offers its own combination of unique benefits — an extremely large capacity ($10^6$ bits) . . . non-volatility . . . non-destructive readout . . . moderate access time and burst operation for increased flexibility . . . interface busing for multi-modular system operation and growth.

The combination of system benefits give commercial and industrial users a highly versatile, cost-effective memory suitable for use in intelligent terminals, multipurpose displays, super calculators, microcomputer peripherals, back-up for volatile main memories, and data recorders — in systems dedicated to point-of-sale, data entry, store-and-forward, numerical control, industrial control, credit authorization, text editing, and secretarial service functions. Since each Module contains all electronics required to support the storage elements, the user provides only power supply, timing, and data handling capability.



### FEATURES

- Non-volatile data storage
- Non-destructive readout
- TTL compatible interface
- Busable interface — up to 16 modules (2 megabytes)
- One megabit capacity
- 256K x 4 bit memory organization
- 100 KHz operation
- Can be combined, for byte-wide operation
- All linear electronics included
- High reliability — no moving parts
- SYSTEM 65 compatible

### INTERNAL TO RLM658

All linear functions:
- Coil drive
- Generator drive
- Detection system
- Transfer in and out drive
- Replicator drive

TTL interface — busable
Module select decoding
Defective loop data

### EXTERNAL TO RLM658

Power supply
Power fail warning
Clock & subtime generation
Data buffering & formatting
Addressing system
Read/write coordination
Parity or other error correction (if used)





Specifications subject to change without notice.

## FUNCTIONAL DESCRIPTION

The RLM658 interface utilizes TTL levels, with the low level (GND) being active (true) for the operational signals. Each of the various controls is designed to be functionally independent.

When DC power is applied, the signal OAF must be applied 20 milliseconds prior to activation of any control signals. This is required to maintain an internally-generated voltage in the replicate/transfer circuitry. Some users find that this requirement is best satisfied by leaving OAF always active. The memory then is ready to accept commands. All functional elements are interlocked — no command will be recognized without the presence of the module select terms and board enable.

The four bubble devices are driven in parallel by coil driver circuitry controlled by four timing terms, (OAF-ODF) as shown in the Coil Drive Timing Diagram. The COILNF signal activates both the X and Y coil and, with sub-timing, turns the X coil on 90 degrees before the Y coil. Each sub-timing signal must be 90 degrees wide to generate the proper triangular waveforms. Phase zero is defined at the peak of the X current. Thus, the fourth quadrant signal ODF is actually the first applied which establishes the X current.

A minimum run duration will be 509 cycles for writing and 366 cycles for reading one block of data. When the coils are turned off, a minimum of 30 microseconds is required before turning the coils back on.

The sense electronics consist of bridge completion resistors, preamplifier, sense amplifier and latch. Data on the output lines are valid until the next cycle, provided the Module remains enabled and the system remains in the read mode.

The transfer in, transfer out and replicate out circuits are all operated in parallel, whereas the four generate circuits are singularly driven. Each of the functions are accomplished by passing a current pulse through the respective loop on the surface of the bubble die. Since the loop design is for a low duty cycle current pulse, all are AC coupled to protect against burnout due to incorrect input logic signals. The generators may be activated every bit time, but the other signals may not be activated more often than every 282 bit times, (one block length). Further protection circuitry is employed to prevent accidental overusage of the signal.

The die is organized as 282 minor loops of data, each containing 1025 bit positions, for a total of 289,050 bit locations. To reduce chip cost by increasing production yields, only 260 of the 282 loops are required to be operational. At final test of the magnetic cell, the 22 "most marginal" loops are decreed "defective" and identified so they can be bypassed in operation of the device. Every memory system must avoid writing bubble information into these loops and ignore any information read from them. The user controller masks out those loops declared defective. The Module utilizes an on-board PROM to retain the loop redundancy information. Each time a read or write operation is performed, the PROM is accessed to use the loop redundancy information as a data mask.

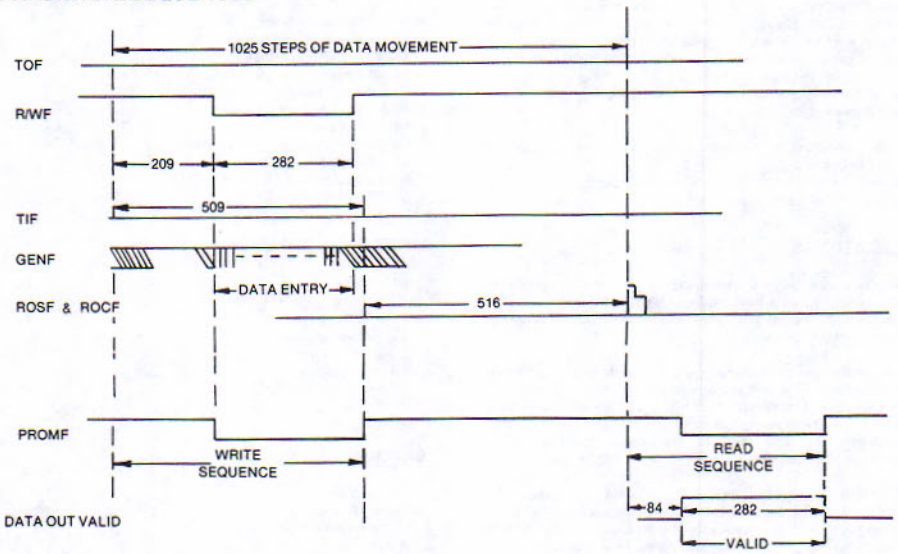
Before entering data into the memory, the addressed block location must be positioned at the transfer-out switch. Activation of the Transfer-Out line (TOF) will empty that block of data on the read track and clear the memory location. After a delay of 209 run cycles, data entry is begun by putting the Read/Write line (R/WF) to ground, which activates the data generator function for all four channels. When R/WF is at ground, the Generate pulse (GENF) must be present and data must be valid on four data input lines. Data being entered must be used in conjunction with the defective loop information so that 260 valid data bits are spaced into the 282 operating loops, interspersed with 22 zero data bits at the location of the bad loops. Eighteen run cycles later, the Transfer-In (TIF) line is activated and a block of data is transferred to the loop storage area of each of the four devices.

Data are read in a non-destructive manner by activating the replicate out signals when the block location is positioned at the transfer out switch corresponding to the desired address and by driving the Read/Write signal high. This stretches and cuts each of the bubbles in the addressed block. One of the resulting bubbles remains in the loop, the other is put into the read track. After a delay of 84 run cycles, the data outputs are valid. This process continues for 282 bits, yielding a 282 x 4 data block. Used in conjunction with defective loop information, the 260 valid data bits are identified.

A minimum 282 cycle delay is required between successive Replicate-Out and/or Transfer-Out commands. This ensures that the read track is entirely clear of bubbles prior to the next transfer or replicate function.



## READ AND WRITE SEQUENCES



## INTERFACE & TIMING DEFINITION

The following signals appear in the interface connector, P2. Power and ground are taken from the edge connector, P1. Signals with an "F" suffix are active in the low (ground) state.

**BRDENF** Board Enable. The module is activated by applying a ground to this line. The signal must be utilized in conjunction with other memory module board enable signals (BRD0F-BRD2F) in order to select the desired module. In multi-board systems, up to 8 modules or module pairs may be enabled.

**COILNF** Coil Enable. This signal activates the coil drive circuitry and initiates data movement. COILNF must be on one complete cycle minimum and off a minimum of 30 microseconds before being energized again. Typically, COILNF remains on for several hundred cycles, to permit access to an entire block of data. It must be on prior to activating any operational signal such as TIF, TOF, ROC, etc.

In the event of a power fail warning, COILNF must be turned off before BRDENF, to prevent loss of data.

**OAF—ODF** Four coil driver timing signals, each defining one quarter of an operation cycle.

As a special case, signal OAF must be true for 25 mS prior to activating COILNF. Most users leave OAF always active. Also note that active operation begins with ODF, which establishes the X field prior to beginning the cycle. It then cycles as the fourth quarter phase.

**DIO0—DIO7** Data in-data out tristate bidirectional line. Ground indicates a '0', high a '1', open when the module is not selected. Input data should change state at 0 nS; Output data changes state at 2500 nS and remains valid until the next 2500 nS point, or until the R/WF line goes low.

**GENF** Generate. A timing signal used to generate a bubble.

**ROCF** Replicate Out Cut. A timing signal which, when energized, replicates a block of data from the storage loops to the read track. ROCF must not occur in the first cycle after COILNF is activated.

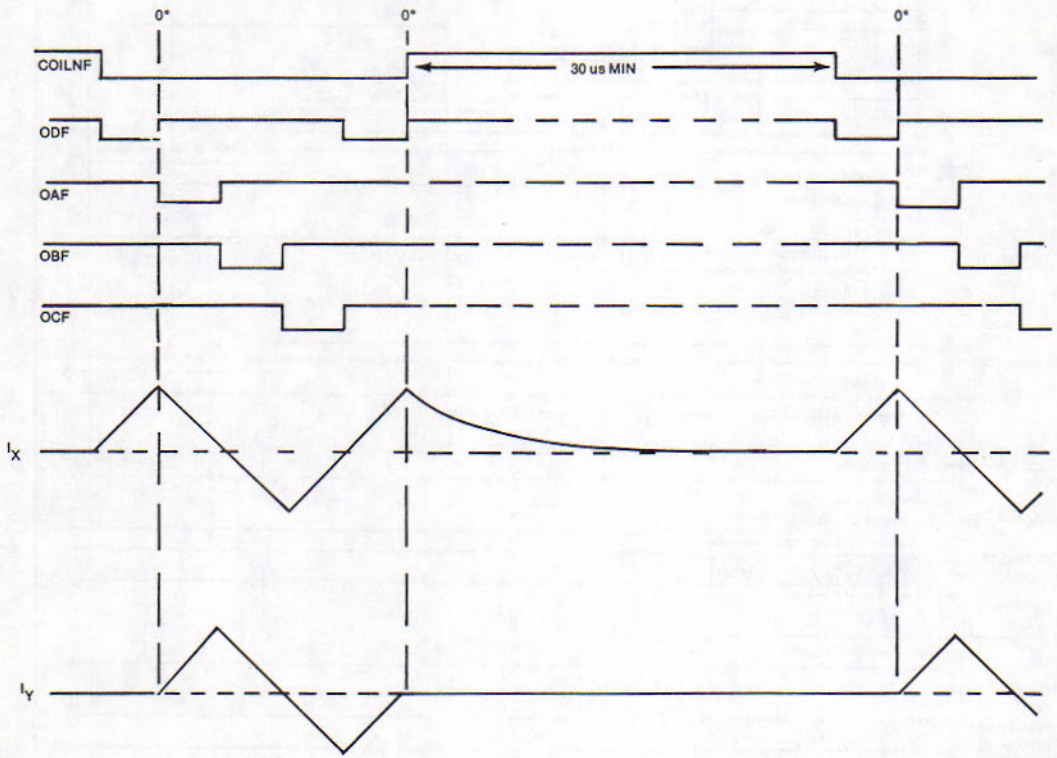
**ROSF** Replicate Out Stretch. Used in conjunction with ROCF for replicating.

**R/WF** Read/Write. Read/Write activates the appropriate operator for the read and write functions. High activates the read (normal condition), ground activates the write. The signal should change state at 0 Ns.

**TIF** Transfer In. A timing signal which, when energized, transfers a block of data from the write track into the storage loops.

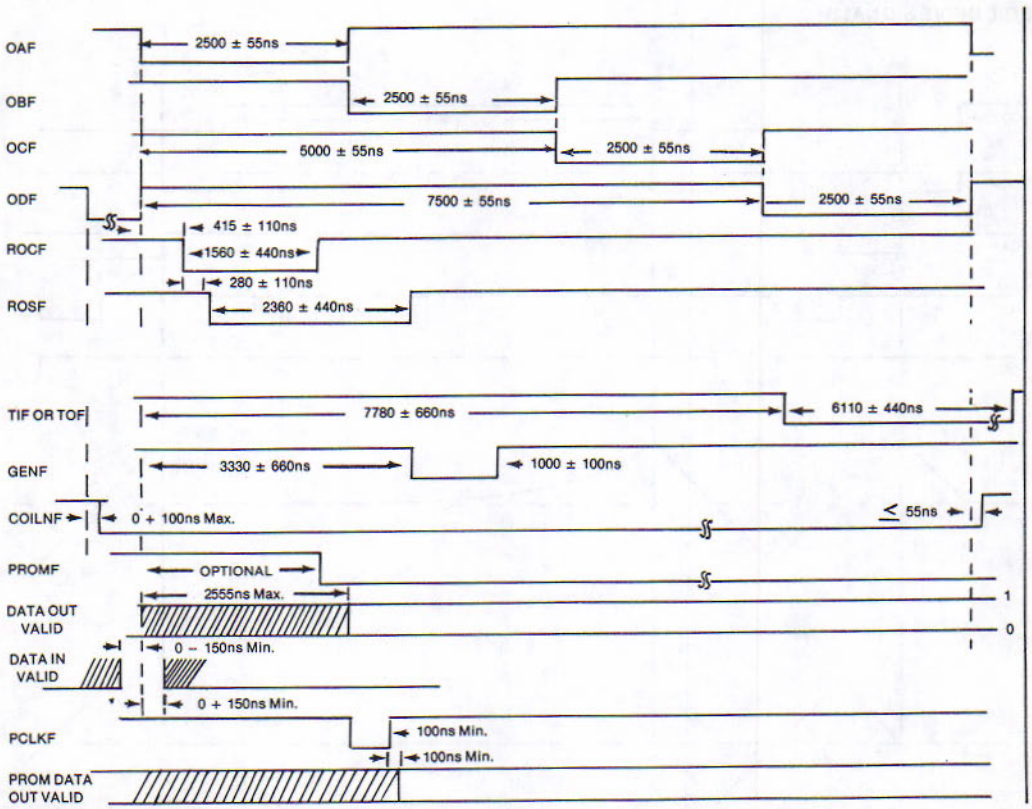
**TOF** Transfer Out. A timing signal which, when energized, transfers a block of data from the storage loops onto the read track.

## COIL DRIVE SIGNALS



| | |
|---|---|
| PROMF | PROM Enable. An enable signal used to start outputting good/bad loop information concurrent with the beginning of the data output or data input. Address zero of the PROM is blown for all four chips and may be used as a marker. Address "one" contains the information of loop "zero" of the bubble memory device. |
| PCLKF | PROM Clock. A 100 KHz clock used to advance the PROM containing the redundancy information. |
| BRD0F—BRD2F | Module Select Addresses. Module select decode lines which select the module. A DIP switch on each module allows each module in a system to be programmed for a unique address. When the plus (+) side is pressed the switch is closed and is grounded. Position 2 is lower bits; 3 is BRD0F; 4 is BRD1F; and 1 is BRD2F. |
| PO0—PO7 | PROM Data Output. Bad loop information, as output from the PROM. PROM outputs appear on either PO1-PO3 or PO4-PO7 as determined by a switch setting. A high level indicates a bad loop. Data on the data output lines is not valid during that cycle. |

## INTERFACE TIMING REQUIREMENTS



## GENERAL PARAMETERS

**Capacity** 1,066,000 bits

**Organization** 1025 blocks
260 x 4 bits/block

| **Access Time (mSec)*** | **Min.** | **Avg.** | **Max.** |
|---|---|---|---|
| Read | 0.84 | 5.96 | 11.09 |
| Write | 2.09 | 7.22 | 12.34 |
| **Cycle Time (mSec)*** | | | |
| Read | 3.66 | 8.78 | 13.91 |
| Write | 5.09 | 10.22 | 15.34 |

*Access time is the time to the first byte read or written; Cycle time is access time plus one block read or write time.

**Modes** Block Read/Block Write

**Data Transfer Rate, Max.** 100,000 nibbles/sec.

| **DC Power Requirements** | **+12V** | **−12V** | **+5V** | **Power** |
|---|---|---|---|---|
| Operating | .60A | .21A | .76A | 13.5W |
| Stand-By | .14A | .21A | .46A | 6.6W |

All voltage tolerances are ±5% at input connector. Voltage sequencing is not required as long as the memory is not being operated.

**Temperature Range**

| | |
|---|---|
| Operating (ambient) | 0°C to 70°C (measured at bubble device case) |
| Non-Volatile Storage | −40°C to +85°C |
| Non-Operating | −40°C to +125°C |

100 linear ft./min. of cooling air is recommended over the component side of the RLM658 to maintain the case temperature of the RBM256 bubble memory devices at or below 70°C.

**Size** 9.75" x 6.0" x 0.65
(247.65mm x 152.4mm x 16.5mm)

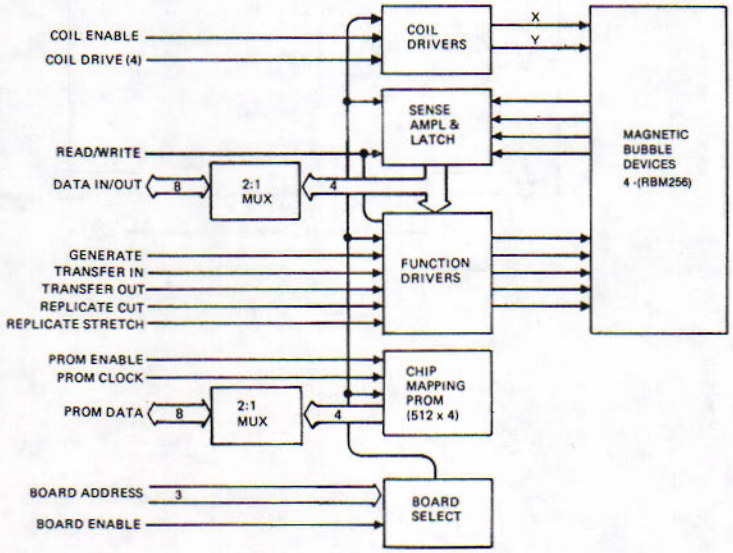
**Weight** 0.88 lb. (400 grams)

**Relative Humidity** Up to 90% without condensation

**Vibration & Shock** That encountered in handling and serving electronic hardware.

### Electrical Characteristics

| Symbol | Characteristic | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{OL}$ | Output Low Voltage ($I_{OC}$ = 16 mA) | | 0.4 | V |
| $I_{OL}$ | Output Low Current | 16 | | mA |
| $V_{OH}$ | Output High Voltage ($V_{CC}$ = 4.75V) | 2.4 | | V |
| $I_{OH}$ | Output High Current ($V_{CC}$ = 4.75V) | 400 | | A |
| $V_{IL}$ | Input Low Voltage | | 0.8 | V |
| $I_{IL}$ | Input Low Current ($V_{CC}$ = 5.25V) | −2.0 | | mA |
| $V_{IH}$ | Input High Voltage | 2.0 | | V |
| $I_{IH}$ | Input High Current ($V_{CC}$ = 5.25V) | 50 | | A |




**RLM658 Module Block Diagram**

## CONNECTOR PIN LISTS

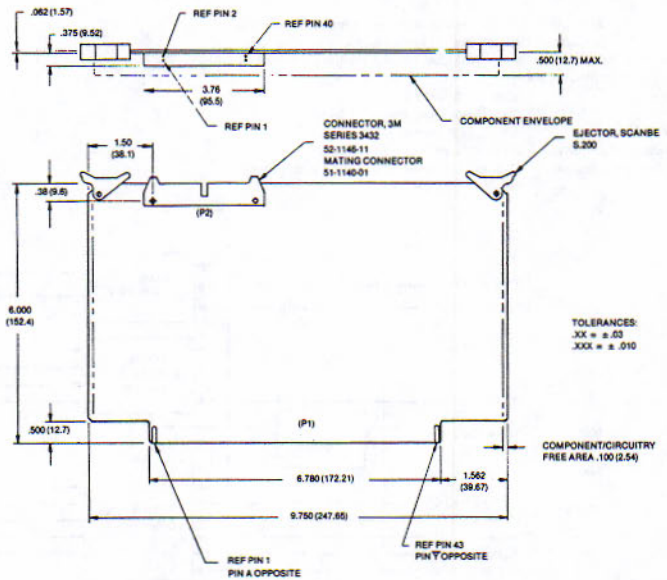
**CONNECTOR P1**

| Pin | Signal |
|---|---|
| 1 | +5V |
| 2 | +5V |
| 3 | +5V |
| A | +5V |
| B | +5V |
| C | +5V |
| 11 | −12V |
| M | −12V |
| 16 | +12V |
| T | +12V |
| 41 | GND |
| 42 | GND |
| 43 | GND |
| W | GND |
| X | GND |
| Y | GND |

**CONNECTOR P2**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | BRD1F | 21 | OAF |
| 2 | BRD2F | 22 | OCF |
| 3 | BRDENF | 23 | PO2 |
| 4 | BRD0F | 24 | PO6 |
| 5 | DIO4 | 25 | SPARE |
| 6 | DIO0 | 26 | SPARE |
| 7 | DIO5 | 27 | GND |
| 8 | DIO1 | 28 | GND |
| 9 | DIO3 | 29 | PO3 |
| 10 | TIF | 30 | ROCF |
| 11 | DIO7 | 31 | PO0 |
| 12 | SPARE | 32 | GENF |
| 13 | DIO6 | 33 | PO4 |
| 14 | SPARE | 34 | PROMF |
| 15 | DIO2 | 35 | PO1 |
| 16 | RWF | 36 | PO5 |
| 17 | OBF | 37 | PO7 |
| 18 | COILNF | 38 | ROSF |
| 19 | SPARE | 39 | TOF |
| 20 | ODF | 40 | PCLKF |

## OUTLINE DIMENSIONS



FILTER
PRODUCTS

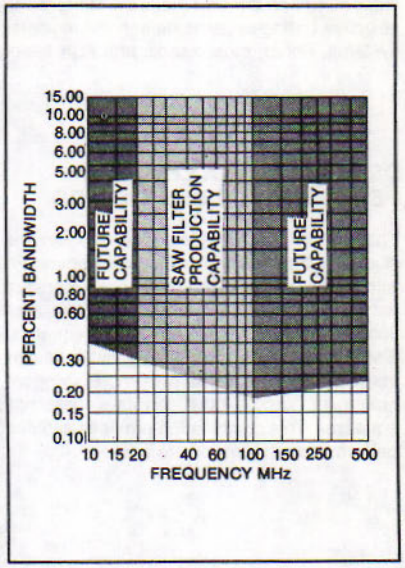
Rockwell

# ROCKWELL-COLLINS FILTER PRODUCTS

## SAW FILTERS

Rockwell produces one of the industry's largest selection of Surface Acoustic Wave (SAW) Filters. SAW Filters are available with center frequencies from 20 MHz to 100 MHz and fractional bandwidths from 0.2 percent to 15 percent.

Rockwell SAW Filters are fabricated on quartz and lithium niobate substrates, and will compliment your design with phase linearity, a flat group delay and controlled amplitude and time response. Further, they're designed to perform in temperatures from -55°C to 85°C, and are produced in microelectronic industry-compatible packages. Rockwell can respond to your custom requirements from 100 to 500 MHz center frequency.

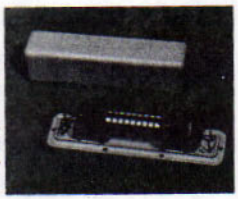



Design Envelope. SAW Filter Percent Bandwidth vs. Frequency Spectrum.

## SAW DELAY LINES

Like the SAW Filters our SAW Delay Lines are available with center frequencies from 20 MHz to 100 MHz, with custom requirements to 500 MHz. We offer a variety of both linear and dispersive Delay Lines with time delays between 0.1 microseconds and 10 microseconds. Tapped linear delay lines are also offered.

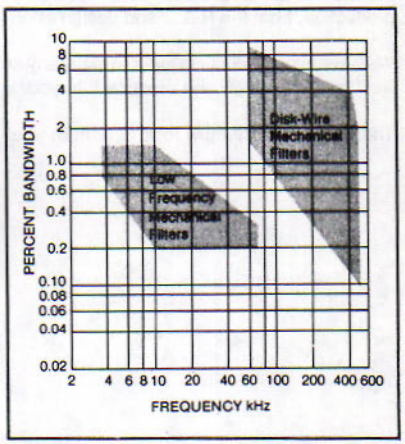
## COLLINS DISC-WIRE MECHANICAL FILTERS



The popular Collins Disc-Wire Mechanical Filters are available with center frequencies from 60 KHz to 500 KHz and fractional bandwidths from 0.1 percent to 9 percent. And they're offered with a wide selection of both Symmetrical Bandpass and Single Sideband types, and are built with either magnetostrictive or piezoelectric transducers.

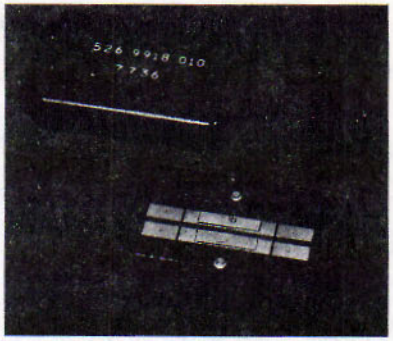
Collins Disc-Wire Mechanical Filters provide excellent discrimination against unwanted signals by steep-skirted selectivity while achieving a flat-topped frequency response. Electrically and mechanically stable, the filters tolerate extreme temperature changes with minor frequency shift, and give continuous service without aging or failing.

The filters are sealed in molded-phenolic cases or hermetically sealed metal cases. Values of stability with temperature vary from 2 to 10 ppm/°C between -40°C and 85°C, depending on the filter.




Design Envelope. Mechanical Filter Percent Bandwidth vs. Frequency Spectrum

## LOW FREQUENCY NARROWBAND MECHANICAL FILTERS

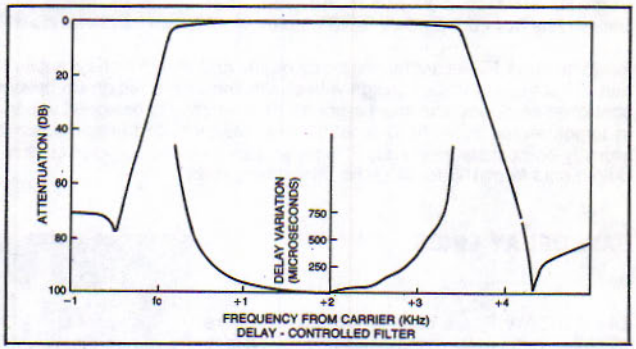


Rockwell-Collins' 3.5 to 70 KHz Mechanical Filter flatpacks are designed for narrow bandwidths in the 0.2 percent to 1.5 percent bandwidth/center frequency range.

These Filters utilize flexure mode, 2 and 3 pole resonators composed of stable iron-nickel alloy bars and piezoelectric ceramic transducers. Small size (1/2 cubic inch) and low cost make the filters ideally suited for Omega Navigation, selective calling systems, telephone multiplex, telemetry, centralized control systems, Sonar, mobile radio and FSK telegraph applications.

## DELAY-CONTROLLED HIGH PERFORMANCE SSB FILTERS

The Disc-Wire Mechanical Filter product line includes high performance Single Sideband Filters with controlled envelope delay characteristics for data communication systems. In many applications, these filters are used without equalization. See illustration for one of the available designs. A majority of those cases with more stringent requirements can be satisfied with a "prescription" equalizer. This combination provides satisfactory performance at a moderate cost.




Delay - Controlled Filter

## WHO WE ARE

We — Rockwell-Collins — are an acknowledged leader in the filter industry. It's a reputation we're proud of, and one that we've earned through an involvement of 25 years in Mechanical Filters and 10 years in Surface Acoustic Wave devices.

We maintain this reputation by commitment to providing our customers — government, military, commercial and the public — the state-of-the-art products at competitive prices and on-target delivery schedules. We're actively involved in all phases of production, from the R & D and design effort, through to manufacturing, quality control and getting our products out to you.

We have filter products to meet virtually any design requirement. And if we can't satisfy your needs with an off-the-shelf device, we'll custom design and produce it to your specifications.

That's who we are, now let's hear from you.

**ROCKWELL INTERNATIONAL**
4311 Jamboree Road
Newport Beach, CA 92660

**ATTN: J.W. CAMPBELL**
**M/S 503-130**

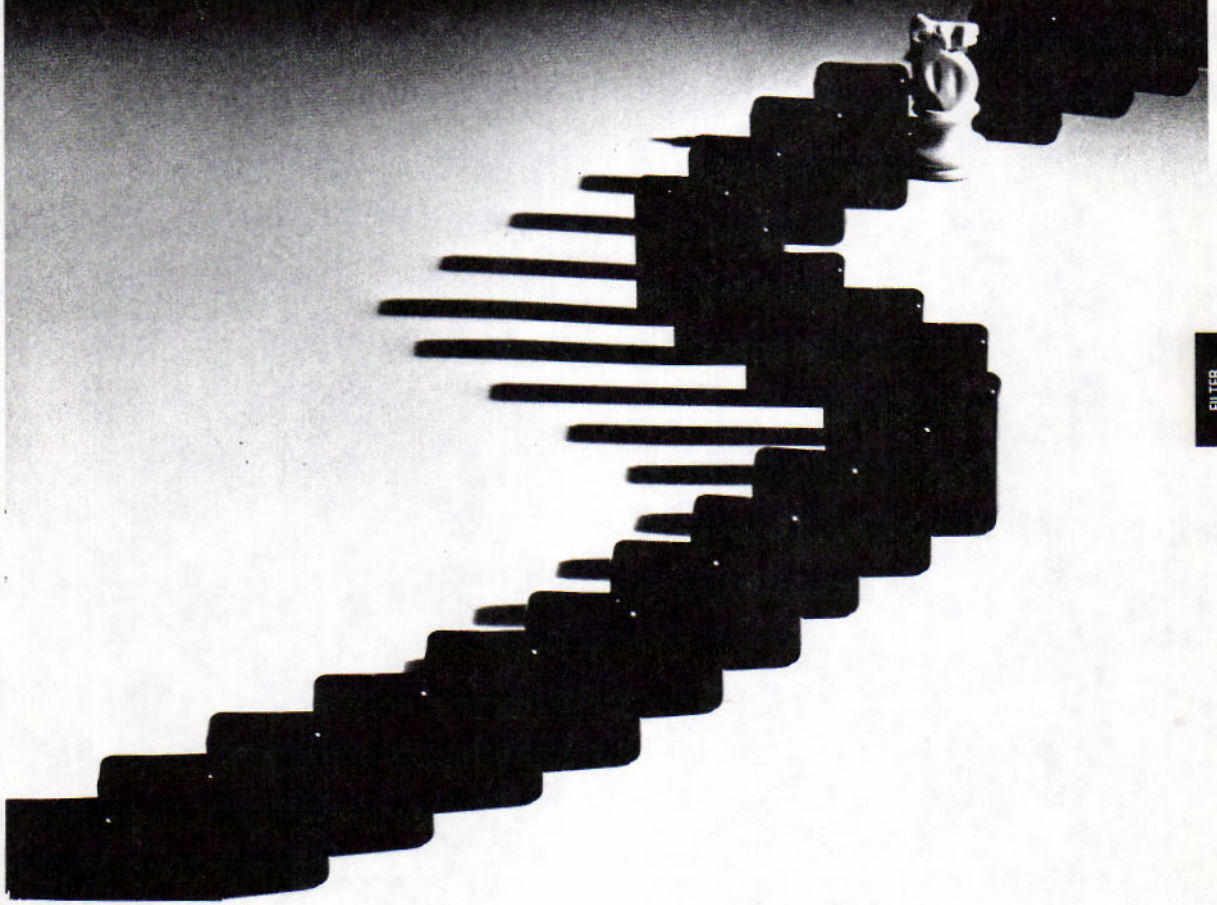
or phone 714/833-4632.

Printed in U.S.A./June 1978/523-1001902-001F2J

FILTER PRODUCTS

# Collins Low Frequency Mechanical Filters

Rockwell



FILTER PRODUCTS

# Collins Low Frequency Mechanical Filters

Rockwell

# Table of Contents


| | | Page |
|---|---|---|
| 1.0 | Introduction to Low Frequency Mechanical Filters | 1 |
| 1.1 | Practical Design Limits | 1 |
| 1.2 | Enclosure Styles | 6 |
| 1.3 | Application Circuits | 6 |
| 1.4 | Applications for Low Frequency Mechanical Filters | 8 |
| 2.0 | Characteristics for Low Frequency Mechanical Filters | 9 |
| 2.1 | Center Frequency Vs. Termination | 9 |
| 2.2 | Center Frequency Vs. Input Voltage Level | 10 |
| 2.3 | Differential Phase Vs. Input Voltage Level | 10 |
| 2.4 | Input to Output Level Linearity | 10 |
| 2.5 | Group Delay Response | 11 |
| 2.6 | Impulse Response | 13 |
| 2.7 | Spurious Responses | 15 |
| 2.8 | Aging | 16 |
| 2.9 | Reliability | 16 |
| 3.0 | Environmental Effects | 16 |
| 3.1 | Temperature Effect on Center Frequency, Loss and Bandwidth | 16 |
| 3.2 | Shock | 17 |
| 3.3 | Vibration | 17 |
| 3.4 | Moisture Resistance | 20 |

# Collins Low Frequency Mechanical Filters

## 1.0 Introduction to Low Frequency Mechanical Filters

The low frequency mechanical filter consists of two metal alloy bars bonded to piezoelectric ceramic transducers and coupled mechanically with wires which also act as the supporting structure. See figure 1. The bars are made out of a constant modulus nickel-iron alloy whose temperature coefficient is adjusted by heat treatment to help compensate for the high positive temperature coefficient of the ceramic. The composite resonators operate in the flexure mode with wires coupling the bars torsionally. Figure 2 shows the equivalent circuit of the filter.

## 1.1 Practical Design Limits

The mechanical filter may be designed as a Chebyshev, Butterworth, TBT, Linear Phase or Bessel filter in either a 2, 3 or 4 pole (resonator) configuration. The Chebyshev (equal passband ripple) designs are available with ripple values ranging from .01 to 1.5 dB. Typical response curves for these designs are available in standard filter handbooks.[1]

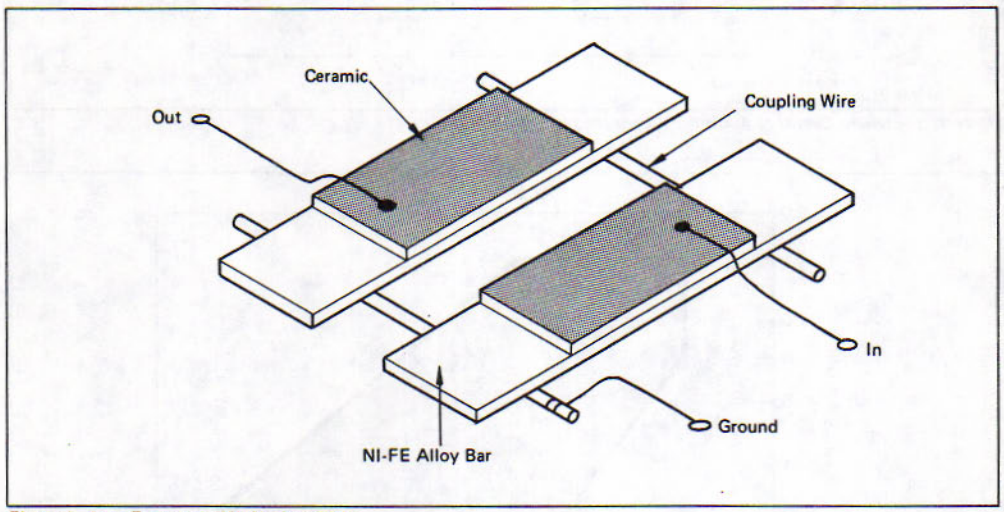



*Figure 1. Low Frequency Mechanical Filter*

[1] G. Hansell, Filter Design and Evaluation, Van Nostrand Reinhold Company, 1969.
Howard W. Sams, Reference Data for Radio Engineers, 1968.
A. Zverev, Handbook of Filter Synthesis, John Wiley and Sons, Inc., 1967.

The practical design limits for low frequency mechanical filters are illustrated in figure 3. The fractional bandwidth ($BW_{3dB}/F_0$) varies from .2% to 1.5% over a center frequency ($F_0$) range of 3.5 to 70 kHz. The fractional bandwidth is further influenced by the environmental restrictions (shock and vibration) and the type of design, such as Chebyshev or Bessel.

Typically, Chebyshev designs having fractional bandwidths between .2% and 1.5% can be achieved for shock levels to 100 G's and vibration levels to 10 G's.

An attenuation comparison for .25 dB ripple Chebyshev filters is presented in figure 4 and a linear phase equiripple (.5° error) design in figure 5.

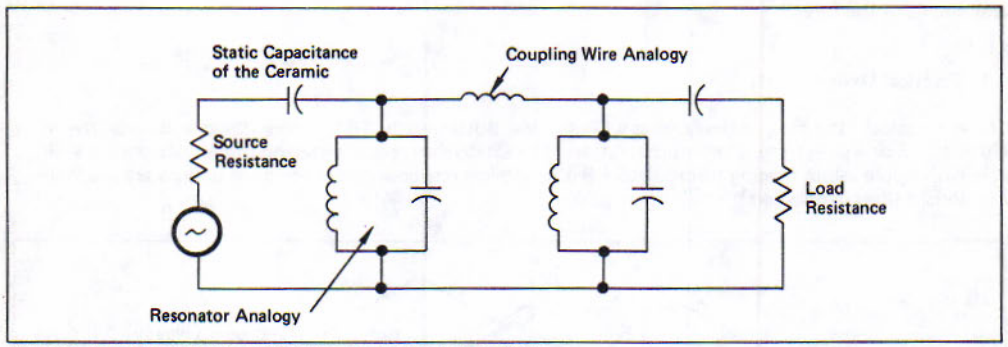



*Figure 2. Equivalent Circuit of A low Frequency Mechanical Filter*

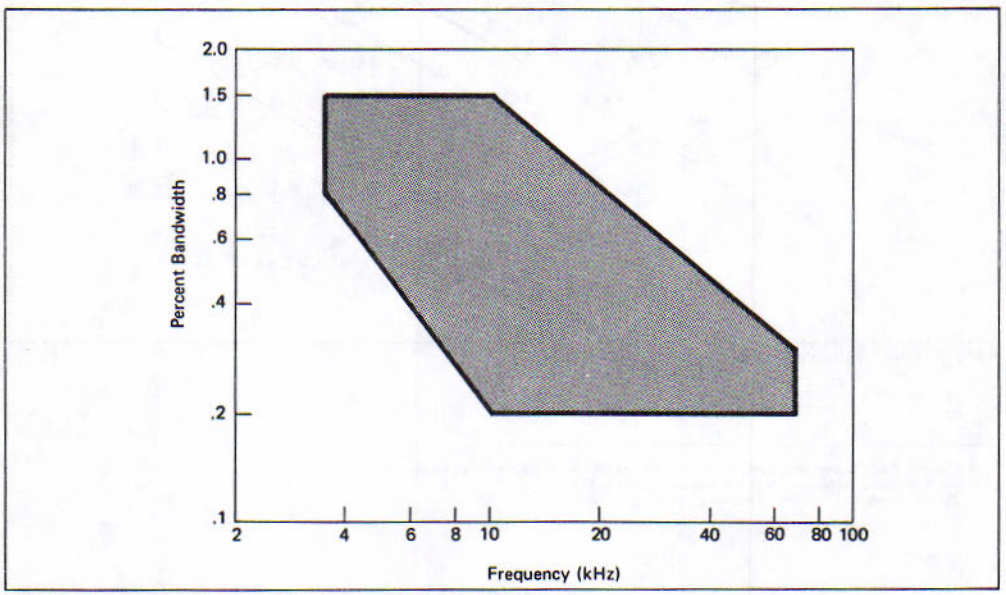



*Figure 3. Practical Design Limits of Low Frequency Mechanical Filters*

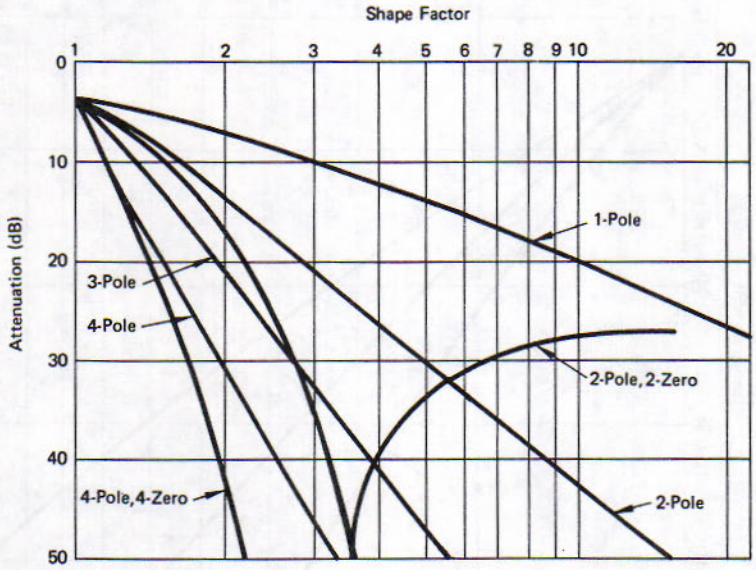



*Figure 4. Attenuation Comparison for .25 dB Ripple Filters*

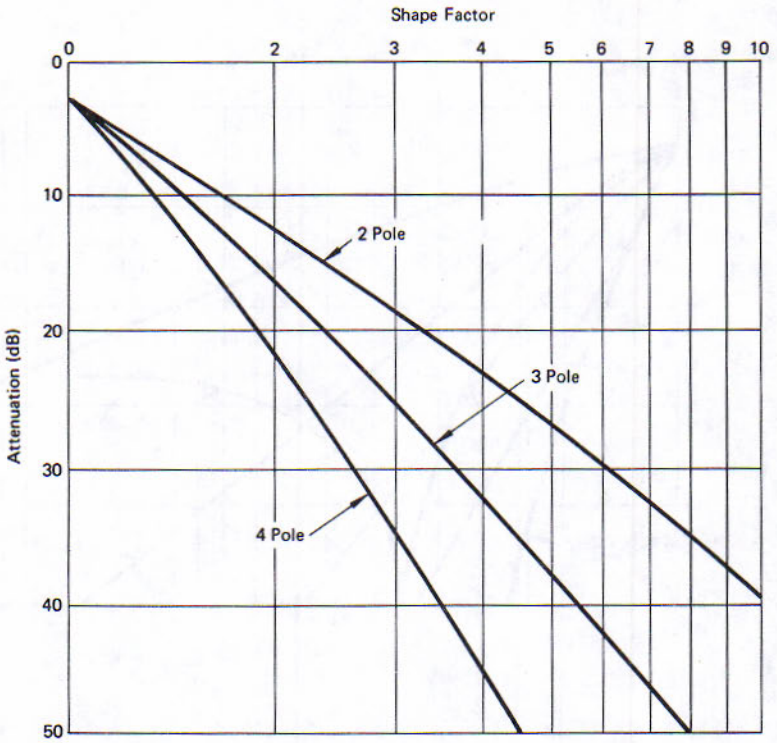



*Figure 5. Attenuation Comparison for Linear Phase Equiripple (.5° Error) Filters*

The Chebyshev designs are primarily for tone selectors while the linear phase designs are used where phase or FSK modulation is transmitted. The linear phase designs have 0 dB ripple and a low ringing impulse response (4% ringing for a 2-Pole). Typical mechanical filter specifications are tabulated in table 1. The values are interrelated (and therefore not independent) and are a function of the type of design, i.e. a very narrow filter would probably not have a high level shock specification.

*Table 1. Mechanical Filter Specifications and Characteristics*

| Specifications | Minimum | Typical | Maximum |
|---|---|---|---|
| Center Frequency ($F_o$) | 3.5 kHz | | 70 kHz |
| Fractional Bandwidth $\frac{BW_{3\ dB}}{F_o}$ | 0.2% | | 1.5% |
| Number of Poles (Resonators) | 1 | | 4 |
| **Characteristics** | **Minimum** | **Typical** | **Maximum** |
| Insertion Loss | 1 dB | 3.5 dB | 10 dB |
| Terminating Resistance | 2 KΩ | 20 KΩ | 50 KΩ |
| Temperature Coefficient of $F_o$ | ± 3 PPM/°C | ± 10 PPM/°C | ± 25 PPM/°C |
| Temperature Coefficient of $BW_{3\ dB}$ | | 500 PPM/°C | |
| Passband Ripple | 0 dB | 0.2 dB | 1.5 dB |
| Vibration (10 Hz to 2000 Hz) | 1G | 10 G's | 15 G's |
| Shock | 15 G's | 100 G's | 1500 G's |
| Differential Phase Vs. Input Level (−70 to −10 dBm) | 0.5° | 0.5° | 2° |
| Volume | 0.5 $IN^3$ | 0.5 $IN^3$ | 1.0 $IN^3$ |

## 1.2 Enclosure Styles

There are four enclosures currently available with low frequency mechanical filters. Three of the enclosures (PA, FS, and LC) are plastic, the fourth (FP) is a hermetically-sealed metal case. It is recommended that the 'LC' case be used whenever possible as it is significantly lower in cost.

Case style 'PA' is a plastic version of the 'FP' enclosure. It is normally not available except under special circumstances.

The 'FS' enclosure is used only on 2-Pole filters which have a 'fail-safe' requirement, i.e. the input can at no time short circuit to the output. This type of filter is normally found in railway systems, people carriers and automated rapid-transit trains. The enclosure is rated for a −20° C to +95° C environment and is not hermetically-sealed.

The 'LC' case is made of plastic and is ultrasonically sealed. It is rated for a −55° C to +95° C environment. Filters in these enclosures have been tested with two consecutive cycles of Mil-Std 202, method 106 for a total time of 20 days at 90% humidity. During the 20 day period filters are thermally-cycled from −10° C to +65° C and intermittently vibrated at 9 G's. This test is designed to evaluate the resistance of component parts to tropical environments. Although the cases and the filters withstood this environment, they may not be able to withstand extremely long period environments because of the permeability of the plastic case. However, if the user provides an additional moisture barrier such as 'post-coat', filters in this enclosure will pass a more rigorous environment.

The alternative enclosure for tropical or high altitude service is the 'FP' case style. This is a cold-welded metal enclosure with glass to metal terminal seals. The filters in this package are rated for a −55° C to +95° C environment and guaranteed to meet the moisture resistance test. A disadvantage is that they are several times more expensive than the 'LC' enclosure.

## 1.3 Application Circuits

The following constraints are suggested limitations on the application circuit. Although these values may be exceeded without damage to the part, the filter will operate in a non-linear portion of its spectrum or will not meet the specifications.

| | |
|---|---|
| Signal input level (across the terminals): | 1 Vrms |
| DC voltage across the terminals: | 50 VDC |
| Source and load termination: | ± 5% |
| Stray capacitance across the input/output terminals to ground: | 50 pf Max |



The application circuits of figure 7 demonstrate the use of bridging capacitors ($C_1$, $C_2$) which are used to convert a monotonic response to an elliptic function response. Bridging the filter with a capacitor between the input and output terminals provides the attenuation poles (transmission zeros) shown in figure 4. This capacitor is typically about 30 pf in value. Although there is a substantial improvement in the filter's shape factor (the ratio of the bandwidth, at a specified attenuation level to the 3 dB bandwidth) the disadvantage with this technique is that the attenuation level in the stopband of the filter decreases as the bridging capacitance is increased. See figure 4 for an illustration of a 2 Pole — 2 Zero design.

A method used for realizing greater performance from a mechanical filter and still maintain a high stopband attenuation level is to cascade two or more units. This method results in an addition of the attenuation levels of each filter at any specific frequency.

The cascading is accomplished by using an active network to prevent interaction between the filters. The network could be either a transistor buffer amplifier or an Op-Amp. See figure 7.

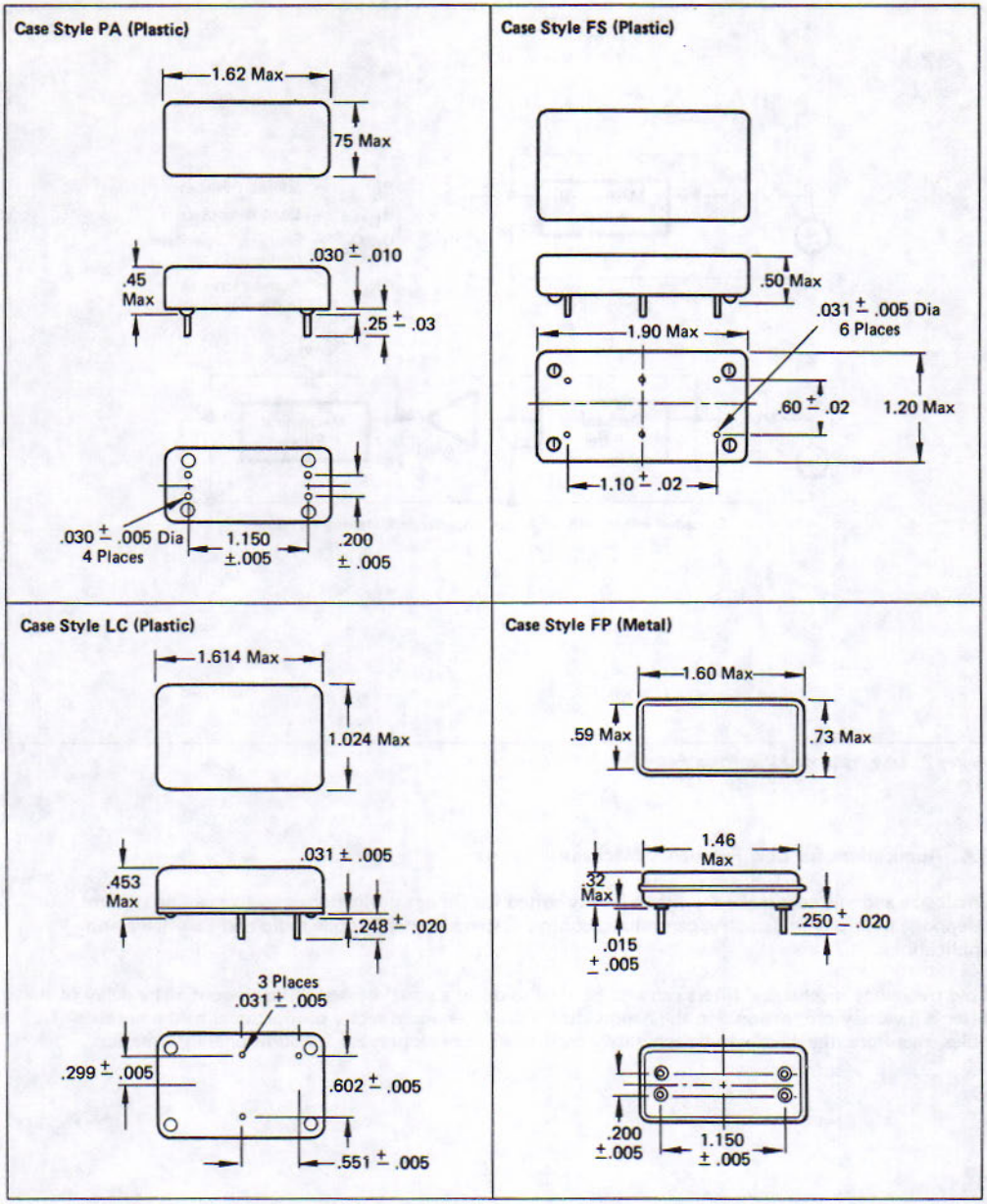



*Figure 6. Low Frequency Narrowband Mechanical Filter Flatpack Dimensions*

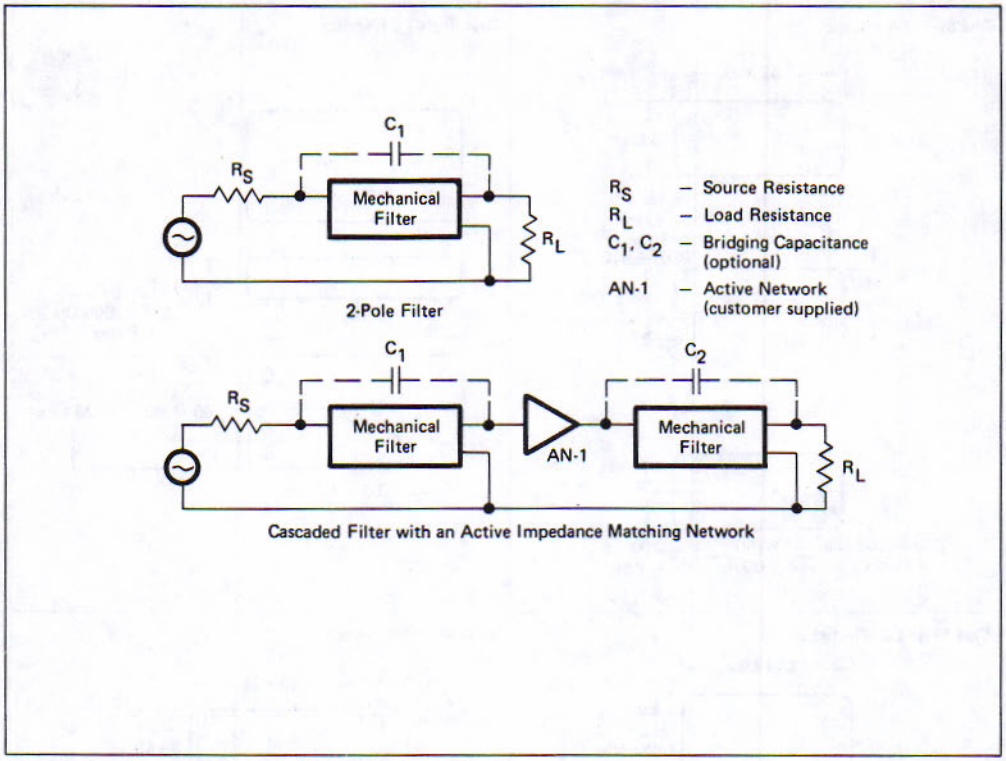



*Figure 7. Low Frequency Mechanical Filter Circuit Configurations*



### 1.4 Applications for Low Frequency Mechanical Filters

Small size and low cost make the filters ideally suited for Omega navigation, selective calling systems, telephone multiplex, telemetry, centralized control systems, Sonar, mobile radio and FSK telegraph applications.

Low frequency mechanical filters can also be used to delay a signal by a specific amount. The delay of the filter is inversely proportional to the bandwidth of the filter and directly proportional to the number of poles, therefore, the delay can be accurately controlled. See section 2.5 for additional information.

## 2.0 Characteristics of Low Frequency Mechanical Filters

### 2.1 Center Frequency Vs. Termination

In normal applications of low frequency mechanical filters, the resistive terminations ($R_S$ and $R_L$) shown in figure 7, should not deviate more than $\pm$ 5% from the specified values. That is, the terminations affect the actual center frequency to some extent. For example, if a filter with a nominal center frequency of 10 kHz and a 50 Hz bandwidth has both its source and load resistances increased by 5% above the specified values, the filter center frequency $\left(\frac{F3H + F3L}{2}\right)$ will increase by .5 Hz. If $R_S$ and $R_L$ are changed (from the specified value) in opposite directions, small changes (2% to 3%) are off-setting, and there is no center frequency shift. For large variations (in opposite directions) in $R_S$ and $R_L$, the effects are not completely offset, and the insertion loss and passband ripple of the filter will increase.

Stray capacitance between the input/output terminals and ground should not exceed 50 pf. Additional capacitance beyond this value will cause changes in insertion loss and center frequency. An increase to 150 pf will result in a .5 dB change in loss and a 75 ppm change in center frequency in the above example.

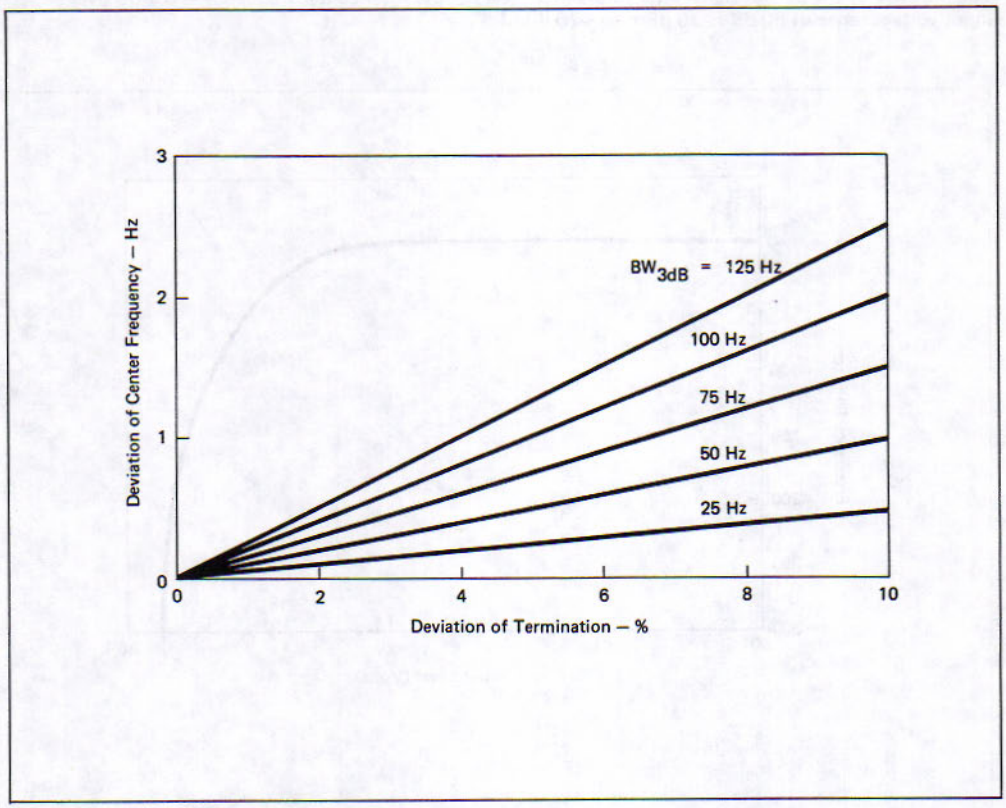



*Figure 8. Variation of Filter Center Frequency with Resistive Termination*

## 2.2 Center Frequency Vs. Input Voltage Level

Low frequency mechanical filters remain very linear with drive level up to 0.5 v, at which point they rapidly become non-linear. See figure 9. The shift in the center frequency at a ten volt level is enough to move some filters out of specification. Also, along with the non-linear effects, excessive drive level causes time dependent changes in the ceramic material. These changes cause the center frequency of the filter to be lower after being driven at a high voltage level. Once the drive level is reduced the filter response begins to return to its original frequency.

## 2.3 Differential Phase Vs. Input Voltage Level

The differential phase at the center frequency of a linear-phase equiripple (.5° error) filter is 0.5 degree over an input level variation of 60 dB, namely −10 dBm to −70 dBm. The change in phase is due to a center frequency shift caused by the nonlinearity of the input transducer.

## 2.4 Input to Output Level Linearity

The linearity of the output signal level to the input level at the filter center frequency is 0.1 dB over an input voltage range of 60 dB (−10 dBm to −70 dBm).

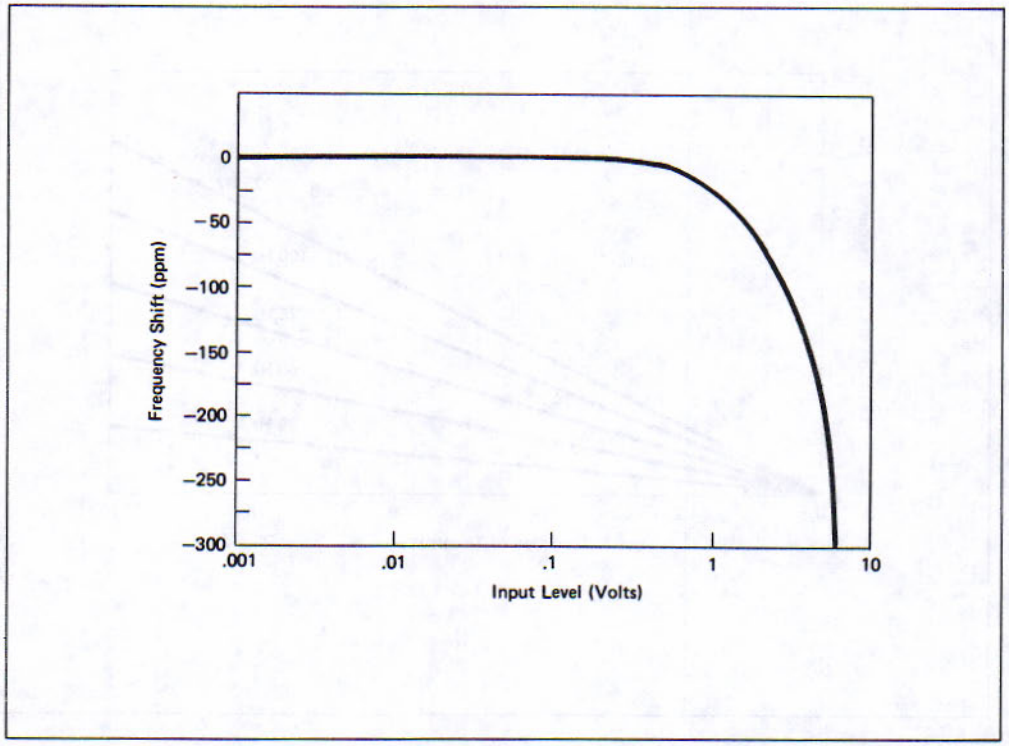



*Figure 9. Variation in Center Frequency with Input Voltage Level*

## 2.5 Group Delay Response

The approximate group (envelope) delay for a mechanical filter can be determined from figures 10, 11, 12 and 13 as well as the following equation.

$$\text{Group delay (sec) at center frequency} = \frac{NGD}{\pi \, BW_{3\,dB}}$$

NGD = Normalized Group Delay from figures 10, 11, 12, or 13

$BW_{3\,dB}$ = 3 dB Bandwidth (in Hz)

Example:

The group delay for a 2 Pole .1 dB Chebyshev filter which has a 40 Hz bandwidth is

N = 2

$BW_{3\,dB}$ = 40 Hz

NGD from figure 12 = 1.4 sec

$$\text{Group delay} = \frac{1.4}{\pi \, 40} = .011 \text{ sec} = 11 \text{ msec}$$

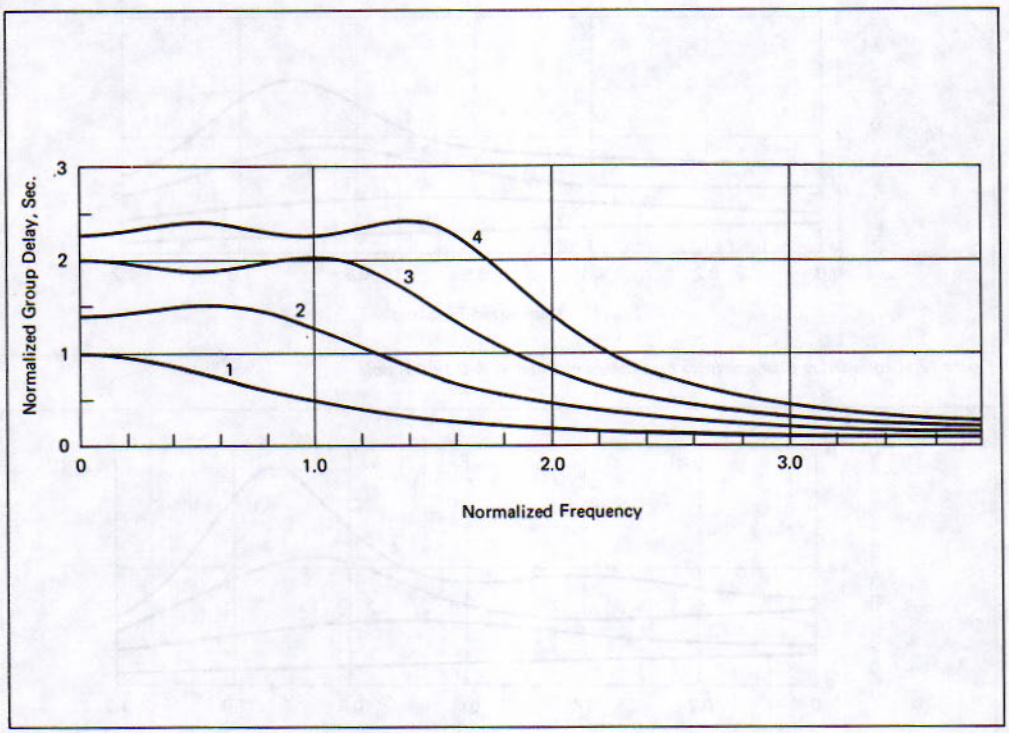



*Figure 10. Group-Delay Characteristics for Linear Phase (Phase Error = .5°) Filter*

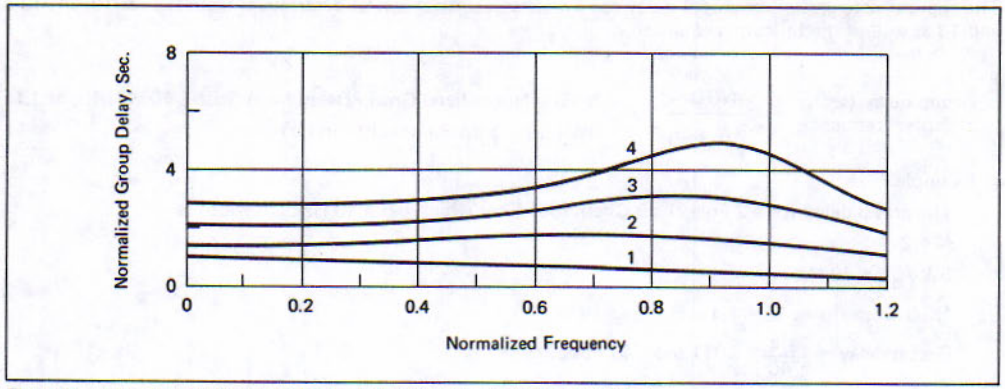



*Figure 11. Group-Delay Characteristics for Chebyshev Filter with 0.01 dB Ripple*

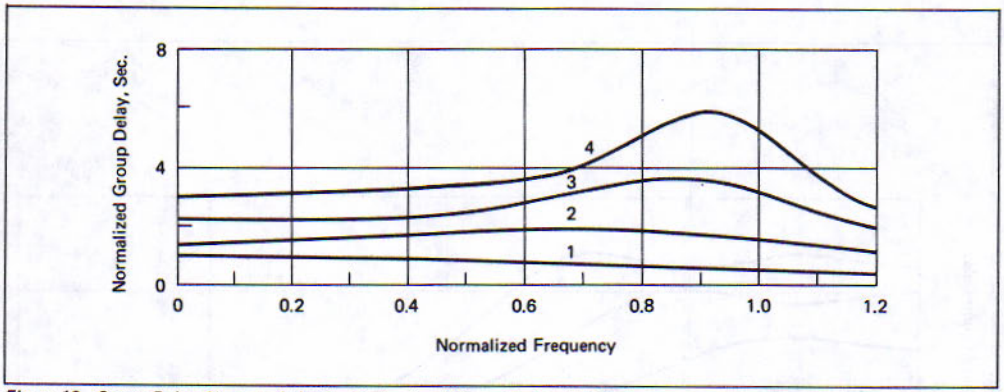



*Figure 12. Group-Delay Characteristics for Chebyshev Filter with 0.1 dB Ripple*



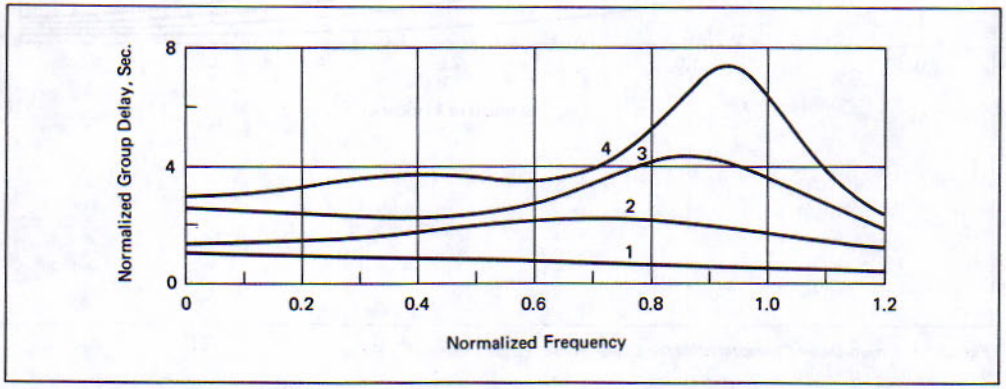
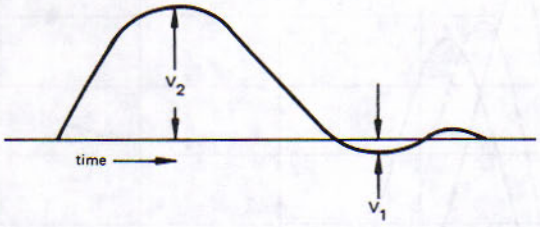



*Figure 13. Group-Delay Characteristics for Chebyshev Filter with 0.5 dB Ripple*

## 2.6 Impulse Response

Figures 14 thru 17 can be used to approximate the impulse response ringing value of a mechanical filter. A definition of ringing is the ratio of $V_1/V_2$ in percent.




For example:

A two-pole mechanical filter designed as a linear-phase filter has an impulse response ringing value of 4%.

N = 2

$V_1$ = .02 from figure 14

$V_2$ = .48 from figure 14

$$\text{Impulse response ringing} = \frac{V_1}{V_2} \times 100 = \frac{.02}{.48} \times 100 = 4.1\%$$

A three-pole .5 dB Chebyshev design has an impulse response of 21%.

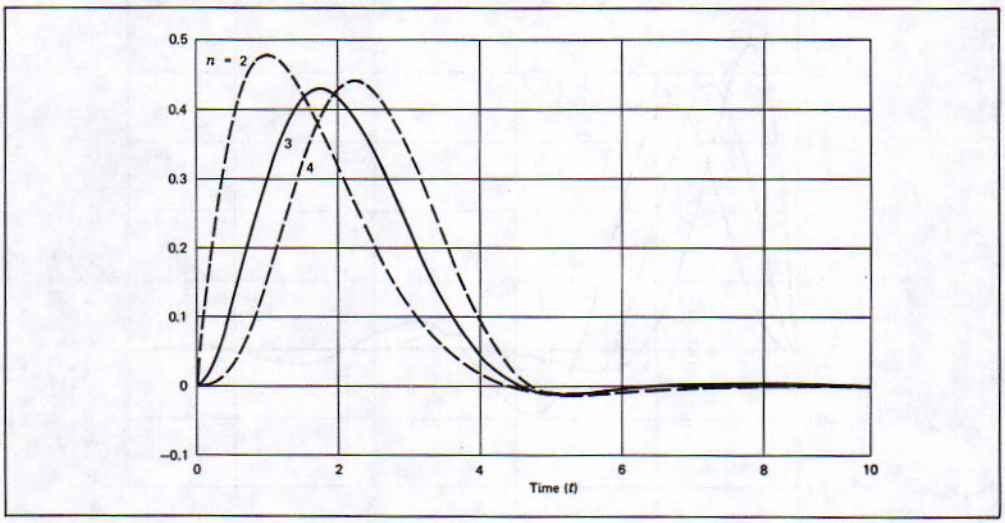



*Figure 14. Impulse Response for Linear Phase (Phase Error = .5°) Filters*

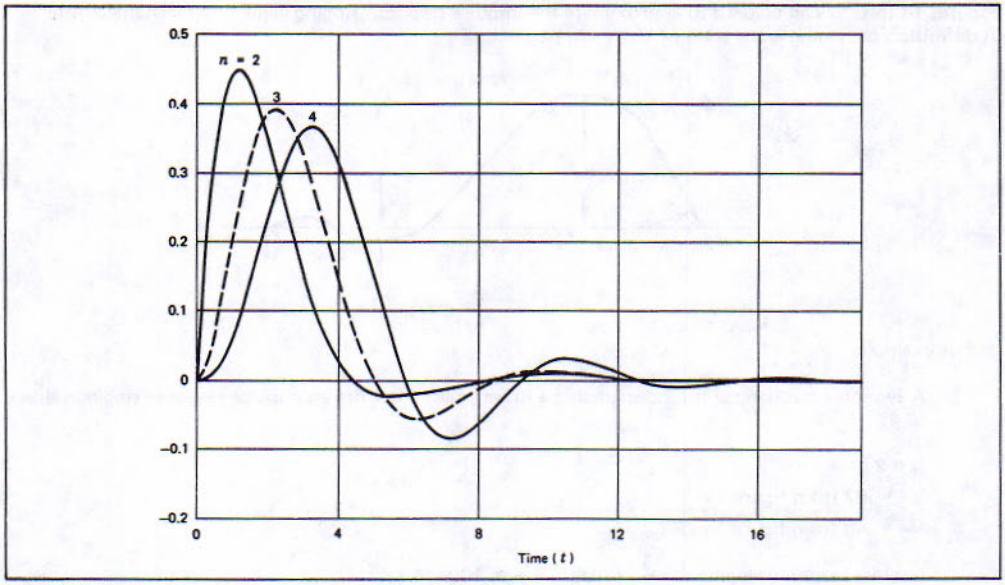



*Figure 15. Impulse Response for Chebyshev Filters with 0.01 dB Ripple*

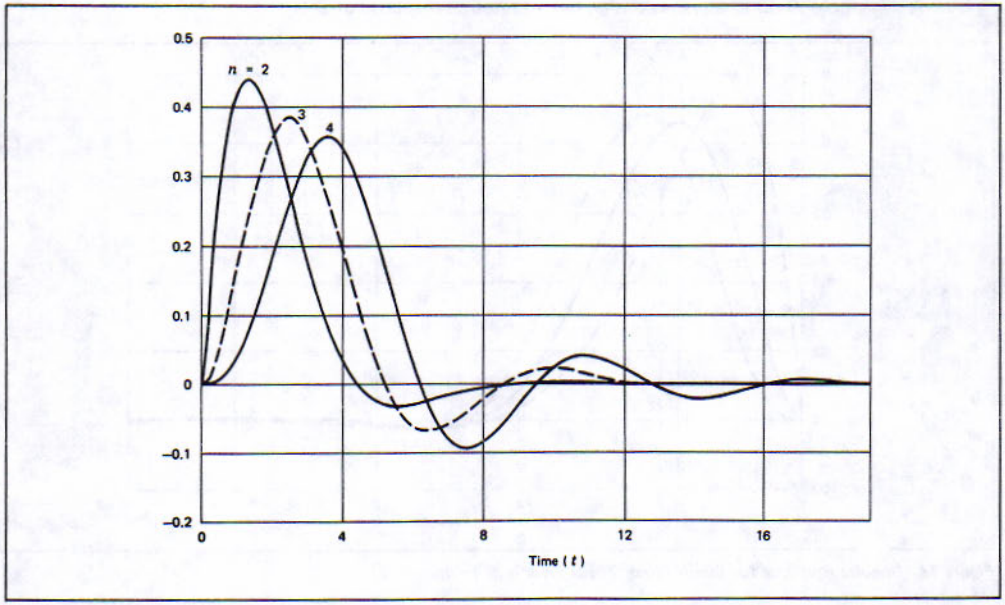



*Figure 16. Impulse Response for Chebyshev Filters with 0.1 dB Ripple*

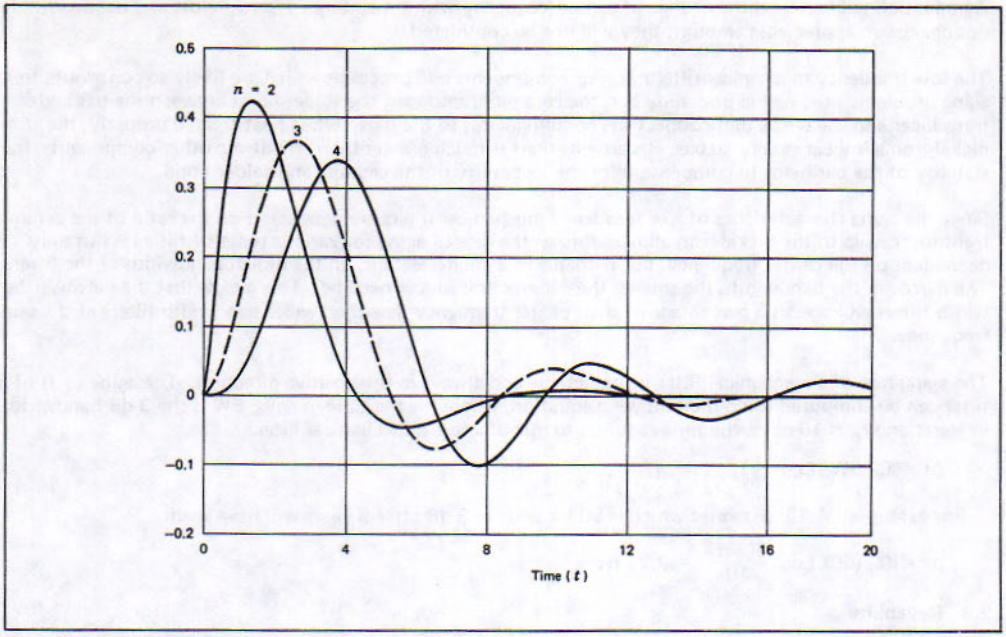



*Figure 17. Impulse Response for Chebyshev Filters with 0.5 dB Ripple*

## 2.7 Spurious Responses

Mechanical filters have resonant frequency overtones very similar to those found in quartz crystals. These overtones occur at multiples of the fundamental; the multiples are 2.4, 4.8, 7.6, 10.6, etc.

As an example, a mechanical filter designed for Omega navigation system applications at 10.2 kHz will have spurious responses (frequency overtones) at 24.5, 49, 77.5 and 108 kHz.

These overtones are inherent to the flexure mode of vibration used in the design of low-frequency mechanical filters. They cannot be suppressed without compromising the filter design. The odd-numbered modes, 2.4 and 7.6, are normally 50 dB below the fundamental. Suppression of these occurs because of the transducer coupling method utilized to drive the fundamental mode. The even-numbered overtones, 4.8, 10.6, have levels approximately 15 dB below the fundamental. These modes cannot be suppressed internally, however, a low-pass filter can be used to reject these higher frequency modes. Another alternative is the use of a bandpass "roofing" filter. See figure 22. The 'roofing' filter will reject both the low frequency microphonic and the high frequency spurious responses. It should be placed after the mechanical filter i.e., the incoming signal should go through the mechanical filter first, then through the 'roofing' filter. In this way, the microphonic responses are rejected as well as the spurious responses. The 'roofing' filter should be compatible with the mechanical filter; it should not affect its passband response.

## 2.8 Aging

Aging is defined herein as the change of center frequency with time. Since insertion loss and bandwidth do not change an appreciable amount, they will not be considered.

The low frequency mechanical filter has four components and processes which are likely to contribute to aging problems: the nickel-iron alloy bar, the ceramic transducer, the solder bond between the bar and transducer and the welds that connect the coupling wires to the bars. When heat treated properly, the nickel-iron alloy bar is very stable. Because its mass is much greater than any of the other components, the stability of the bar helps to compensate for the instability of the ceramic and solder bond.

Since the aging characteristics of low frequency mechanical filters are dependent on the ratio of the ceramic transducer mass to the nickel-iron alloy bar mass, the rate of aging for various types of filters is not only dependent on the center frequency, but perhaps, to a greater extent, on the design bandwidth of the filter. The narrower the bandwidth, the smaller the ceramic transducer need be. This means that the narrower bandwidth filters will age, as a percentage of their center frequency, less than wider bandwidth filters at the same frequency.

The aging rate of a mechanical filter is predictable and always in the positive direction. The aging ($\Delta$ f) of a filter can be computed using the following equation, where $t$ is the time in days, BW is the 3 dB bandwidth in Hertz and $t_o$ is 10 days, the time required to manufacture a mechanical filter.

$$\Delta f = .02 \text{ BW } (\text{Log } \frac{t}{to})$$

For example: A 12 kHz filter which is 50 Hz wide at 3 dB after 5 years will have aged:

$$\Delta f = .02\ (50)\ \text{Log } \frac{5(365)}{10} = 2.26 \text{ Hz}$$

## 2.9 Reliability

The MTBF (mean time between failures) is $3 \times 10^7$ hours. This is based on field data which was accumulated over a period of several years.

## 3.0 Environmental Effects

### 3.1 Temperature Effect on Center Frequency, Loss and Bandwidth

Design techniques for low frequency mechanical filters utilize compensating factors which minimize the shift of the filter center frequency with a change in temperature.

The center frequency shift vs. temperature is normally compensated to a tolerance of $\pm$ 10 ppm/°C over a temperature range of –20°C to +65°C. The tolerance can be as high as $\pm$ 25 ppm/°C for the largest fractional bandwidth filters. The filters may be used over larger temperature ranges, such as –55°C to +95°C without any physical damage or permanent effect on the frequency response characteristics.

The variation of insertion loss with temperature is typically $\pm$ 1 dB (with a maximum variation of $\pm$ 1.5 dB) over a temperature range of –20°C to +65°C. The narrower the filter bandwidth the smaller the insertion loss variation.

Bandwidth normally changes very little with temperature in absolute terms. A typical variation for a filter with a 100 Hz bandwidth would be 1.5 Hz over a temperature range of +25°C to +65°C. This is a bandwidth shift of +375 ppm/°C.

The variations in center frequency, loss and bandwidth due to temperature change are temporary in nature; the filter will return to its original condition when the temperature is restored to +25°C.

### 3.2 Shock

A resilient rubber shock mount is used to isolate the mechanical filter structure from shock forces which could cause damage. This mount allows the average filter to withstand 100 G, 6msec, shocks without a change in the filter response. Certain mechanical filters can withstand 1500 G's of shock before permanent damage occurs.

### 3.3 Vibration

The internal shock mount, that so effectively isolates the filter from shock, also does an excellent job against vibration forces. The average filter will safely withstand a constant 10 G vibration level between 10 to 2000 Hz. At approximately 15 G's the elastic limit is reached causing the filter to become permanently damaged.

Often it is not only important that a filter survive a specific vibration level, but it is also important that it retains the proper response characteristics during the vibration. While the attenuation response shows little change, there is some variation of phase and some microphonic effects during vibration. These are important characteristics in applications like Omega navigation systems.

The variation of phase of an Omega filter as a function of vibration frequency is shown in figure 18. It will be noticed that there is a peak deviation point around 400 Hz. The reason for the peak is that the entire filter structure has a resonance at this point. This structural resonance also has an effect on the microphonic noise level.

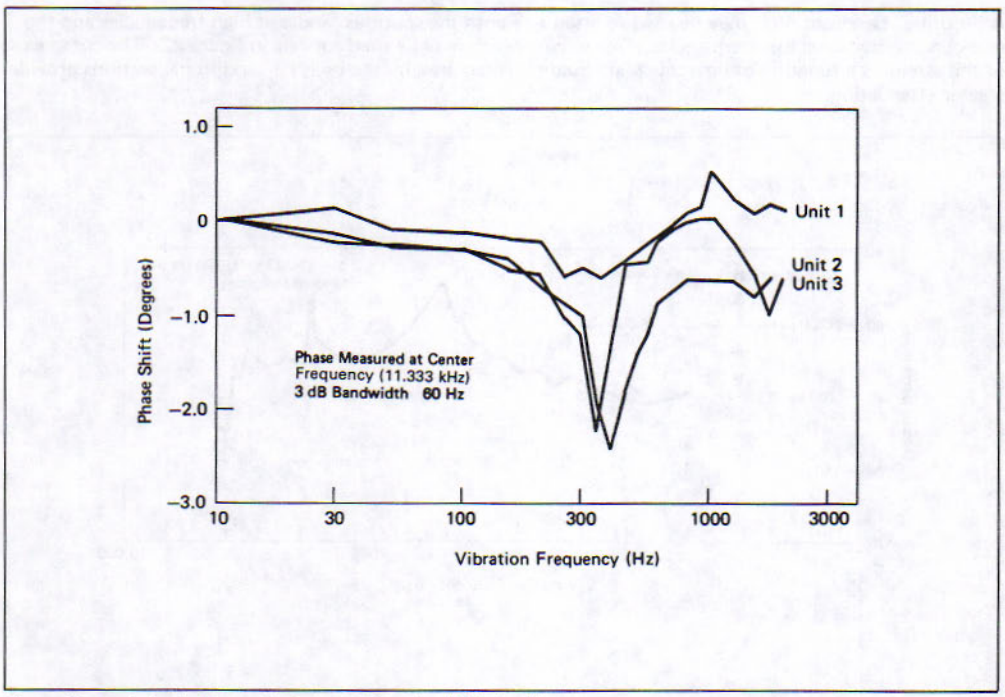



*Figure 18. Variation in Phase with External Vibration (10 G Level)*

Figure 19 illustrates the levels of microphonic responses of a 100 Hz bandwidth Omega filter. These levels were measured while the filter was vibrated at a constant 5 G level over the frequency range of 50 to 4000 Hz. The maximum output occurred at 525 Hz at a level of −50 dBv.

In applications where these levels are intolerable, special structural designs can be incorporated into the equipment in order to dampen the vibrations around 500 Hz. Methods such as mounting the filter near a brace or an equipment corner, using a low-Q rubber or elastomer as an external filter mount and other vibration suppression techniques will help in limiting the phase shift and amplitude response microphonics.

A successful technique for attenuation of the low frequency microphonic responses is the use of a highpass filter network. These filters are placed in the signal path between the mechanical filter and the detector. Figures 20, 21 and 22 illustrate 3 types of filters which may be used to reduce microphonic responses. They differ in the type and number of components required. The improvement in microphonic amplitude response as a result of using these filters is presented in figures 23 through 26.

The filter circuit of figure 20 will attenuate the microphonic level by approximately 15 dB. It is a single section consisting of 1 reactive component, however, it will not attenuate any spurious frequencies above the filter passband.

The high-pass circuit of figure 21 consists of 3 reactive components and will attenuate only frequencies below 9 kHz. This LC circuit provides 60 dB of rejection at microphonic frequencies.

A "roofing" bandpass filter may be used to attenuate both the spurious modes at high frequencies and the microphonic signals at low frequencies. One circuit which may be used appears in figure 22. The complexity of this circuit is a function of how much attenuation is required by the user, i.e., additional sections provide greater attenuation.

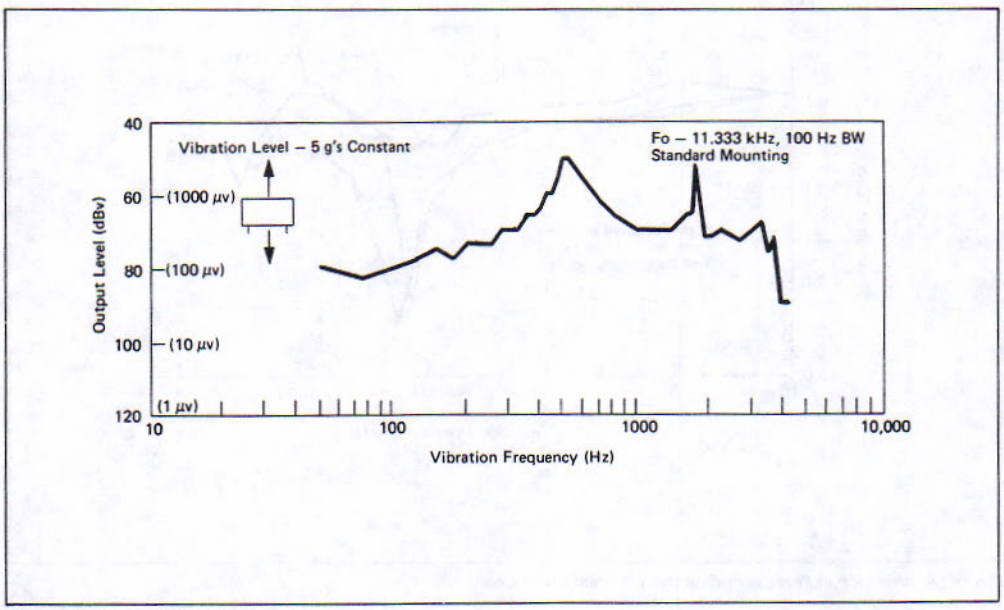



*Figure 19. Omega Filter Microphonic Response*

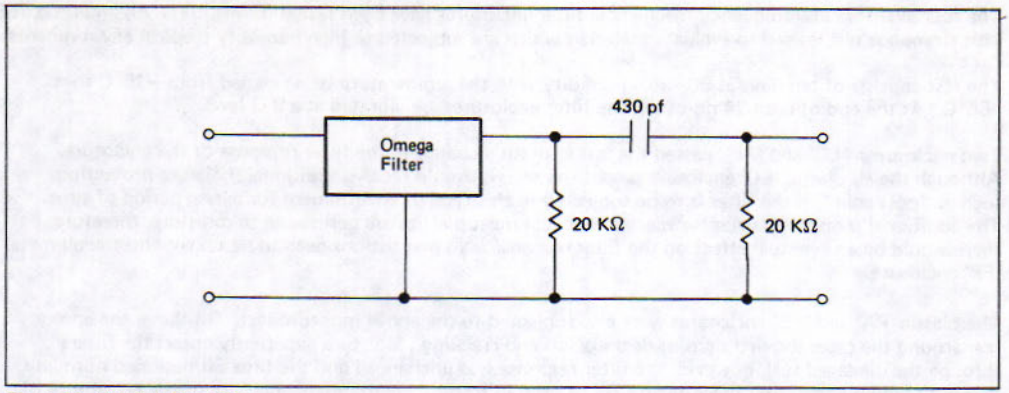



*Figure 20. RC High-Pass Filter*

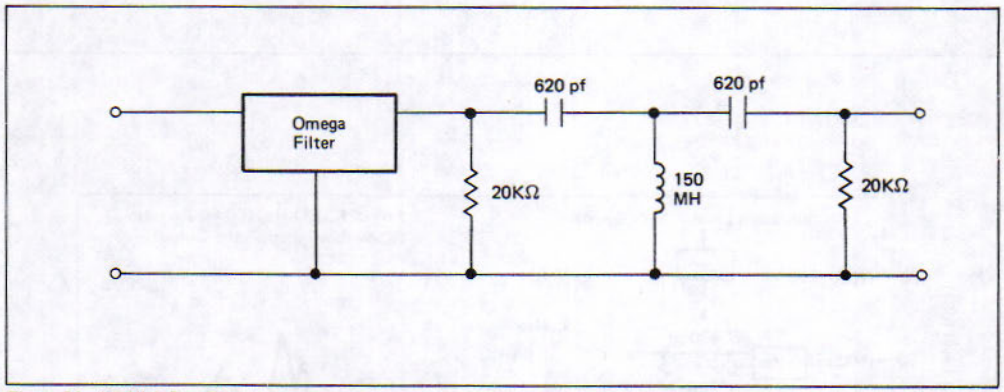



*Figure 21. LC High-Pass Filter*

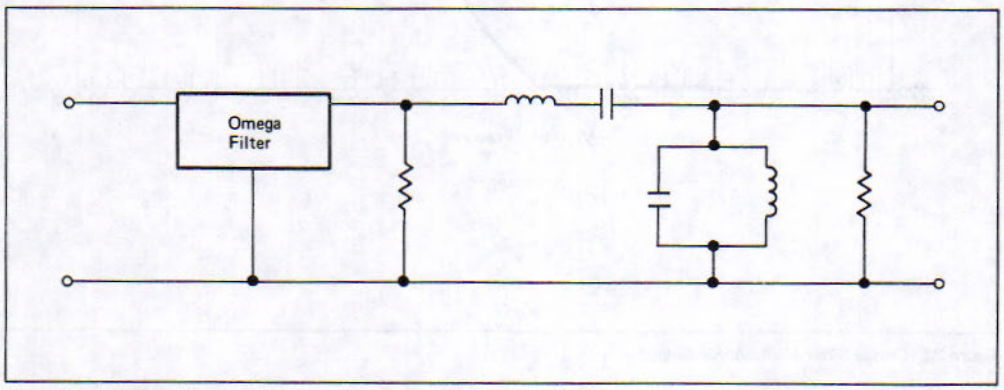



*Figure 22. Bandpass Filter*

### 3.4 Moisture Resistance

The four available low-frequency mechanical filter enclosures have been tested to MIL-STD-202, method 106. This strenuous test is used to evaluate materials which are subjected to high humidity tropical environments.

The test consists of ten days at 90–95% humidity with the temperature being cycled from −10°C to +65°C. At the end of each 24 hr. cycle, the filter enclosures are vibrated at a 9 G level.

Two enclosures, 'LC' and 'FP', passed the test without a change in the filter response or the enclosure. Although the all-plastic 'LC' enclosure passed the test, it should receive additional moisture protection, such as "post coat", if the filter is to be subjected to this type of environment for a long period of time. The additional moisture barrier is necessary because most plastics are permeable to moisture, therefore, there would be an eventual effect on the filter response. No precautions need to be taken with the all-metal 'FP' enclosure.

The plastic 'PA' and 'FS' enclosures were also subjected to the above moisture test. On these, the epoxy seal around the cases showed signs of degradation and cracking. Moisture apparently enters the filters through the damaged seal, however, the filter response was unchanged and the filters functioned normally. It is not recommended that these enclosures be used in tropical environments because of the possibility of seal failure.

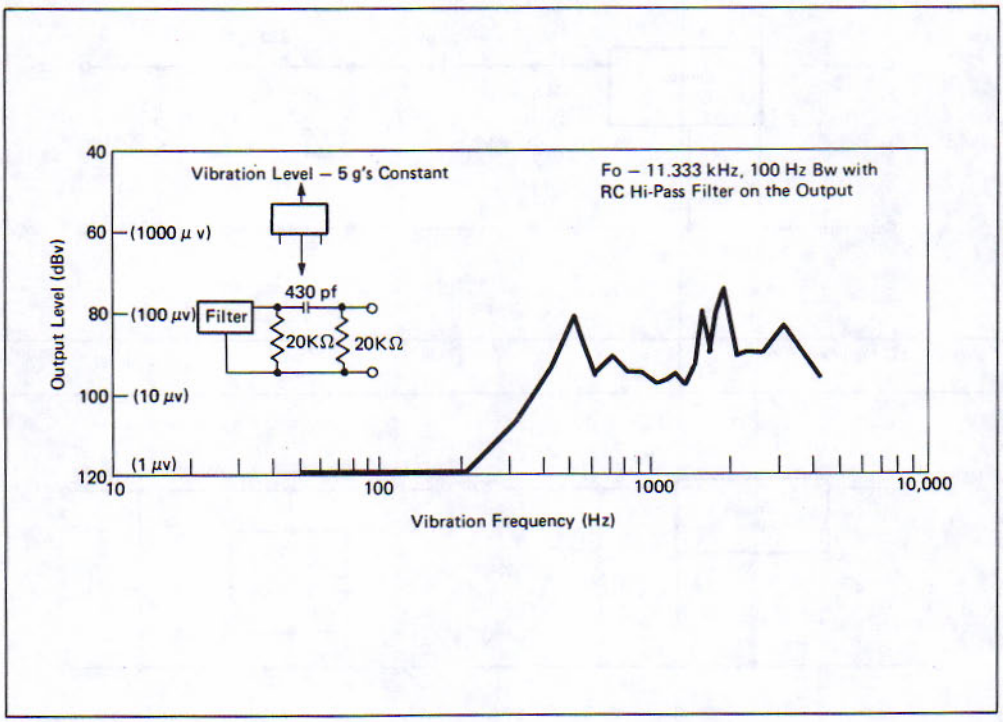



*Figure 23. Omega Filter Microphonic Response*

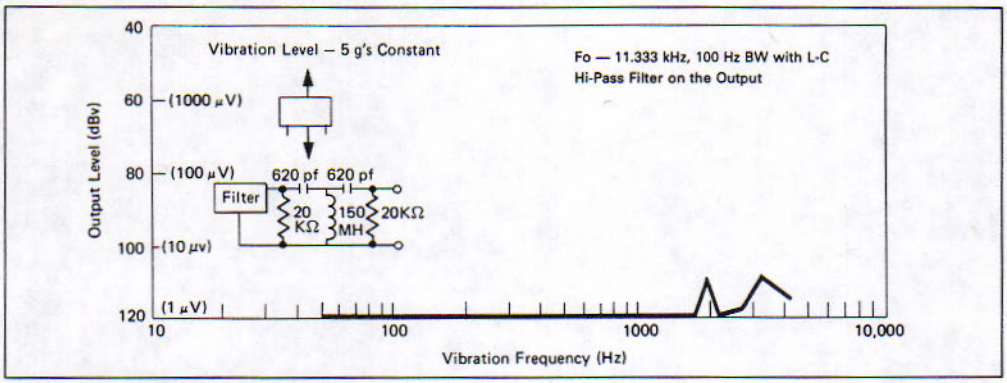



*Figure 24. Omega Filter Microphonic Response*

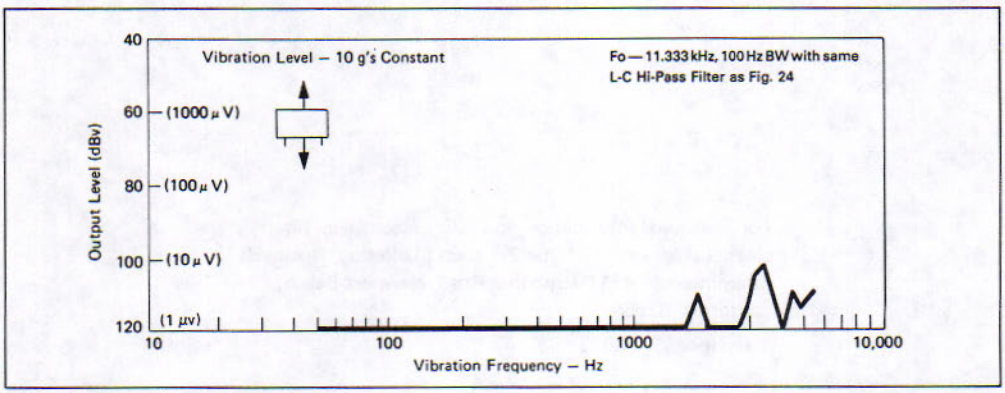



*Figure 25. Omega Filter Microphonic Response*

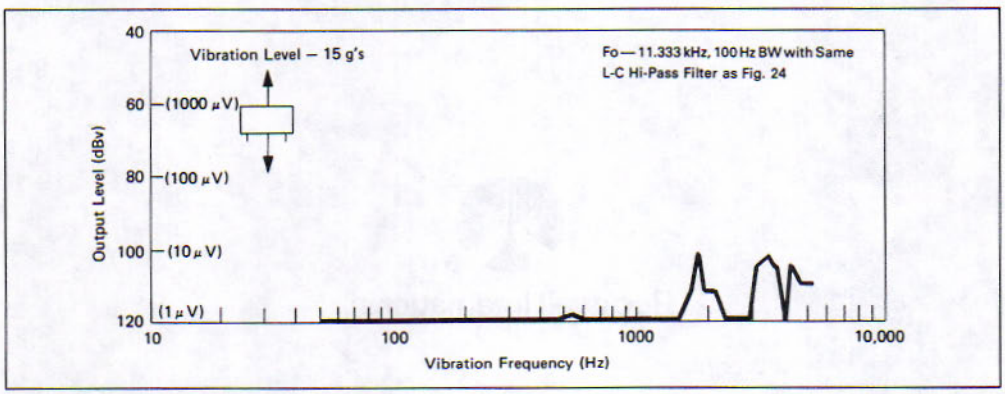



*Figure 26. Omega Filter Microphonic Response*

For additional information on Collins mechanical filters, please call or write: **Filter Products Marketing, Rockwell International - 4311 Jamboree Road, Newport Beach, California 92660.**

Telephone: 714 833-4632

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**Rockwell International**

Printed in USA/April 1978/523-1001793-101F20

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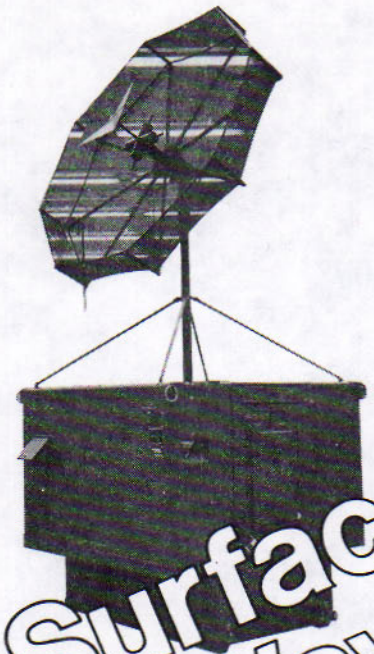
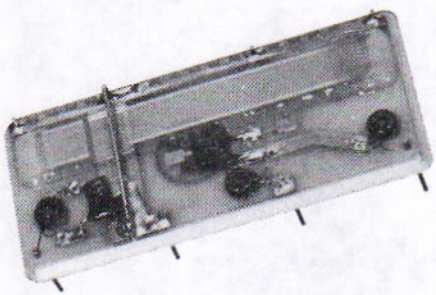


# Surface Acoustic Wave Devices



FILTER PRODUCTS

## Filter Products

# Surface Acoustic Wave Devices

## 1.0 INTRODUCTION

Rockwell International has pioneered in the design and development of Surface Acoustic Wave (SAW) devices through its Electronic Research Center and the Rockwell Science Center. The R&D program has been conducted over the past 10 years. The wide range of experience and knowledge acquired during this period enabled Rockwell to emerge in a leadership position in the field of Surface Acoustic Wave devices. Filter Products, a major producer of mechanical filters for the past 25 years, now is offering production devices and can respond to your development needs. Our filter production and product line experience is being applied to the newest mechanical filter, the SAWD.

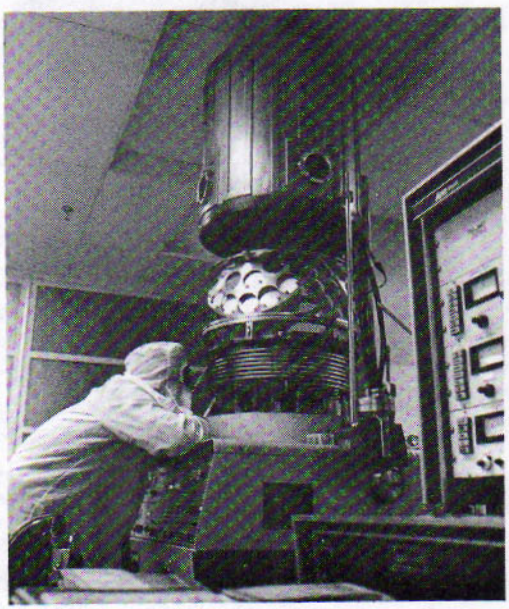
Located in Newport Beach, California, Rockwell Filter Products has complete facilities for all tooling, processing, assembly and test for SAW devices on a production basis. Our production setup allows us to engage in applications for customer prototype designs, from concept through production, or to build existing designs. We are in a position to accommodate your SAW needs and assist you in determining your requirements.

This publication is designed to acquaint you with currently available SAW technology from Rockwell International, Filter Products. It describes the basic device and provides the necessary information to specify production applications when ordering Rockwell SAW devices. For basic technical information, a good general reference is H. Mathews, *Surface Wave Filters*, John Wiley & Sons, 1977.

### 1.1 Masks

Rockwell has extensive design experience in filter and delay line applications. Based on this expertise, mask tooling is created internally for use by our wafer fabrication production department. Fabrication and assembly area personnel have twelve years of experience in fabricating both high-grade custom and consumer MOS/LSI devices. The test area uses the best, up-to-date production equipment available on the market today. Within this facility a MIL environmental test area for full qualification testing is included and operates in accordance with MIL-Q-9858. A department is completely dedicated to the assembly and test of SAW devices.

Mask



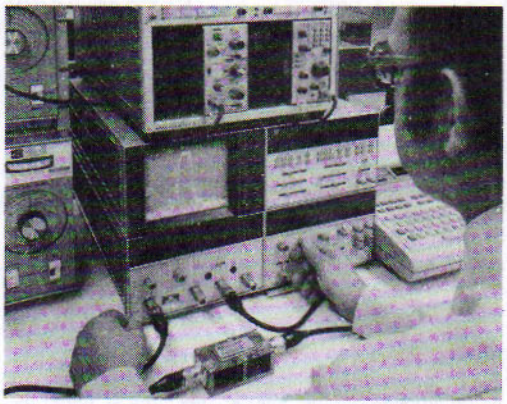
Fabrication

### 1.2 Resources

In addition to the extensive internal operations support in filter technology and LSI processing, Rockwell's Electronic Research Center in Anaheim, California and its Science Center in Thousand Oaks, California, provide technological support. Both centers are presently engaged in research and development of SAW devices.

The benefits derived from new technology and processing techniques, such as Very Large Scale Integration, E-Beam and X-ray Lithography, are available today at Rockwell for application in present and future SAW devices.

Assembly



Test

## 2.0 GENERAL DESCRIPTION OF SAW DEVICES

A Surface Acoustic Wave Device (SAWD) is a simple component in both its physical structure and in its operating principles. The structure, in its most basic form, consists of an array of metal electrodes deposited on a slice of quartz or other crystaline substrate. One set of electrodes acts as the input, whereas the other set of electrodes supplies the output. In addition, one or two inductors may be used for tuning purposes. These components, when packaged, comprise the basic device.

Figure 1 illustrates the simple operation of these devices. The input and output electrodes are shown

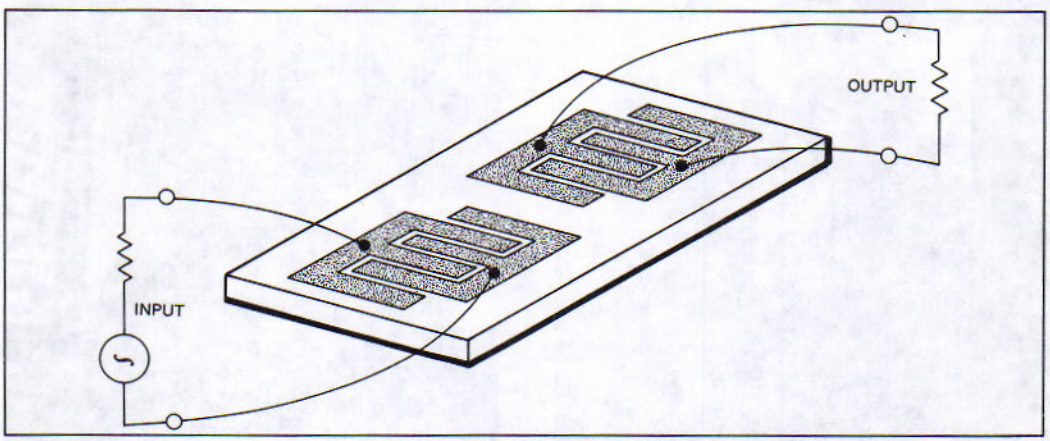



Figure 1. Surface Acoustic Wave (SAW) Device.

deposited on a piezoelectric material. The material undergoes mechanical stress when subjected to an electrical field, causing mechanical vibrations.

Figure 1 illustrates that when a voltage is applied to the input set of electrodes, which perform the function of an input transducer, an electrical field is generated between each pair of transducer fingers. The fingers act like plates of a capacitor, located side-by-side, as illustrated in figure 2.

The field generated between the electrodes causes the quartz crystal, where quartz is used as a substrate, to vibrate. These mechanical or acoustic vibrations then spread out in directions that are determined by the angle at which the substrate was cut from its parent crystal. One of these vibrations is a surface acoustic wave (SAW) that can be likened to the action of an ocean wave or to the rolling wave produced by an earthquake. This wave confines itself to the surface on the electrode side of the crystal, and penetrates only minutely into the substrate, thus deriving its name. Since the crystal is cut at a specific angle, the waves propagate in directions both toward and away from the output transducer. Waves that travel away from the output transducer are absorbed in the damping material (RTV), as shown in figure 2. Waves that travel toward the output transducer produce an eletric field between the fingers which, in turn, generate a voltage across the output. Converting surface acoustic waves to electrical energy is the reciprocal effect as that of generating surface acoustic waves at the input transducer.

## 3.0 TECHNICAL DESCRIPTION

This section describes the frequency and time response of SAW devices.

### 3.1 Center Frequency and Bandwidth

Surface acoustic waves are a series of crests and troughs that travel across the surface of the substrate. When the signal frequency is such that the spacing between a crest and trough is the same as the spacing between adjacent fingers, then a peak output occurs. In other words, the crests create and sum one polarity of voltage, and the troughs create the opposite polarity in the other set of electrode fingers. As the frequency varies on either side of the frequency of maximum, some cancellation occurs and the output voltage decreases. When the frequency is such that the sum of the voltages generated across the electrodes equals zero, a null, or transmission zero, is obtained. This can be seen in the filter frequency response curve shown in figure 3.

Center frequency (fo) is directly related to finger spacing and the bandwidth is determined by the null, or transmission zero frequencies, $f_{+1}$, $f_{-1}$, $f_{+2}$, $f_{-2}$, etc. In equation form:

$$fo = \frac{v}{2\ell}$$ (v = velocity, $\ell$ = spacing between adjacent fingers)

$$BW = \frac{fo}{N}$$ (N = number of finger pairs in each transducer)

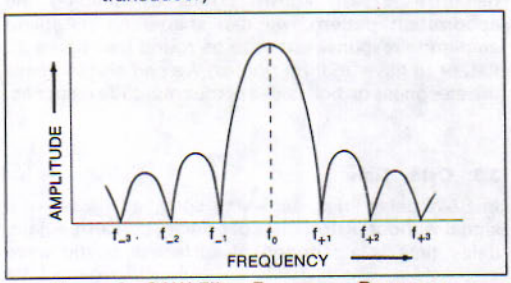



Figure 3. SAW Filter Frequency Response.

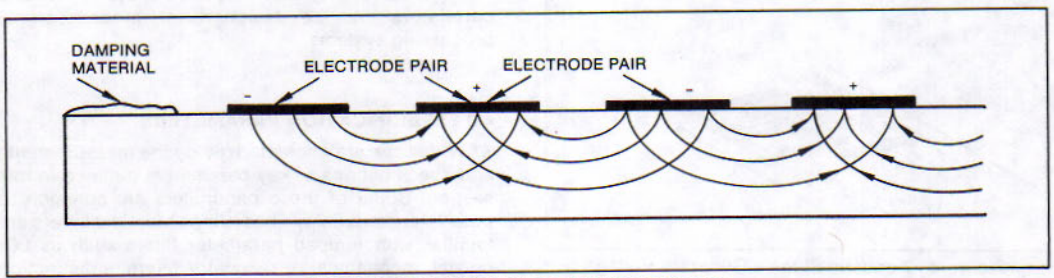



Figure 2. Electric Field Distribution Between Transducer Fingers.

### 3.2 Time Delay and Phase

Time delay in SAW bandpass filters remains constant with frequency change, thus, a linear phase is obtained. This relationship makes SAW filters unique in their operation. This is the result of the fact that velocity of surface acoustic waves remains constant with frequency change; therefore, the time required for a wave front to travel between transducers is a constant. This characteristic is very similar to that found in non-recursive digital filters and can be of great value to the system designer. In fact, the shape of the curve, shown in figure 3, can be varied by varying the amount of overlap between adjacent electrodes and the delay still remains constant with frequency change.

The concept of finger overlap is represented by the crosshatched regions in figure 4. When a surface acoustic wave front moves across the electrodes, a voltage that is proportional to the amount of finger overlap is generated by the transducer.

Therefore, if the wave is in the form of an impulse, the output amplitude response, with time, is identical to the shape of the finger overlap (which is commonly referred to as the apodization pattern). You may recall that if the response to an impulse is known, then, by applying the Fourier transform, the amplitude response is also known. Thus, by shaping the apodization pattern, we can shape the passband amplitude response either to be round (see figure 3), flat, or to have uniform ripples. We can also increase the steepness on both sides of the amplitude response.

### 3.3 Delay Time

In SAW delay lines, achieving specified delays of a signal without distortion is of primary concern. Again, delay time is a function of surface acoustic wave velocity and of distance between input and output transducer. This function is expressed as:

$$DT = \frac{d}{v}$$ (d = distance between transducer arrays and v = wave velocity)

Surface acoustic wave velocity is determined by the type of substrate material used. For ST-cut quartz the velocity is 3180 meters per second and for Lithium Niobate it is 3488 meters per second. Therefore, to obtain the same delay in both cases, the transducers, when Lithium Niobate is used, must be spaced further from each other than when quartz is used.

When choosing a substrate material, temperature characteristics of the material and its ability to achieve a required bandwidth with minimum loss are probably of greater importance than velocity. Where fractional bandwidths of less than 5 percent (bandwidth divided by center frequency) are required, an ST-cut quartz substrate should be used. This material has electro-mechanical coupling properties great enough to enable filter termination without excessive insertion loss. The concept of electro-mechanical coupling is similar to the limiting of bandwidth in an amplifier by shunt capacitance. This is because the input and output impedances of the SAW devices can be represented by a shunt RC; and the resistance and capacitance related by the electro-mechanical coupling. Where bandwidths greater than 5 percent are required, a Lithium Niobate substrate should be used. Lithium Niobate ($LiNbO_3$) is less stable than ST-cut quartz by more than an order of magnitude. However, because of the wider filter bandwidth this is of less importance.

The previous paragraphs covered filters and simple delay lines. By electrically separating the finger pairs, a tapped delay line can be formed. Also, by varying the spacing between fingers from one end of the transducer to the other, a dispersive (time delay varies with frequency) delay line can be realized. In this manner, compressors and expanders, convolvers and correlators can be designed for modern signal processing systems.

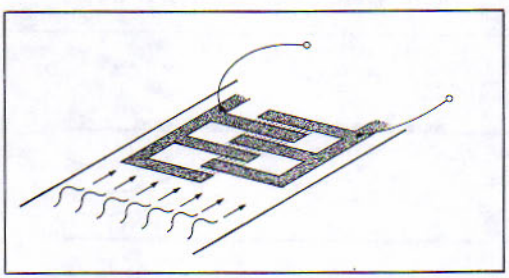


Figure 4. Acoustic Signals Generate Voltage Between Finger Overlaps.

## 4.0 SPECIFICATION PARAMETERS

SAW devices are characterized by the measurements and specifications of key parameters outlined in this section. Some of these parameters are common to both filters and delay lines. Since most designers are familiar with lumped parameter filters such as LC, crystal, mechanical or resonator filters, a distinction will be made where SAW technology basically differs.

### 4.1 Ripple Distortion

Ripple or response variation is the amplitude change over the SAW passband, between specified limits in frequency or in overall response. Compared with lumped parameter filters, where the overall number of peak-to-valley reversals in amplitude are equal to the filter poles, SAW filters have an overall smooth response with usually one or two main peaks. However, due to the triple transit effect, a fine grain ripple of short frequency exists that is normally low in magnitude. See figure 5. A 0.5 dB overall response variation over the 1 dB filter bandwidth is typical; however, this can be modified by specific shaping requirements. Fine grain ripple will typically be less than 0.25 dB but may be greater for wider bandwidth filters.

### 4.2 Bandwidth

The specified bandwidth is defined as the range of frequencies where the filter response provides either less (passband) or greater (stopband) attenuation than specified. Figure 6 shows a typical 3 dB bandwidth for the passband and 40 dB bandwidth for the stopband range.

The actual 3 dB bandwidth is greater than the fixed point difference and the actual 40 dB bandwidth is less than the fixed point difference.

### 4.3 Shape Factor

The shape factor is the ratio of the bandwidth at a high loss to that at a low loss. This is expressed in the following typical equation:

$$\text{Shape Factor (40/3)} = \frac{\text{BW40dB}}{\text{BW3dB}}$$

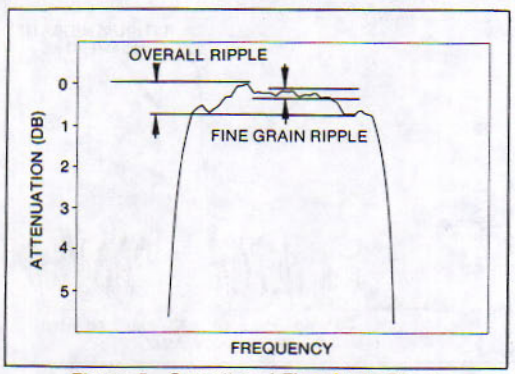



Figure 5. Overall and Fine Grain Ripple.

Shape factor is more often specified in lumped parameter filters to relate to the number of "poles". In SAW filters, the nature of the transition band, the desired bandwidth and the second-order effects are critical in determining the exact shape factor as compared to number of poles and finite zero realizations in lumped-parameter devices. Generally, low shape factors can be realized in SAW devices. Variations due to temperature and manufacturing tolerances make it necessary to specify frequency points and shape factors that are looser than the average response.

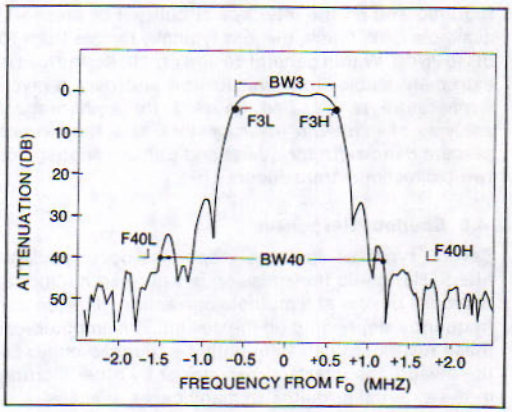



Figure 6. Actual Bandwidth and Specified 3 dB and 40 dB Points.

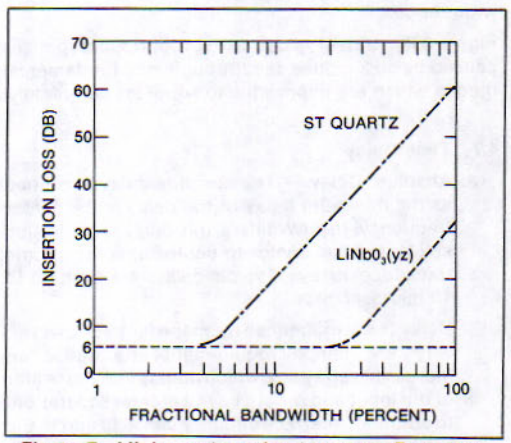



Figure 7. Minimum Insertion Loss as a Function of Fractional Bandwidth.

### 4.4 Center Frequency

Center frequency, which is sometimes a reference frequency, often is the arithmetic average of F3L and F3H. This number may or may not be meaningful depending on system parameters.

### 4.5 Insertion Loss

Insertion loss is the loss of the filter at its maximum response with respect to the circuit response at the same frequency, with the filter replaced by an input to output shorting element. Insertion loss depends on bandwidth, material used, triple transit suppression required and on the interface circuitry. For presently available SAW filters, the loss typically ranges from 10 dB to 25 dB. Within general design practices, the loss is extremely stable from unit to unit and over a given temperature range. See figure 7 for a theoretical analysis of minimum insertion loss as a function of percent bandwidth for quartz and Lithium Niobate for two bidirectional transducers.

### 4.6 Spurious Responses

Several types of spurious responses occur in SAW filters. Harmonic transmission is where an additional response occurs at a multiple or fraction of the center frequency, depending on the design. The amplitude of these responses can frequently be reduced either by the design, the interface circuitry or by other filtering in the external circuitry. In many cases, responses as great as 30 dB must be tolerated. It should be noted, however, that if shielding is adequate, the rejection is typically 60 dB to 80 dB or greater over an extremely wide range.

Figure 8 illustrates typical cases of spurious responses caused by bulk modes, feedthrough, and fundamental modes which are impossible to suppress completely.

### 4.7 Time Delay

a. Absolute Delay — The absolute delay is defined as the minimum delay or the delay at the center frequency. In SAW filters, this delay is controlled solely by the center-to-center spacing of the transducer arrays. Typical delays are from 0.1 to 10 microseconds.

   Delay is not influenced by shape factor. However, very low shape requirements do cause an increase in array size which means that the center of the input and output have a greater separation. In addition, interface circuitry can also add to the total delay.

b. Delay Variation — Delay variation, or delay distortion, is the variation of the delay over the fre-

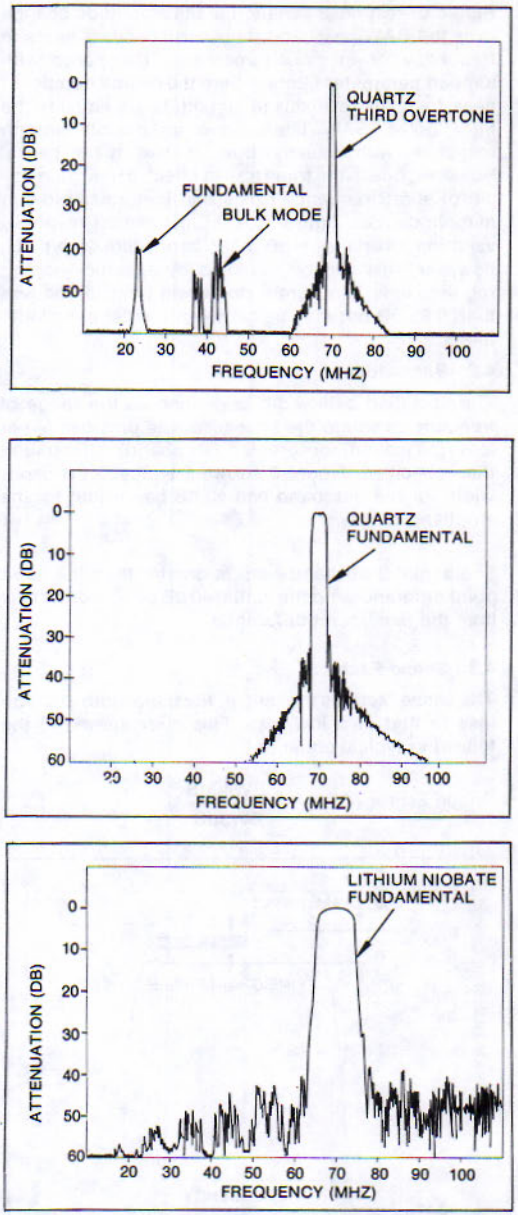



Figure 8. Spurious Responses in 3rd Overtone and Fundamental Mode Designs.

quency band of interest. Typically, this is the 1 dB bandwidth. An outstanding feature of SAW device technology is that delay variation is very small and is affected only by second-order effects, such as triple transit and interface circuitry. As a result, SAW filters do not require equalizers and are excellent for applications in data transmission, PSK, QPSK, BPSK, etc., where delay distortion is critical. For a comparison of delay variation in a typical SAW filter and in a lumped-parameter Butterworth filter, see figure 9.

### 4.8 Time Response

The time response is directly related to the overlap finger pattern although it is somewhat distorted by three factors: feed-through, triple transit, and regeneration.

a. Feed-Through — Since electro-magnetic waves travel at 100,000 times the speed of surface acoustic waves, precursor signals will be present in the SAW filter. By careful design and mechanical construction of filters or delay lines, these signals can generally be reduced to 40 dB or more below the desired response. See figure 10.

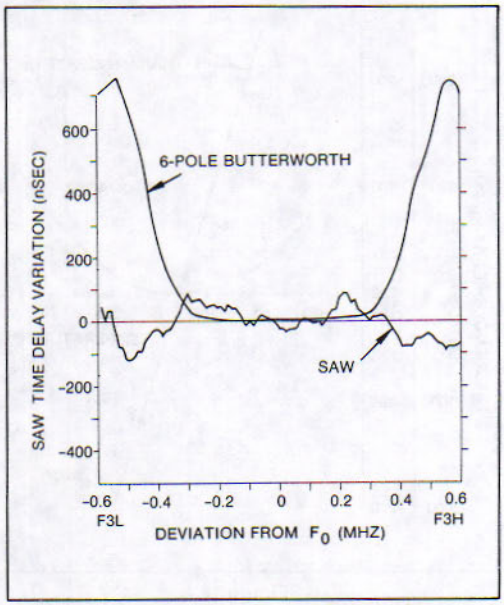



Figure 9. Delay Variations of SAW and Lumped Resonator Filters.

b. Triple Transit — Due to the bidirectional nature of the transducers, the acoustic signal is reflected back, from output to input, and back again arriving at three times the desired delay time. In choosing proper termination and other design criteria, this can be reduced to 40 dB or more below the desired time response.

c. Regeneration — Acoustic waves that are regenerated by the finger pairs, sometimes cause a slight "smearing" at the upper end of the desired time response. This occurs generally 40 dB or more below the main response.

### 4.9 Time — Bandwidth

This is a measure of the pulse compression/dispersion for a dispersion compression/expansion delay line. Devices that are presently available have a typical TBW (time-bandwidth) product of 30 to 150. Figure 11 shows a plot of time vs. bandwidth.

### 4.10 Temperature

The operating temperature range of SAW devices is limited by shifts allowable in their specification. Basic construction and materials used in these devices are extremely stable over a very wide temperature range, easily covering the -50°C to +85°C MIL range. Very high temperatures of +125°C are not desirable due to thermal expansion. However, they will cause no damage to the SAW devices. Temperature shift of the center frequency and delay time are important factors in SAW devices. Figure 12 shows frequency shifts for ST-cut quartz and Lithium Niobate substrates as a function of temperature.

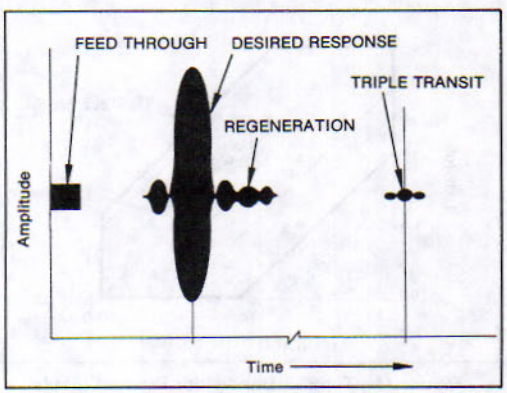



Figure 10.

### 4.11 Other Parameters

Solid construction makes SAW devices extremely insensitive to shock and vibration, making them comparable to hybrid microelectronic circuit components. All internal parts are secured by epoxy and elastomers.

Specifications:

| | |
|---|---|
| Shock | — MIL-STD-202, Method 213, Test Condition C |
| Vibration | — MIL-STD-202, Method 204, Test Condition E |
| Humidity | — MIL-STD-202, Method 103, Test Condition B |
| Salt Spray | — MIL-STD-202, Method 101, Test Condition A |

The extremely simple construction, use of redundant connection paths and proven procedures, make SAW devices highly reliable and result in long-life operation.

## 5.0 PACKAGING

To provide low-cost packaging, SAW devices use standard microelectronic packages wherever possible. It is sometimes necessary to use machined/casting type packages for some custom applications. The standard lower cost, hermetically-sealed packages available for SAW filters have high reliability and excellent performance criteria. Standard pin configurations are used on the packages shown in figure 13.

The TO-8 package is limited to wideband, short-delay devices not to exceed 10 mm in transducer length. Interface circuitry must generally be external.

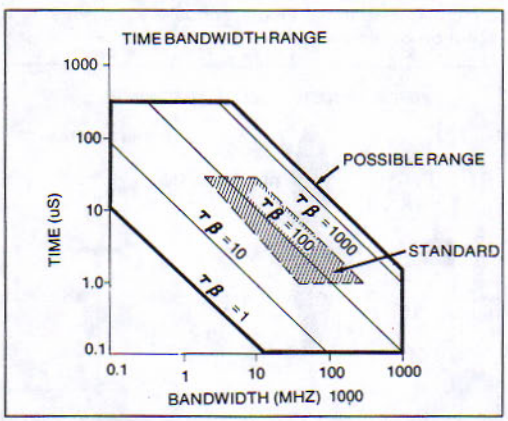



Figure 11. Time — Bandwidth Product Limits.

The Dual-Inline Packages (DIP) allow for much narrower bandwidths and greater delay times. Internal interface circuitry for matching fixed terminations may be included inside the package.

A low-cost plastic package may be used in high volume applications for commercial devices. Whatever your specific application might be, Rockwell packaging engineers will assist you in finding a cost/performance effective solution.

### 5.1 Shielding

Internal shielding is incorporated into the SAW filter package, where necessary. It might be necessary for the user to supply additional external input/output shielding to obtain the maximum system benefits.

### 5.2 Cost/Performance Trends

Since packaging is a high-cost element in SAW technology, Rockwell is continuing the development of packages to obtain better cost/performance effective solutions.

## 6.0 APPLICATION INFORMATION

This section describes application effects for interface circuits, buffering, shielding, power levels and spurious responses.

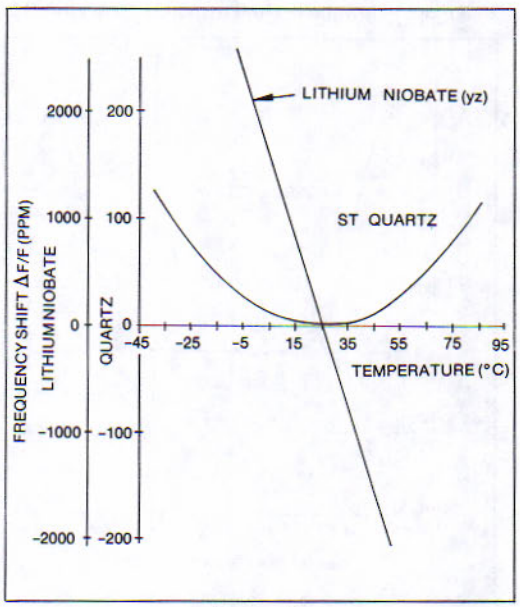



Figure 12.

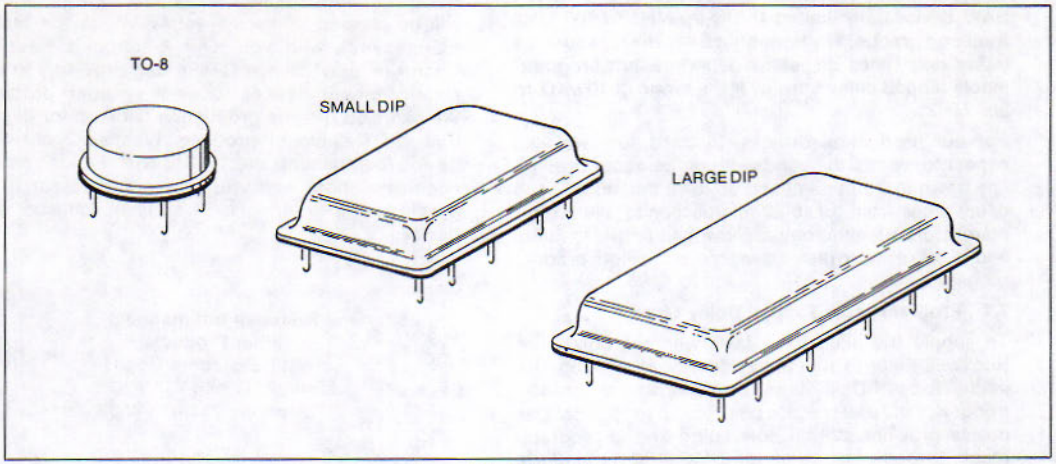



Figure 13. SAWD Packages.

### 6.1 Interface

In order to obtain maximum usage of surface acoustic wave device capabilities, it is necessary to properly optimize interface between the device and the circuit in which it is used. Rockwell Filter Products design engineers have extensive experience in the design of filter interface circuits and invite you to discuss your particular application with them.

If the SAWD must operate between a user specified source and load, then a combination of inductors, capacitors, resistors or transformers may be needed. In many cases, these components can be mounted inside the package, thus greatly simplifying the interface network required externally. If mounting these components inside the package is not desirable, Rockwell Filter Products engineers can recommend suitable external circuitry to be used. Generally, we can also supply interface circuits to match resistive source and load requirements from 25 ohms to 1250 ohms.

### 6.2 Buffering

When using SAW devices, it is desirable to keep the VSWR "seen" by the device as close to 1:1 as possible. This is to minimize the variation in performance characteristics of the device. A recommended maximum ratio is 1:1.25. Due to the accompanying mismatch, passband characteristics and insertion loss are the most susceptible characteristics.

### 6.3 Shielding

Adequate shielding in input and output terminals is important to achieve the full effect of suppressing unwanted signals in the filter. This is particularly true when using IC flatpack cases. Frequently, it has been found that the spacing between the circuit board and the package for wave soldering is sufficient to degrade performance appreciably. In this case, it is necessary to provide a barrier on the circuit board.

### 6.4 Power Levels

The power handling capabilities of SAW devices are generally controlled by the voltage and frequency that may appear across the transducers. Signal voltages of up to 5 to 10 volts are usually acceptable in the 30 to 300 MHz frequency range, with the higher voltage being applicable to the lower end of the frequency range.

### 6.5 Spurious Response

In some cases, spurious responses exist outside the passband. In these cases, it may be desirable to provide additional low-pass or high-pass filtering or to provide a bandpass "roofing" filter.

We invite you to contact Rockwell Filter Products' design engineers and they will recommend a solution to this problem. They will assist you in determining proper interface circuitry and to allow you to utilize all of the high performance characteristics that are built into Rockwell Filter Products surface acoustic wave devices.

## 7.0 FUTURE TRENDS

At present, our product line offerings for production SAW devices are limited to the 20 MHz to 100 MHz frequency range. We have built SAW devices such as filters, delay lines, dispersive delay lines and programmable tapped delay lines over the range of 10 MHZ to 500 MHZ.

For our production devices, in the future we also expect to extend the bandwidth range of our product line down to 0.1 percent and up to 25 percent and the delay times from 0.1 to 20 microseconds. We further plan to offer technology for low insertion-loss filters and to make improvements in time-bandwidth product ranges.

### 7.1 Programmable Tapped Delay Lines

To supply the need for a fast switching correlator, Rockwell Filter Products has developed a "Programmable Tapped Delay Line" that operates at a center frequency of 70 MHz with a chip rate up to 10 MHz. This device provides 128-bit correlation and is programmable through fast switching CMOS/SOS LSI chips. Coding may be changed in a serial mode in less than 5 microseconds at a 5-volt operating level. Eight chips are used to progam 16 taps each with possible serial/parallel combinations.

## CUSTOM REQUIREMENTS

Rockwell Filter Products welcomes your inquiry and will be pleased to discuss your SAW device custom requirements with you. Our Electronics Research Center or our Science Center can provide you with state-of-the-art devices for your research products. We can also provide production back-up for devices that are feasible to produce. Whatever your SAW device requirements are, let Rockwell Filter Products' engineers share with you 10 years of research and development experience in surface acoustic wave devices.

Contact:

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Telephone 714/833-4632



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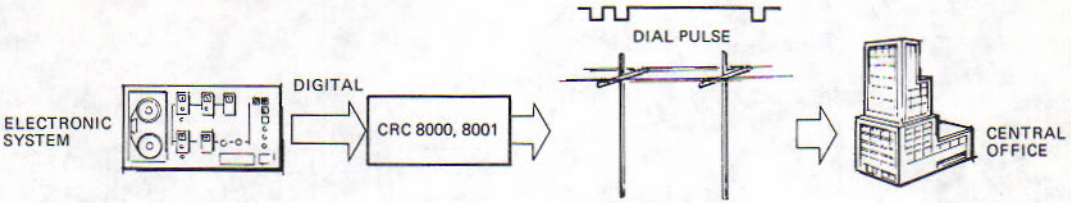
TELECOM
DEVICES

Rockwell International

# Rockwell MOS/LSI Telecommunication Products

## CRC 8000, 8001 — Binary to Dial Pulse Dialer




*16 Digit First-In-First-Out (FIFO) Memory*

*Asynchronous Operation*

*10pps (2KHz Clock) Dial Pulse Operation with a Minimum 650ms Interdigit Time*

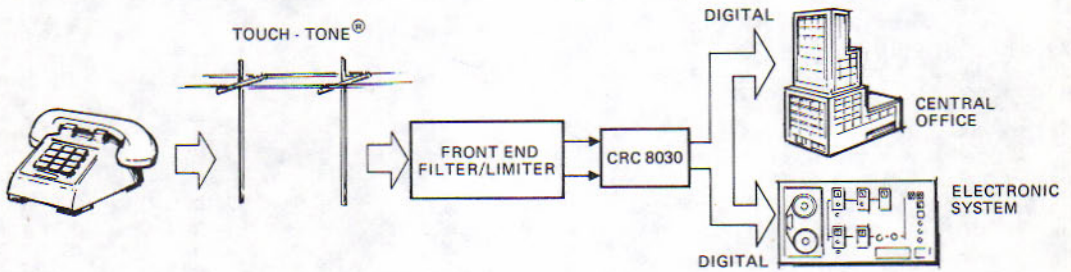
*20pps (4KHz Clock) Dial Pulse Operation with a Minimum 325ms Interdigit Time*

*CRC 8000, TTL Input compatible*

*CRC 8001, MOS Input compatible*

The dialer accepts binary data, stores the data in a first-in-first-out memory, and generates dial pulses at normal telephone rates. Internal timing is derived from an external 2KHz or 4KHz clock. With a 2KHz clock, a 10pps (60% break/40% make) dial pulse frequency having a minimum 650 ms interdigit time is generated. If a 4KHz clock is used, the dial pulse frequency is 20pps and the interdigit time is reduced to 325ms minimum. The memory section is necessary as the incoming data rate may be much faster than the normal dial pulse output rate. Binary codes one (1) through fifteen (15) produce the same number of dial pulses. A binary zero input produces sixteen (16) dial pulses.

## CRC 8030 — Dual Tone Multi-Frequency Detector




*Digital range filter detects all 16 Touch-Tone® signal combinations*

*Detects a tone pair in 22 ms to 39 ms*

*Digital logic impervious to frequency or bandwidth drift caused by time, temperature, or voltage*

*Automatic internal reset when no tones are present*

*Variable pulsewidth Strobe output provides increased talk-off protection*

*Binary or 2-of-8 coded outputs option*

*Inputs/outputs can be left floating when not used*

*Single or dual power supply option*

*On-chip oscillator – 3.579545 MHz color-burst crystal*

*Central-office-quality detection*

*Excellent talk-off protection – As little as one hit on Mitel test tape (CM 7290)*

Dual-Tone Multi-Frequency (DTMF) or Touch-Tone® signaling has made telephone communication faster, more efficient and more convenient than dial pulse signaling. Touch-Tone® telephone instruments or automatic dialers generate a tone pair representing the "dialed" number and send them over the lines to a receiver which detects the tones and reliably identifies the number.

Utilizing a digital filter algorithm, the CRC 8030 provides a low-cost and high-performance solution for DTMF detection.

A strobe output indicates when the output data are valid.

When linked with a front-end band-split filter/limiter, the CRC 8030 implements a complete DTMF receiver.

This design approach provides the optimum technological benefits of analog and digital design techniques.



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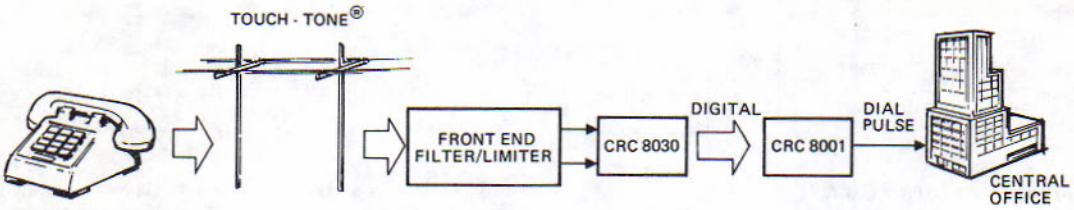
# DTMF to Dial Pulse Conversion




A DTMF to dial pulse converter can be easily implemented using the CRC 8030 and the CRC 8001.

For example, where electronic switching systems (ESS) are not available, the CRC 8030, a Dual-Tone Multi-Frequency Detector, and the CRC 8001, a Binary to Dial Pulse Dialer, can be utilized to convert Touch-Tone® signals to dial pulse signals. The CRC 8030 decodes Touch-Tone signals to their binary equivalent and the CRC 8001 converts the binary information to a train of pulses compatible with the standard telephone dial pulse signals.

Rockwell

# MOS/LSI TELECOMMUNICATIONS DEVICES

## TECHNICAL BULLETIN

## Binary to Dial Pulse Dialer

## CRC 8000, 8001

*16 Digit First-In-First-Out (FIFO) Memory*

*Asynchronous Operation*

*10pps (2KHz Clock) Dial Pulse Operation with a Minimum 650ms Interdigit Time*

*20pps (4KHz Clock) Dial Pulse Operation with a Minimum 325ms Interdigit Time*

*TTL Compatible*

### General Description

The CRC 8000 and CRC 8001 are P-channel enhancement mode MOS Binary to Dial Pulse Dialer utilizing ion implant, low threshold voltage processing. The Dialer accepts binary data, stores the data in a first-in-first-out memory, and generates dial pulses at normal telephone rates. Internal timing is derived from an external 2KHz or 4KHz clock. With a 2KHz clock, a 10pps (60% break/40% make) dial pulse frequency having a minimum 650 ms interdigit time is generated. If a 4KHz clock is used, the dial pulse frequency is 20pps and the interdigit time is reduced to 325ms minimum. CRC 8000 and CRC 8001 are identical except for their input interface. CRC 8000 inputs are TTL compatible and CRC 8001 inputs are MOS compatible. The devices are available in a 16 pin dual-in-line package.

The CRC 8000 can be installed in telephone central office stations to perform binary to dial pulse conversions. In areas where electronic switching systems (ESS) are not available, the CRC 8000 and CRC 8030, a Dual-Multi-Frequency Detector, can be utilized to convert Touch-Tone® signals to dial pulse signals. The CRC 8030 decodes Touch-Tone signals to their binary equivalent and the CRC 8000 converts the binary information to a train of pulses compatible with the standard telephone dial pulse signals.

### Operation

Digits, in the form of four binary inputs, are loaded asynchronously relative to the clock into a 16 digit first-in-first-out (FIFO) memory. This memory section is necessary as the incoming data rate may be much faster than the normal dial pulse output rate. Binary codes one (1) through fifteen (15) produce the same number of dial pulses. A binary zero input produces sixteen (16) dial pulses.

Dialer operation is controlled by the "Load" and "Memory Read Inhibit" inputs. A load pulse is required in order to input each digit into the FIFO. With a 2KHz clock, the maximum data entry rate is 500 digits per second.

The Memory Read Inhibit line can be used to delay the Dial Pulse Output. If the Memory Read Inhibit line is low (binary zero), the first digit entering the FIFO memory initiates the dialing sequence. The digit is transferred from the memory to a down counter that generates the appropriate number of dial pulses. Internal timing produces the proper interdigit time between pulse trains. If there is a pause in the binary data input, the circuit generates an extra length interdigit time in a manner identical to that created by a rotary dial.

A high level (binary one) Memory Read Inhibit prevents the reading of the memory thereby causing a pause. During this condition, existing data in the FIFO will be stored until Memory Read Inhibit is released (low level). When the inhibit line is changed from a low level (binary zero) to a high level (binary one), a dial pulse train in process will be completed before pausing. Additional digit data may be input to the FIFO memory as long as the 16 digit capacity is not exceeded.

The Busy output line is high when there is data in memory or dial pulses are being generated.

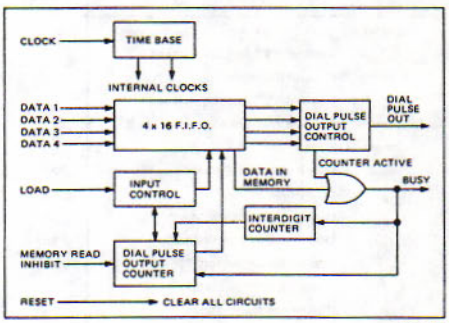
The Reset input is a "Master Reset". If the Reset input line is low, Busy is set to a low level and Dial Pulse Out is set to a high level. The outputs will remain in that state until a new digit is input to the FIFO.

### Technical Characteristics

MAXIMUM RATINGS

Non-operating voltages with no damage to device

| | |
|---|---|
| Supply Voltage $V_{DD}$ | $V_{SS}$ - 8.0V |
| Supply Voltage $V_{GG}$ | $V_{SS}$ - 21.0V |
| Positive Voltage on any pin | $V_{SS}$ + 0.3V |
| Negative Voltage on any pin | $V_{SS}$ - 20.0V |
| Power Dissipation at 25°C | 275mw |
| $V_{SS}$ = +5.0V, $V_{GG}$ = -12.0V | |
| Operating Temperature Range (case) | 0°C to +70°C |
| Storage Temperature Range (case) | -55°C to +150°C |

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CRC 8000, 8001 Binary to Dial Pulse Dialer

*RECOMMENDED OPERATING CONDITIONS/ELECTRICAL CHARACTERISTICS FOR 10pps OPERATION*

*Unless Otherwise Noted $V_{SS}$ = +5.0V, $V_{GG}$ = -12.0V, $V_{DD}$ = 0.0V, $0^oC \leq T_A \leq 70^oC$, and clock frequency = 2.0KHz ± 5%*

| PARAMETER | | MIN | TYP | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| **Power Supplies** | | | | | | |
| $V_{SS}$ | Supply Voltage | 4.75 | 5.0 | 5.25 | V | $V_{DD}$ = 0.0V See Note 1 |
| $V_{GG}$ | Supply Voltage | -13.0 | -12.0 | -11.0 | V | $V_{DD}$ = 0.0V |
| **Inputs** | | | | | | |
| $V_{IN}(0)$ | Logical "0" Input voltage | -1.0 | 0.0 | 0.8 | V | See Note 2 |
| $V_{IN}(1)$ | Logical "1" Input voltage | $V_{SS}$-0.7 | | $V_{SS}$+0.2 | V | See Note 2 |
| $C_{IN}$ | Input capacitance | | | 10 | pF | $V_{IN} = V_{SS}$ - 1.0V |
| **Input Timing** | | | | | | |
| $f_c$ | Clock repetition rate | 1.9 | 2.0 | 2.1 | KHz | See Note 3 |
| $t_{pc}$ | Clock duty cycle | 45 | 50 | 55 | % | Applies to all inputs including clock |
| $t_r$ | Input pulse rise time | 40 | | 500 | ns | Applies to all inputs including clock |
| $t_f$ | Input pulse fall time | 40 | | 500 | ns | Applies to all inputs including clock |
| $t_{LH}$ | Load pulse width "High" | 1.9 | | | ms | See Timing Diagram |
| $t_{LL}$ | Load pulse width "Low" | 0.1 | | | ms | See Timing Diagram |
| $t_{d1}$ | Data set-up time | | | 0.5 | ms | See Timing Diagram |
| $t_{d2}$ | Data hold time | 1.75 | | | ms | See Timing Diagram |
| $t_{ML}$ | Memory Read Inhibit stable time relative to Load | | | 650 | ms | See Note 4 |
| $t_{MDP}$ | Memory Read Inhibit stable time relative to Dial Pulse Out | | | 650 | ms | See Note 4 |
| $t_R$ | Reset pulse width | 1.0 | | | $\mu s$ | See Timing Diagram |

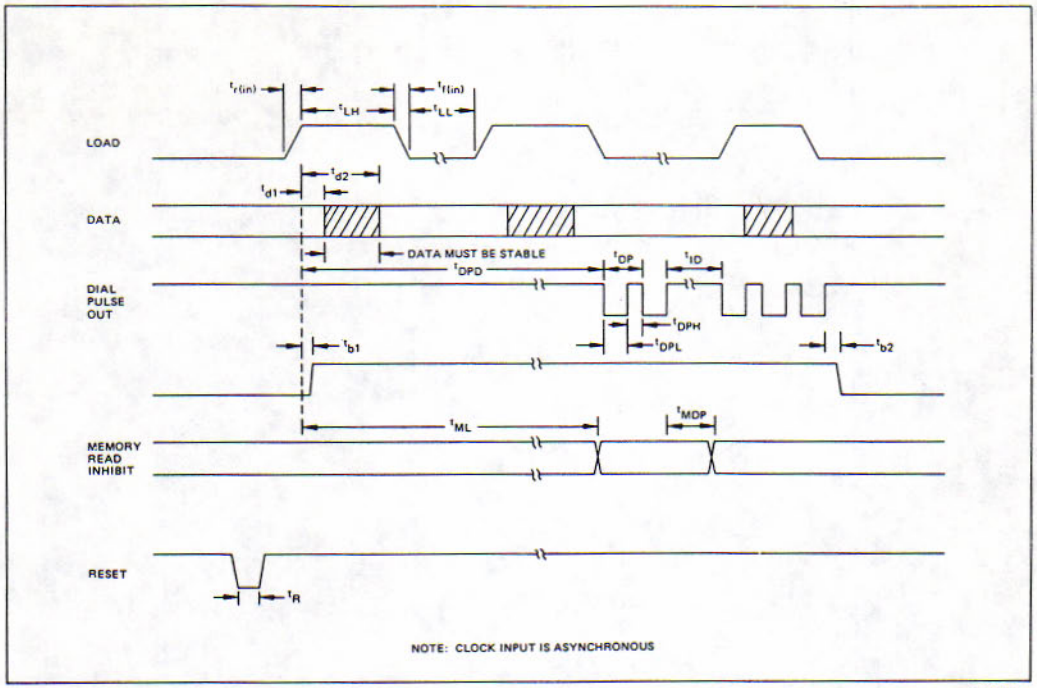
## NOTES

1. Other supply parameters are permissible including $V_{SS}$ = 0.0V, $V_{DD}$ = -6V, and $V_{GG}$ = -12V. Input/output parameters will be adjusted accordingly.

| | Min. | Typical | Max. |
|---|---|---|---|
| $V_{in}$ (0) | -7.0 | -6.0 | -5.2 |
| $V_{in}$ (1) | -0.7 | 0.0 | +0.2 |
| $V_{out}$ (0) | 0.0 | 0.0 | -5.6 |
| $V_{out}$ (1) | -2.6 | 0.0 | 0.0 |

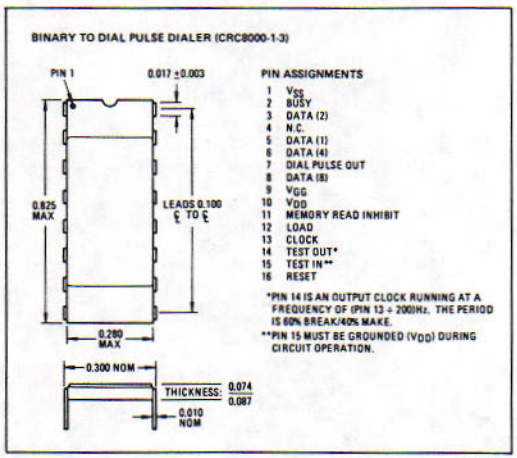
2. All inputs of CRC 8000 have "on chip" 3200 ±30% ohm pull-up resistor to $V_{SS}$ and are suitable for being driven by TTL. All inputs of CRC 8001 have a high impedance input (no pull-up resistor) and are suitable for interface with MOS devices.
3. For 20pps operation, a 4.0 KHz is clock required. If the clock has a 5% tolerance, the operating specification can be derived from the above table. All parameters will remain the same except for the following timing parameters which will be reduced by one half: $t_{LH}$, $t_{LL}$, $t_{d2}$, $t_{ML}$, $t_{MDP}$, $t_{DPD}$, $t_{DP}$, $t_{DPL}$, $t_{DPH}$, $t_{ID}$. Similarly, a 10 KHZ clock could be used, producing a 50pps output rate.

| PARAMETER | | MIN | TYP | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| **Outputs** | | | | | | |
| $V_{out}(0)$ | Logical "0" output voltage | | | 0.4 | V | $I_{sink}$ = 1.6 mA |
| $t_f$(out) | Output fall time | | | 500 | ns | 90% to 10% |
| $V_{out}(1)$ | Logical "1" output voltage | 2.4 | | | V | $I_{source}$ = 0.1 mA |
| $t_r$(out) | Output rise time | | | 400 | ns | 10% to 90% |
| **Output Timing** | | | | | | |
| $t_{DPD}$ | Dial Pulse Out Delay | 700 | | 900 | ms | |
| $t_{DP}$ | Dial Pulse Period | 95 | 100 | 105 | ms | See Note 3 |
| $t_{DPL}$ | Dial Pulse Width "Low" | 57 | 60 | 63 | ms | and Timing |
| $t_{DPH}$ | Dial Pulse Width "High" | 38 | 40 | 42 | ms | Diagram |
| $t_{ID}$ | Dial Pulse Interdigit Time | 650 | 740 | | ms | |
| $t_{b1}$ | Busy Low/High Delay | | | 2.1 | ms | |
| $t_{b2}$ | Busy High/Low Delay | | | 10 | $\mu s$ | |
| **Power** | | | | | | |
| $P_D$ | Power Dissipation | | 125 | 275 | mw | |




30377-6

4. To prevent a dial pulse train from being output, Memory Read Inhibit must be stable prior to initiating that pulse train. This stabilization point is specified for two cases: (1) If no pulse trains are presently in process (e.g., the device has been reset), Memory Read Inhibit must be stable 650ms after the load pulse was initiated; (2) If a pulse train is in process, to prevent the next pulse train from being output, Memory Read Inhibit must be stable 650ms after the interdigit time was initiated.

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## Packaging and Ordering Information

The Binary to Dial Pulse Dialer is available in a 16-pin hermetically sealed ceramic dual-in-line package (see pin assignments and package dimension diagram). Order by type numbers.
CRC 8000-1-3 (ceramic DIP) 765-1892-001
CRC 8001-1-3 (ceramic DIP) 765-5841-001

For further information on Rockwell MOS/LSI Standard Products, call or write your local Rockwell Sales Office at:

MOS/LSI Products
Rockwell International
Microelectronic Devices
4311 Jamboree Blvd.
Newport Beach, California 92663
Telephone: 714-833-4638, 4634
TWX 910-595-1705

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Rockwell

# MOS/LSI TELECOMMUNICATIONS DEVICES
## DATA SHEET

# Dual Tone Multi-Frequency Detector

*Digital range filter detects all 16 Touch Tone® signal combinations*

*Detects a tone pair in 22 ms to 39 ms*

*Digital logic impervious to frequency or bandwidth drift caused by time, temperature, or voltage*

*Automatic internal reset when no tones are present*

*Variable pulsewidth Strobe output provides increased talk-off protection*

*Binary or 2-of-8 coded outputs option*

*Inputs/outputs can be left floating when not used*

*Single or dual power supply option*

*On-chip oscillator — 3.579545 MHz color-burst crystal*

*Central-office-quality detection*

*Excellent talk-off protection — As little as one hit on Mitel test tape (CM 7290)*

### DTMF Signaling and Receivers

Dual-Tone Multi-Frequency (DTMF) or Touch-Tone® signaling has made telephone communication faster, more efficient and more convenient than dial pulse signaling. Touch-Tone® telephone instruments or automatic dialers generate a tone pair representing the "dialed" number and send them over the lines to a receiver which detects the tones and reliably identifies the number. DTMF signals are defined by a 4 x 4 audio tone matrix as illustrated in figure 1. Each digit is represented by one tone from the low-group and one tone from the high-group. These non-harmonically related frequencies protect the message against false-keying by stray signals and voice-generated tones.

A DTMF receiver must recognize the dual tones within a certain bandwidth while tolerating dial tone, noise, input amplitude variation and "twist" or amplitude differential between the two tones. In addition, the receiver has to comply with timing restrictions imposed by the DTMF generation process and meet other specific requirements of the particular application.

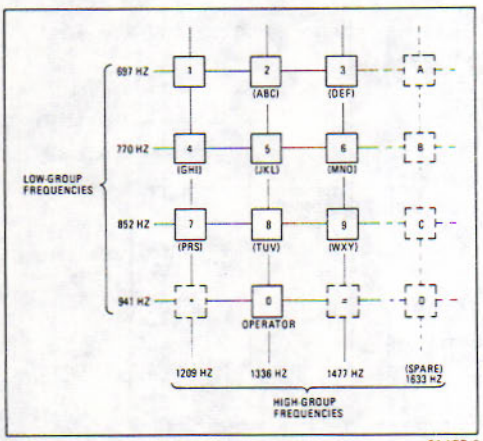


*Figure 1. Touch Tone® Pad (Dual Tone Multi-Frequency Signaling)*

### CRC 8030 General Description

The CRC 8030 provides a low-cost and high-performance solution for DTMF detection. Utilizing a unique digital filter algorithm, the patented* CRC 8030 performs the key critical functions of a DTMF receiver. When used in conjunction with a front-end band-split filter/limiter, the CRC 8030 implements a complete DTMF receiver (figure 2). This design approach provides the optimum technological benefits of analog and digital design techniques.

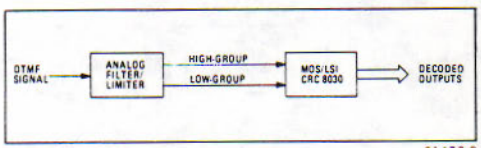


*Figure 2. DTMF Receiver Utilizing CRC 8030*

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*U.S. Patent No. 4016371

The exact requirements for the front-end filter/limiter vary with the particular receiver application. For example, high quality central office receivers require a more selective front-end filter. Conversely, low-noise environment keyphone systems can use a less stringent front-end filter design.

DTMF receivers historically have been implemented with all-analog filtering techniques, i.e., phase-locked loops, LC filters and active filters. Compared to a phase-locked-loop receiver, the CRC 8030 provides much superior performance. Compared to LC or active filter receivers, the CRC 8030 can be manufactured for a significantly lower cost while providing improved performance. The CRC 8030 provides the economy, performance, size and reliability benefits of digital MOS/LSI. The CRC 8030 is packaged in a 28-pin DIP.

## Applications

The CRC 8030 can be applied to all systems requiring DTMF detection. This includes the traditional telephony systems: keyphone, PABX, central office, intercom and mobile radio communications. Other applications include computer signaling and control systems. Where it is necessary to interface with a dial pulse system, the CRC 8030 and the CRC 8000 (a Binary-to-Dial-Pulse Dialer) implement a DTMF-to-dial-pulse conversion system.

The CRC 8030 has been functionally designed to provide optimum performance for a wide variety of DTMF detection applications.

## Operation

The CRC 8030 is a DTMF detector implemented with PMOS ion-implantation processing. This detector accepts group-filtered and square-shaped DTMF frequencies and converts them to binary data or 2-of-8 coded data in 22 ms to 39 ms; out-of-tolerance frequencies are rejected. The device ignores the first few pulses of the input signal in order to prevent errors in detection due to the transients from the Touch-Tone® pad. The signal is then analyzed several times by a digital range filter prior to being accepted as valid. As soon as the range filter has recognized a frequency below 1680 Hz, the Audio Detect (AUD) output is enabled. This output provides the user with a signal for controlling the limiter gain at the receiver front-end. A Strobe (ST) output indicates when the output data are valid.

Once a digit is accepted as valid, the CRC 8030 will ignore any change in tone frequency until either the high-group or low-group tone disappears for more than 10 ms. When this occurs, the device is reset internally and will be ready to accept another Touch-Tone® digit. This feature provides immunity to frequency drift that could be caused by Doppler shift. Should a frequency in either the high- or low-group disappear for less than 10 ms, the gap is bridged resulting in only one digit.

A block diagram of the CRC 8030 is shown in figure 3. The functions include timebase generation, wave shaping circuitry, range counters with correlation circuitry, and the output timing and decoding functions.

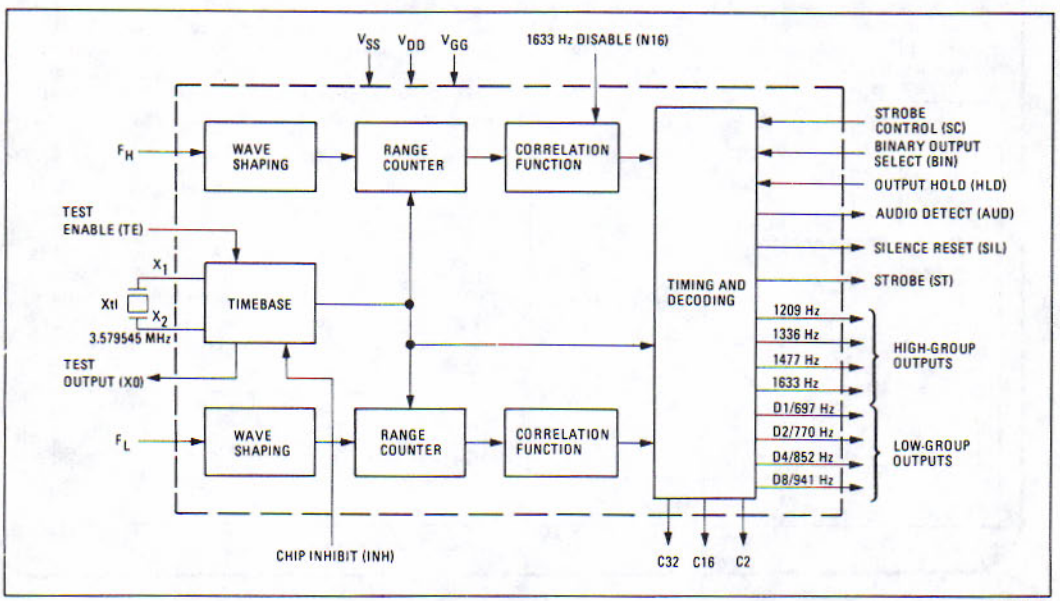


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*Figure 3. CRC 8030 Block Diagram.*

## Technical Characteristics

Maximum Ratings: Non-operating voltages with no damage to device —

Supply Voltage $V_{DD}$ . . . . . $V_{SS}$ -8.0V
Supply Voltage $V_{GG}$ . . . . . $V_{SS}$ -21.0V
Positive Voltage on any pin . . . . . $V_{SS}$ +0.3V
Negative Voltage on any pin . . . . . $V_{SS}$ -20.0V

Power Dissipation ($0^{o}C \leq T_A \leq 70^{o}C$) . . . . . 200 mW
Operating Temperature Range (case) . . . . $0^{o}$ to $+70^{o}C$*
Storage Temperature Range (case) . . . $-65^{o}C$ to $+150^{o}C$

*An extended temperature range device will be available in the future.

## Inputs and Outputs

The inputs and outputs are illustrated in figure 3 and are described below with a positive logic convention assumed. However, the operation is defined such that when a 2-of-8 output format is chosen, the Strobe and the low-group outputs display data with a negative logic convention. The high-group outputs always display data in a negative logic convention. Detailed timing is shown in the timing diagram, figure 4.

### Inputs

Logic levels are MOS compatible. Inputs BIN, INH, HLD, SC, N16, and TE have on-chip active pull-up devices to $V_{ss}$ with a minimum of 50 KΩ resistance; therefore, no connection is required to these pins if a high-level input is desired.

- High- and low-group DTMF signals (FL, FH) — These are the filtered and square-shaped DTMF tones. When no signal is present, both input levels should be low (most negative level).
- Binary Output Select (BIN) — If this input is low (most negative level), the decoded outputs are displayed in a binary format and Strobe (ST) pulses from a normally low state to a high state (figure 4). If this input is high or open, the decoded outputs are displayed in a 2-of-8 code and Strobe pulses from a normally high state to a low state.
- Chip Inhibit (INH) — If this input is low, the device is inhibited from decoding any DTMF tones. When decoding binary, the outputs stay low. When decoding 2-of-8, the outputs stay high. If this input is high or open, the outputs function normally. Chip Inhibit is also a master reset except for the output data registers when Output Hold is low.
- Output Hold (HLD) — If this input is low, the output data, if valid, are stored in the output registers. If the input is high or open, the outputs will function normally.
- Strobe Control (SC) — This input controls the pulsewidth of the Strobe (ST) output.

  When Strobe Control is high or open, the signal is analyzed for the full 39 ms data acquisition ($t_{DA1}$, Long Strobe) period. If the input tone-pair is detected within 22 ms, then the Strobe (ST) output pulsewidth is at a maximum of 17 ms. If detection takes more than 22 ms, the Strobe pulsewidth is reduced by the extra time needed for detection. If the signal is detected after the 39 ms period, no Strobe pulse will occur.

  When Strobe Control is low, the input signal is analyzed for a 33 ms period ($t_{DA2}$, Short Strobe). If the tone is detected within 25 ms after its inception, then the Strobe pulsewidth is 8 ms. If detection occurs after 25 ms, then the Strobe pulsewidth is reduced by the lag time. If no signal is detected within the 33 ms period, no Strobe pulse will occur.

  When a Short Strobe is selected, a higher quality input signal must be present in order to be accepted as a valid signal. Thus, voice or noise signals on the telephone line, which require a longer detection time, will be ignored by the chip. As a result, the device has a higher immunity to false-keying when Strobe Control is low.

  In either case, the tone pair may be detected, but the Strobe signal may not necessarily be generated, depending on the quality of the input tone-pair.
- 1633 Hz Disable (N16) — If this input is low, the device will not respond to the 1633 Hz tone, thus improving the talk-off rate. If this input is high or open, the device will respond to the 1633 Hz tone.
- Clock Inputs and Control (X1, X2, TE) — The CRC 8030 contains an on-chip oscillator for a 3.57954 MHz parallel resonant crystal. This crystal is connected to X1 and X2 and TE is held high or left open. As an option, an external 447.443 kHz oscillator can be used to clock the CRC 8030. In this case, X1 is the 447.443 kHz clock input, X2 is left open, and TE is held low. For some applications (e.g., using several CRC 8030 devices on a board), it is possible to drive the chip with an external 3.579545-MHz clock at pin X2, while leaving the TE pin open, and tying pin X1 to $V_{SS}$.

### Outputs

All outputs feature open-drain devices. With a single-power supply ($V_{GG} = V_{DD}$), they will drive LPTTL, MOS or CMOS inputs. With a dual power supply, they will drive the base of a transistor. The open-drain output devices must be tied through a pull-down resistor to a negative voltage between $V_{DD}$ and $V_{GG}$ (when used); the value of this resistor depends upon the type of interface. Typically:

| Resistor | Interface |
|---|---|
| 1.5KΩ | LPTTL |
| 10.0KΩ | MOS or CMOS |
| 7.5KΩ | Base of a Transistor |

These outputs can also drive LEDs. For more design details, consult the Collins Application Note, "CRC 8030 Telephone DTMF Receiver".

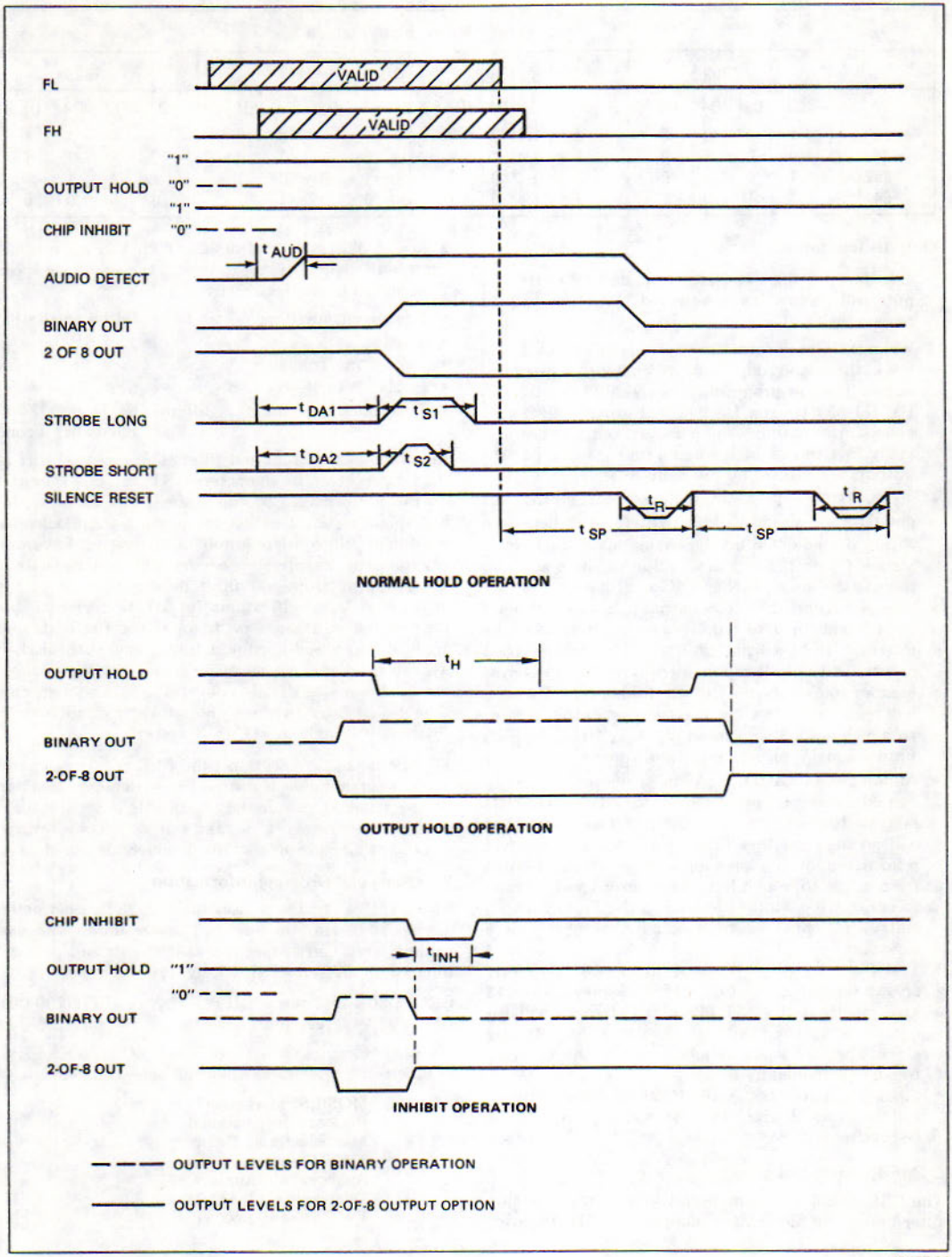
- Decoded Outputs (D1/697 Hz, D2/770 Hz, D4/852 Hz, D8/941 Hz, 1209 Hz, 1336 Hz, 1477 Hz, 1633 Hz) — These outputs display decoded information in either a binary or a 2-of-8-coded format as described below.

  When a 2-of-8 format is selected (BIN input is held high or left open), all 8 outputs are utilized. When a particular digit is decoded, the corresponding high- and low-group outputs go low (figure 1). For

*RECOMMENDED OPERATING CONDITIONS/ELECTRICAL CHARACTERISTICS*
*Unless Otherwise Noted $V_{SS}$ = +5.0V, $V_{GG}$ = -8.0V, $V_{DD}$ = 0.0V*
*0°C ≤ $T_A$ ≤ 70°C*
*Positive Logic*

| PARAMETER | | MIN. | TYP. | MAX. | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| **Power Supplies** | | | | | | |
| $V_{SS}$ | | +4.75 | +5 | +5.25 | V | |
| $V_{GG}$ | | -13.0 | -8.0 | $V_{DD}$ | V | |
| $V_{DD}$ | | | | 0 | | |
| **Inputs** | | | | | | |
| $V_{IN}(0)$ | Logical "0" input voltage | -13.0 | -8.0 | $V_{SS}$-4.0 | V | |
| $V_{IN}(1)$ | Logical "1" input voltage | $V_{SS}$-0.7 | | $V_{SS}$+0.2 | V | |
| $R_{IN}$ | Input impedance | 50 | | | kΩ | |
| $C_{IN}$ | Input capacitance | | | 10.0 | pF | $V_{IN}$ = $V_{SS}$-1.0V |
| $t_r$ & $t_f$ | Input voltage rise or fall time | | | 15.0 | μS | Voltage swing 10% to 90% of final level |
| **Input Timing** | | | | | | |
| $F_1$ | Clock Crystal Frequency | | 3.579545 | | MHz | ±0.005% |
| $F_2$ | Optional Clock Frequency | | 447.443 | | KHz | ±0.005% |
| DC | Clock duty cycle | 45 | 50 | 55 | % | Optional Clock |
| $t_r$ | Input clock pulse rise time | 40 | | 200 | ns | 10% to 90% of final level (Optional Clock) |
| $t_f$ | Input clock pulse fall time | 40 | | 200 | ns | 90% to 10% of final level (Optional Clock) |
| Detected Frequencies Low Group | | | 697 | | Hz | Bandwidth range: −1.9 to −3.2% |
| | | | 770 | | Hz | |
| | | | 852 | | Hz | |
| | | | 941 | | Hz | |
| Detected Frequencies High Group | | | 1209 | | Hz | +2.0 to +3.3% |
| | | | 1336 | | Hz | |
| | | | 1477 | | Hz | |
| | | | 1633 | | Hz | |
| IDC | Input signal (FL or FH) duty cycle | 30 | 50 | 70 | % | |
| **Outputs*** | | | | | | |
| $V_{OUT}(0)$ | Logical "0" output voltage | | | | | $V_{GG}$ + $R_L$ $I_{sink}$ |
| $t_f$(OUT) | Output fall time | | | | | 2.2 $R_L$ $C_L$ |
| $V_{OUT}(1)$ | Logical "1" output voltage | $V_{SS}$-0.4 | | | V | $I_{SOURCE}$ = 2.0 mA |
| $t_r$(OUT) | Output rise time | | | 4 | μS | 10% to 90% of final level (with 30 pF load) |
| **Output Timing** | | | | | | |
| $t_{SP}$ | Silence Period | 9.4 | 10 | 10.6 | ms | |
| $t_R$ | Silence Pulsewidth | 1.0 | 1.1 | 1.2 | ms | |
| $t_{DA1}$ | Data Acquisition Time Option 1 | 22 | | 39 | ms | |
| $t_{DA2}$ | Data Acquisition Time Option 2 | 25 | | 33 | ms | |
| $t_{AUD}$ | Audio Detection Time | 1.5 | 5 | 8 | ms | |
| $t_H$ | Output Hold Set-up Time | 10 | | | μS | |
| $t_{INH}$ | Chip Inhibit Pulsewidth | 2 | | | μS | |
| $C_2$ | Clock | | 2 | | kHz | |
| $C_{16}$ | Clock | | 16 | | kHz | ±0.1 % |
| $C_{32}$ | Clock | | 32 | | kHz | |
| $t_{S1}$ | Strobe Pulsewidth Option 1 | 0 | | 17 | ms | |
| $t_{S2}$ | Strobe Pulsewidth Option 2 | 0 | | 8 | ms | |
| **Power** | | | | | | |
| $P_{D1}$ | Power Dissipation (Dual Power Supply) | | | 200 | mW | $V_{SS}$ = 5.25V; $V_{GG}$ = -13V |
| $P_{D2}$ | Power Dissipation (Single Power Supply) | | | 180 | mW | $V_{SS}$ = 5.25V; $V_{GG}$ = $V_{DD}$ = 0V |

*For a full description of the output buffer capabilities, refer to the CRC 8030 Application Note.




21477-12

*Figure 4. Timing Diagram*

| Touch-Tone® Matrix: Binary Outputs | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1209 | | | | 1336 | | | | 1477 | | | | 1633 | | | |
| | D1 | D2 | D4 | D8 | D1 | D2 | D4 | D8 | D1 | D2 | D4 | D8 | D1 | D2 | D4 | D8 |
| 697 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 770 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 852 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 941 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

21477-13

**Outputs (continued)**

example, for digit 1, D1/697 Hz and 1209 Hz outputs will go low when detected. All other outputs remain high.

When the binary format is selected (BIN input is held low), the high-group outputs operate as described above. The low-group outputs (D1/697 Hz, D2/770 Hz, D4/852 Hz and D8/941 Hz) provide the binary coded information. These binary outputs are normally low and go high when a tone is detected. The outputs are defined by the above matrix:

- Strobe (ST) — This output indicates when the output data are valid. Validity is defined as detection within 39 ms or 33 ms depending upon the level of Strobe Control. For a description of the operation, refer to the inputs BIN and SC and figure 4.
- Silence Reset (SIL) — This output pulses to a low level when silence is detected. This occurs 9 ms after the interruption of a signal on either high- or low-group inputs. This output can be used to reset any external logic or to exercise the Output Hold option. The chip will reset itself after the Silence Reset output returns to a high level. Silence reset pulses at 10 ms intervals until a signal is present on either $F_L$ or $F_H$.
- Audio Detect (AUD) — Audio is defined as energy carried by any frequency lower than 1680 Hz. AUD remains low when both FL and FH are low; AUD will go high if either FL or FH is toggling and will return to a low level as soon as Silence Reset returns from a low to a high level. This output may be used to control the admissible level in the Front-End circuitry (off-chip) or to give advance notice of a tone-pair.
- Test Output (X0) — When using the 3.579545 MHz crystal on-chip oscillator, X0 will display a 447.443 kHz clock. If the 447.443 kHz external oscillator option is utilized, X0 will display a 55.930 kHz clock. The X0 output frequency will be the X1 input frequency divided by 8.
- Clock Outputs (C2, C16, C32) — These outputs will generate 2 kHz, 16 kHz and 32 kHz clocks, respectively.

**DTMF Receiver Design**

The CRC 8030, in conjunction with a front-end analog filter/limiter, implements a complete DTMF receiver. Figure 2 illustrates this design. With this approach, a central-office-quality receiver with the following specification can be implemented:

- Input Dynamic Range . . . . . -26 dBm to +6 dBm
- Twist . . . . . -8 dB to +4 dB
- Valid Tone Tolerance . . . . . ±1.5%
- Invalid Tone Reject Limit . . . . . ±3.5%
- Tone Burst (minimum) . . . 40 ms ON, 11 ms OFF at 12 bursts per second

Inasmuch as the front-end filter is an essential part of the total receiver, its characteristics have a major impact on the performance of the system. For example, for high-quality central-office receivers, a more selective front-end filter is required. Conversely, low-noise environment keyphone systems will operate with a less stringent front-end filter design. In view of the differences in specifications for DTMF receivers, the front-end design must be tailored for the particular application. Several manufacturers have off-the-shelf hybrid products which meet these filtering requirements. For more details concerning these design considerations, refer to the Collins "Application Note — CRC 8030 Telephone DTMF Receiver"

For specialized applications, the CRC 8030 has several mask programmable features. The parameters that can be programmed include the bandwidth, detection time, strobe time, silence time, and output decode format. Contact Collins Applications Engineering for details.

**Packaging and Ordering Information**

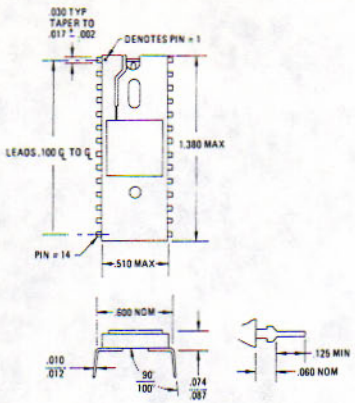
The DTMF Detector is available in a 28-pin, hermetically sealed ceramic dual-in-line package and in a 28-lead ceramic chip carrier (see pin assignments and package dimension diagrams). Order by type number.

CRC 8030-1-3 (ceramic DIP) . . . . 765-5795-001
CRC 8030-4-3 (ceramic carrier) . . . 765-5795-003

For further information on Rockwell MOS/LSI Standard Products, call your local Rockwell Sales office or:

MOS/LSI Marketing
Rockwell International
Microelectronic Devices
3310 Miraloma Avenue
Anaheim, California 92803
Telephone (714) 632-2558
TWX 910-591-1698

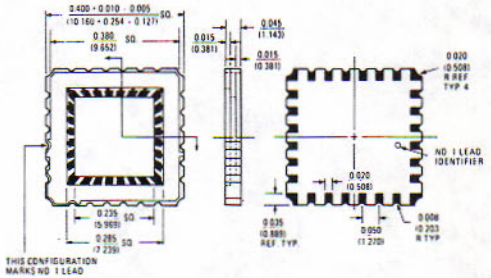
## DTMF DETECTOR (CRC 8030-1-3)




| PIN NO. | FUNCTION | PIN NO. | FUNCTION |
|---|---|---|---|
| 1 | $V_{SS}$ | 15 | 1209 HZ |
| 2 | 1633 HZ | 16 | HLD |
| 3 | SIL | 17 | SC |
| 4 | INH | 18 | $V_{DD}$ |
| 5 | C2 | 19 | D4/852 HZ |
| 6 | C16 | 20 | D8/941 HZ |
| 7 | C32 | 21 | ST |
| 8 | X2 | 22 | D2/770 HZ |
| 9 | $V_{GG}$ | 23 | BIN |
| 10 | X1 | 24 | FL |
| 11 | TE | 25 | FH |
| 12 | X0 | 26 | D1/697 HZ |
| 13 | AUD | 27 | 1477 HZ |
| 14 | 1336 HZ | 28 | N16 |

21477-14

## DTMF DETECTOR (CRC 8030-4-3)




PINS ARE READ COUNTERCLOCKWISE

| PIN NO. | FUNCTION | PIN NO. | FUNCTION |
|---|---|---|---|
| 1 | $V_{SS}$ | 15 | 1209 HZ |
| 2 | 1633 HZ | 16 | HLD |
| 3 | SIL | 17 | SC |
| 4 | INH | 18 | $V_{DD}$ |
| 5 | C2 | 19 | D4/852 HZ |
| 6 | C16 | 20 | D8/941 HZ |
| 7 | C32 | 21 | ST |
| 8 | X2 | 22 | D2/770 HZ |
| 9 | $V_{GG}$ | 23 | BIN |
| 10 | X1 | 24 | FL |
| 11 | TE | 25 | FH |
| 12 | X0 | 26 | D1/697 HZ |
| 13 | AUD | 27 | 1477 HZ |
| 14 | 1336 HZ | 28 | N16 |

21477-15



*NOTE: Collins MOS/LSI Products is now a part of Microelectronic Devices, Rockwell International.*

Rockwell

MOS/LSI TELECOMMUNICATIONS DEVICES
**APPLICATION NOTE**

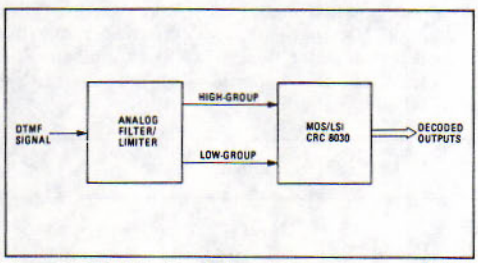
# CRC 8030 Dual Tone Multi-Frequency Receiver

## I. Introduction

The CRC 8030 is a patented* MOS/LSI Dual-Tone Multi-Frequency (DTMF) detector. Utilizing a digital filter algorithm, the CRC 8030 provides a low-cost and high-performance solution for DTMF detection. When linked with a front-end band-split filter/limiter, the CRC 8030 implements a complete DTMF receiver (figure 1). This Application Note, along with the CRC 8030 Data Sheet, provides the necessary information required to design a DTMF receiver. Inasmuch as the specifications for receivers vary with the application (e.g. central office, keyphone), the requirements for the front-end design also vary. The key element of this Application Note is a discussion of various approaches to the receiver design, plus a set of two typical test results based upon two solutions. The complete table of contents is listed below:

**Table of Contents:**

I. Introduction
II. DTMF Signaling
III. Specifications for DTMF Receivers
IV. General Description of the CRC 8030
V. Front-End Design
VI. Test Results
VII. DTMF to Dial-Pulse Conversion
VIII. Interface Capabilities of the CRC 8030

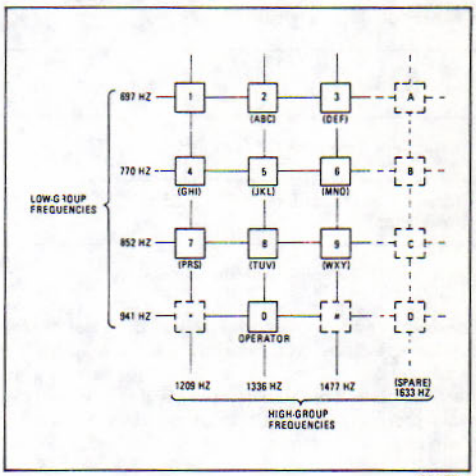



21477-9

*Figure 1. DTMF Receiver Utilizing CRC 8030*

## II. DTMF Signaling

DTMF signaling has made telephone communication faster, more efficient and more convenient through the use of a push-button pad in lieu of a rotary dial. Touch-Tone® telephone instruments or automatic dialers generate a tone pair representing the "dialed" number and send them over the lines to a receiver which detects the tones and reliably identifies the number (figure 2). This receiver can be part of a keyphone installation, a PBX or a central office. Given the differences in specifications of these three types of installations, the design requirements for the receiver will vary. The DTMF receiver must recognize the dual tones within a certain bandwidth while tolerating dial tone, noise, input amplitude variation and "twist" (i.e. amplitude differential between the two tones). In addition, the receiver has to comply with timing restrictions imposed by the DTMF generation process.




21477-8

*Figure 2. Touch Tone® Pad (Dual Tone Multi-Frequency Signaling)*

## III. Specifications for DTMF Receivers

A survey of several telephone industry OEM suppliers has led to the specifications shown in figure 3. Additional specifications such as rejection of a third tone, maximum silence bridging interval and signal-to-noise ratio, tend to vary from one manufacturer to another.

## IV. General Description of the CRC 8030

The DTMF Receiver can be implemented in two sections: The CRC 8030 (Digital Design) and a front-end (Analog Circuitry) which will interface with the telephone lines (see figure 1).



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*U.S. Patent No. 4016371

| | Keyphone | PBX Or PABX | Central Office |
|---|---|---|---|
| Input Level Dynamic Range (into 600Ω) | -10 dBm to +3 dBm | -16 dBm to +3 dBm | -26 dBm to +6 dBm |
| Twist (for valid tones) | -3 dB to 0 dB | -6 dB to 0 dB | -8 dB to +4 dB |
| Dial Tone Frequency (Present during first digit dialing) | None | 350 Hz and 440 Hz at -10 dBm | 350 Hz and 440 Hz or possibly: 480 Hz or 680 Hz at -10 dBm |
| Frequencies Used For Touch-Tone® | 697, 770, 852, 941, 1209, 1336, 1477 Hz. Unused combinations: 941 and 1209, 941 and 1477 Hz. | Same tones +1633 Hz | Same tones +1633 Hz |
| Tone Burst (Minimum) | Can vary. | 40 ms ON, 40 ms OFF | 40 ms ON, 40 ms OFF |
| Repetition Rate (Maximum) | 12 pps | 12 pps | 12 pps |
| Silence Bridging | Can vary. | 15 ms or less | 15 ms or less |
| Valid Tone Tolerance | ±1.5% | ±1.5% | ±1.5% |
| Invalid Tone Reject Limit (Maximum) | ±3.5% | ±3.5% | ±3.5% |

21577-8

*Figure 3. DTMF Receiver Specifications.*

The front-end is an essential part of the total receiver; its characteristics will certainly have a major impact on the quality of the system. This subsystem receives the tone pair from the telephone line and puts out two square wave signals corresponding to the high group and low group inputs of the CRC 8030.

The CRC 8030 accepts these inputs and converts them to binary or 2-of-8 coded outputs within as little as 22ms (figure 4). The device ignores the first few pulses to prevent any error due to transients or noise spikes present on the line. It bridges any silence or gap of 10ms or less, and otherwise resets the data registers in order to accept a new tone pair. For more details of the operation of the device, see the CRC 8030 data sheet.



| | Touch-Tone® Matrix: Binary Outputs | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1209 | | | | 1336 | | | | 1477 | | | | 1633 | | | |
| | D1 | D2 | D4 | D8 | D1 | D2 | D4 | D8 | D1 | D2 | D4 | D8 | D1 | D2 | D4 | D8 |
| 697 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 770 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 852 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 941 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

21577-9

*Figure 4. Touch Tone® Matrix — Binary Outputs*

## V. Front-End Design

The DTMF Receiver front-end provides the following functions (see figure 5).

- Couple AC signals from the line without disturbing the balance or the impedance. In some cases such as direct interface with the telephone instrument, DC power will also have to be supplied.
- Reject the dial tone while receiving the first tone pair. This function is not necessary in most keyphone applications.
- Separate the DTMF signal into tones belonging to a high group and to a low group using band-splitting filters.
- Reduces the adverse effect of "twist" or level differential between the two tones.
- Accept a wide dynamic range of the composite input signal level.
- Minimize the effect of noise.
- Produce square wave outputs at voltage levels compatible with ▬ CRC 8030 inputs.

In view of the differences in specification of the keyphone, PBX and central office (CO) DTMF receivers, the front-end design will have to be tailored to these particular applications. However, CO and PBX receivers have close characteristics and can thus use a single design. Figure 5 illustrates the front-end design for these applications.

A. Keyphone Application (Figure 6)

In this case, the front-end needs to be as simple and as economical as possible while satisifying the input signal requirements. Note in figure 6 that only a single AGC is required. The main components at the front-end design are:

1. Transformer — with a typical ratio of 1:1 $R_L$ range: 600Ω to 20 KΩ depending on the requirements.
2. Chokes — Needed only for providing power to Touch-Tone® pad. A typical value would be 150mH.
3. AGC —This circuit can be built either with discrete components or with IC's such as the LM 370. It can also be obtained in hybrid form from various manufacturers. In order to prevent any mixing products from developing, the AGC will have to be as linear as possible. Otherwise harmonics of the low-group frequencies will fall into the higher-group and detection is impeded.

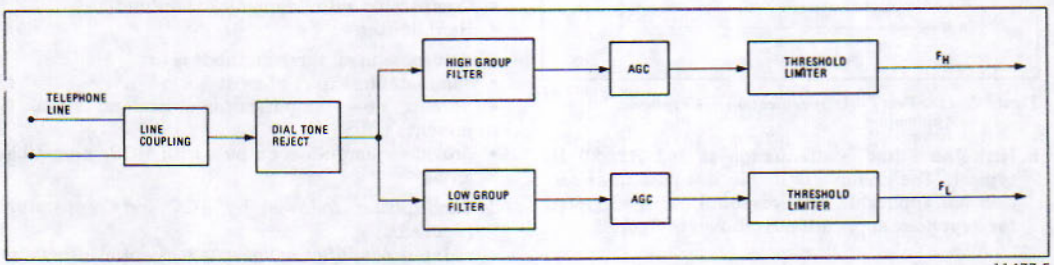



*Figure 5. Front-end Block Diagram for CO or PBX Quality Receiver*

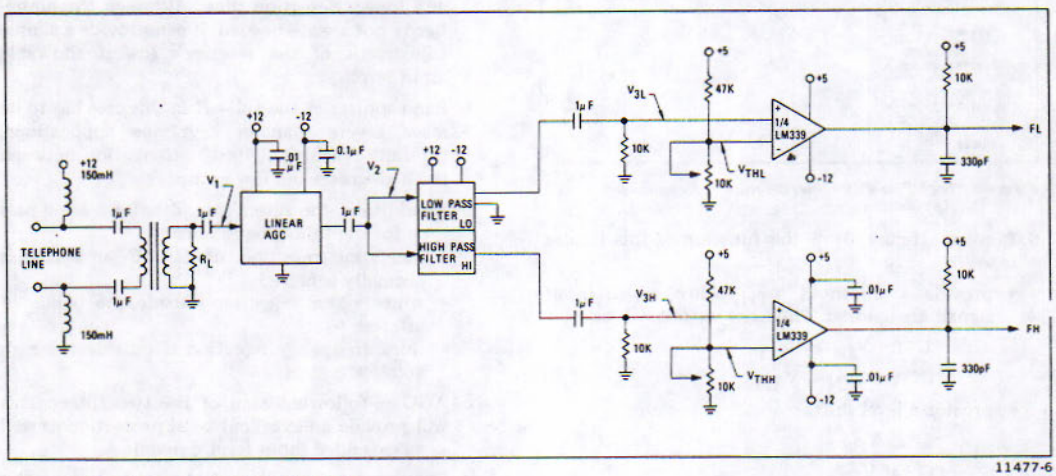



*Figure 6. Keyphone Application Schematic.*

The AGC amplifier can be omitted entirely if the input level dynamic range is limited to a few dB as it is often the case.

Input dynamic range: -13 dBm to 0 dBm (assuming a 3 dB insertion loss for the transformer)

4. Low-Pass Filter — attentuation at 1209 Hz: 30 dB typical. Such a filter can be achieved using a passive LC design or an Active RC network. Insertion loss is typically 6 dB and ripple ±1 dB. Several manufacturers have designed filters specifically for this application, although the frequency roll-off varies from one product to another. The response curve suggested for the keyphone application is shown in figure 7.

   In some keyphone systems where the 941 Hz/ 1209 Hz combination is not used, the filter requirements become somewhat less stringent.

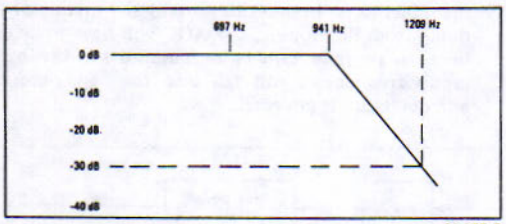



*Figure 7. Low-Pass Filter Specification — Keyphone Application*

5. High-Pass Filter — attenuation at 941 Hz: 30 dB typical. The comments in the low-pass-filter section are applicable. The response curve suggested for keyphone applications is shown in figure 8.

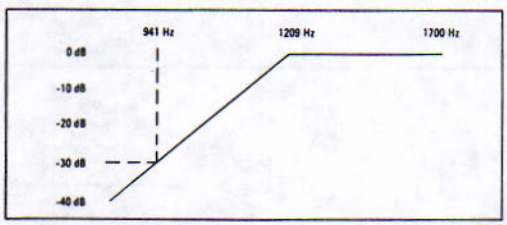



*Figure 8. High-Pass Filter Specification — Keyphone Application*

6. Limiter: (figure 6) — the function of this limiter is to:

   - provide a threshold $V_{TH}$ below which input signals are ignored. Thus, the output will be:

     "1" for $V_{IN} \geq V_{TH}$

     "O" for $V_{IN} < V_{TH}$

   - provide a level shift:

     "1" at $V_{SS}$

     "O" at $V_{GG}$

   An illustration is provided in figure 9.

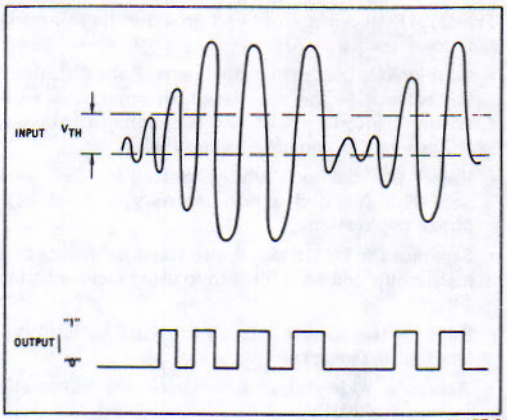



*Figure 9. Limiter Operation*

B. PBX and CO Application

In this case three different approaches can be taken for the circuitry following the band-splitter:

- AGC and comparator
- Comparator with "dynamic" threshold
- Hard limiter

The purpose in all three methods is to:

- eliminate the effect of twist
- prevent noise amplification when no signal is present
- provide square-wave outputs with MOS-compatible levels

1. Band-splitter followed by AGC and Comparator: (figure 10)
   a. Input Amplifier — linearity is essential, otherwise mixing products do develop and the CRC 8030 inputs will display a high jitter content resulting in a longer detection time. Although this amplifier is not always needed, it can provide a simple adjustment of the receiver's lowest allowable input level.
   b. Band-splitter — the roll-off in this case has to be more severe than in keyphone applications, typically reaching a 40 dB attenuation between the high-group and low-group.

      In addition, the filters should be of a band-pass type for the following reasons:
      - dial tone rejection of 50 dB or better is normally achieved
      - white noise rejection outside the bands of interest
      - third frequency rejection if outside the high and low groups.

   c. AGC — following each of the two filters. This will provide an excellent twist protection as well as an extended input level dynamic.
   d. Comparator — the threshold is set to reject noise in the absence of signal.

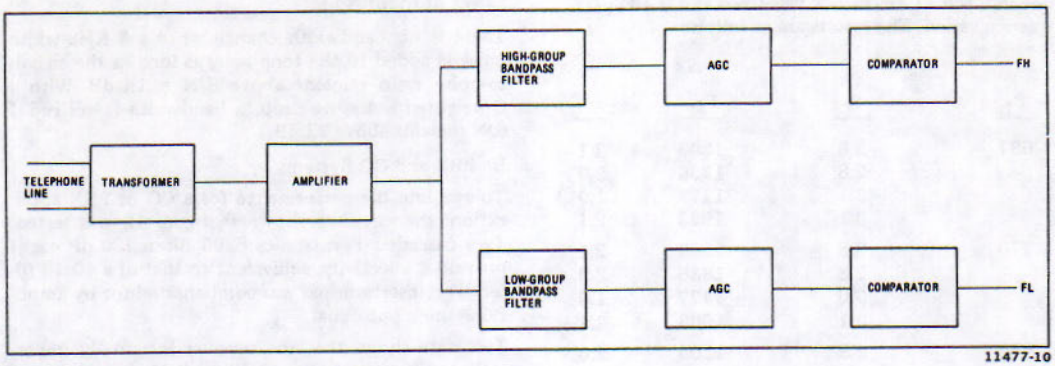



*Figure 10. PBX and CO Application Block Diagram*

2. Comparator with "dynamic" threshold: (figure 11): Instead of using an AGC circuit to adjust the signal level at the input of the comparator, the threshold level is adjusted so that signals levels within the desired range are accepted by the comparator.

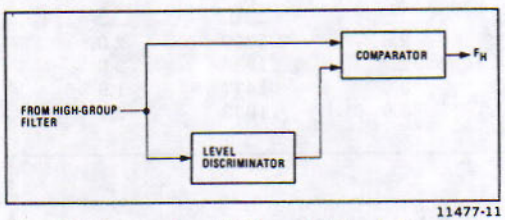



*Figure 11. Comparator with "Dynamic" Threshold*

## VI. Test Results

A. Keyphone System

Utilizing the front-end design shown in figure 6, the performance of the resulting receiver was evaluated. The high-pass and low-pass filter was implemented with a Ferritronics 8200-3 dual filter. The attenuation of this filter is 30 dB at 1209 Hz or 941 Hz.

The AGC used has a 0 dBm output level. Thus $V_2 \simeq 2.1$ VPP (measurements conducted with a single tone). Following the Ferritronics 8200-3 dual filter, the loss is 7 dB (4 dB insertion loss and 3 dB loss due to the separation of the tone pair), and $V_{3L} = V_{3H} \simeq 1$ VPP.

The threshold of each comparator will then be set at a compatible level. This level needs to be higher than the line noise, yet low enough to allow separation between the high and low groups. Typically, it is adjusted so that the cut-off frequencies are:

1040 Hz for the low group
1080 Hz for the high group
} with 1 VPP single tone input.

The result is: $V_{THL} \simeq V_{THH} \simeq 100$ mV

Testing was conducted using a DTMF synthesizer (TS-2000) manufactured by Tone Commander Systems, Inc. The criteria used in accepting a detected tone pair are:

1. The strobe pulse (STL) has to be present when detecting 10 consecutive 40 ms tone bursts.

2. The valid tone bandwidth has to be a minimum of ± 1.5%.

3. The input level dynamic range spans -10 dBm to +3 dBm (both tones having the same amplitude).

First, the $F_H$ frequency was fixed and the $F_L$ frequency varied. The results are as follows:

| $F_H$ | -% | $F_L$(Hz) | +% |
|---|---|---|---|
| 1209 Hz | 2.1 | 697 | 1.6 |
| | 2.3 | 770 | 1.7 |
| | 2.6 | 852 | 1.8 |
| | 2.7 | 941 | 1.5 |
| 1336 Hz | 2.4 | 697 | 1.9 |
| | 3.0 | 770 | 1.9 |
| | 2.8 | 852 | 2.0 |
| | 3.0 | 941 | 2.0 |
| 1477 Hz | 2.4 | 697 | 2.0 |
| | 2.7 | 770 | 2.1 |
| | 2.6 | 852 | 1.9 |
| | 3.2 | 941 | 1.9 |
| 1633 Hz | 2.4 | 697 | 1.7 |
| | 2.9 | 770 | 2.2 |
| | 2.9 | 852 | 2.0 |
| | 3.1 | 941 | 1.6 |

Second, the $F_L$ frequency was fixed and the $F_H$ frequency varied. The results are as follows:

| $F_L$ | -% | $F_H$ | +% |
|---|---|---|---|
| 697 | 2.6 | 1209 | 2.1 |
| | 2.8 | 1336 | 2.0 |
| | 3.1 | 1477 | 1.9 |
| | 3.1 | 1633 | 2.1 |
| 770 | 2.8 | 1209 | 2.1 |
| | 2.8 | 1336 | 2.0 |
| | 3.0 | 1477 | 1.9 |
| | 3.1 | 1633 | 2.1 |
| 852 | 2.8 | 1209 | 2.0 |
| | 2.6 | 1336 | 1.9 |
| | 3.0 | 1477 | 1.9 |
| | 3.1 | 1633 | 2.0 |
| 941 | 2.6 | 1209 | 1.7 |
| | 2.2 | 1336 | 1.6 |
| | 2.7 | 1477 | 1.6 |
| | 2.8 | 1633 | 1.7 |

Effect of Twist:

Twist causes the tone with the higher amplitude to be accepted with a slightly wider bandwidth, whereas the tone with the lower amplitude will be seeing a narrower bandwidth. Up to a 4 dB differential can be sustained without any drop in performance.

Effect of Input Noise:

There is no bandwidth change when a 3 KHz white noise is added to the tone pair, as long as the signal-to-noise ratio remains above S/N = 18 dB. With a C-weighted noise, no drop in bandwidth is noticed if S/N remains above 22 dB.

B. PBX and CO Systems

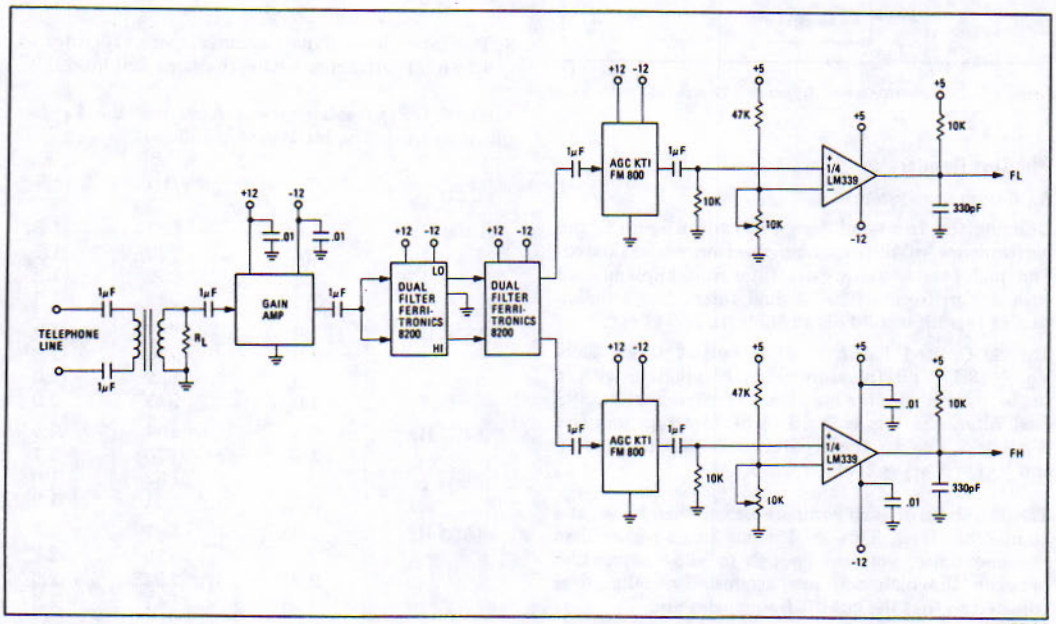
To evaluate the performance for a CO or PBX application, the circuitry shown in figure 12 was tested. Two cascaded Ferritronics 8200 filters (20 dB each) provide a selectivity equivalent to that of a 40 dB filter. The insertion loss was compensated for by amplifying the input signal.

Test data shows that the receiver is actually impervious to twist within the +4 dB to -8 dB specifications. It can accommodate an input signal with a dynamic range of more than 32 dB.

Bandwidth Data:

| -% | $F_L$ | +% |
|---|---|---|
| 2.8 | 697 | 1.8 |
| 2.9 | 770 | 1.9 |
| 2.9 | 852 | 1.9 |
| 3.0 | 941 | 1.8 |

| -% | $F_H$ | +% |
|---|---|---|
| 2.8 | 1209 | 2.0 |
| 2.7 | 1336 | 2.0 |
| 3.0 | 1477 | 1.9 |
| 3.0 | 1633 | 2.7 |




11477-12

*Figure 12. PBX and CO Application.*

### Dial Tone Effect:

The bandwidth figures are not altered when dial tone is added to the tone pair. The measurements were made with a dial tone of 440 Hz and a level as high as 16 dB over the composite DTMF signal.

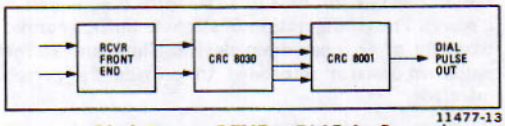
### Noise Effect:

When white noise (limited to a 3 KHz bandwidth is added to the tone pair, there is no significant change in tone detection bandwidth if the signal-to-noise ratio stays above 20 dB. At S/N = 18 dB, the 1.5% minimum bandwidth specification is still met.

In case of a C-weighted white noise, valid tone detection bandwidth remained the same with S/N = 24 dB. It drops to a minimum of 1.5% with S/N = 18 dB.

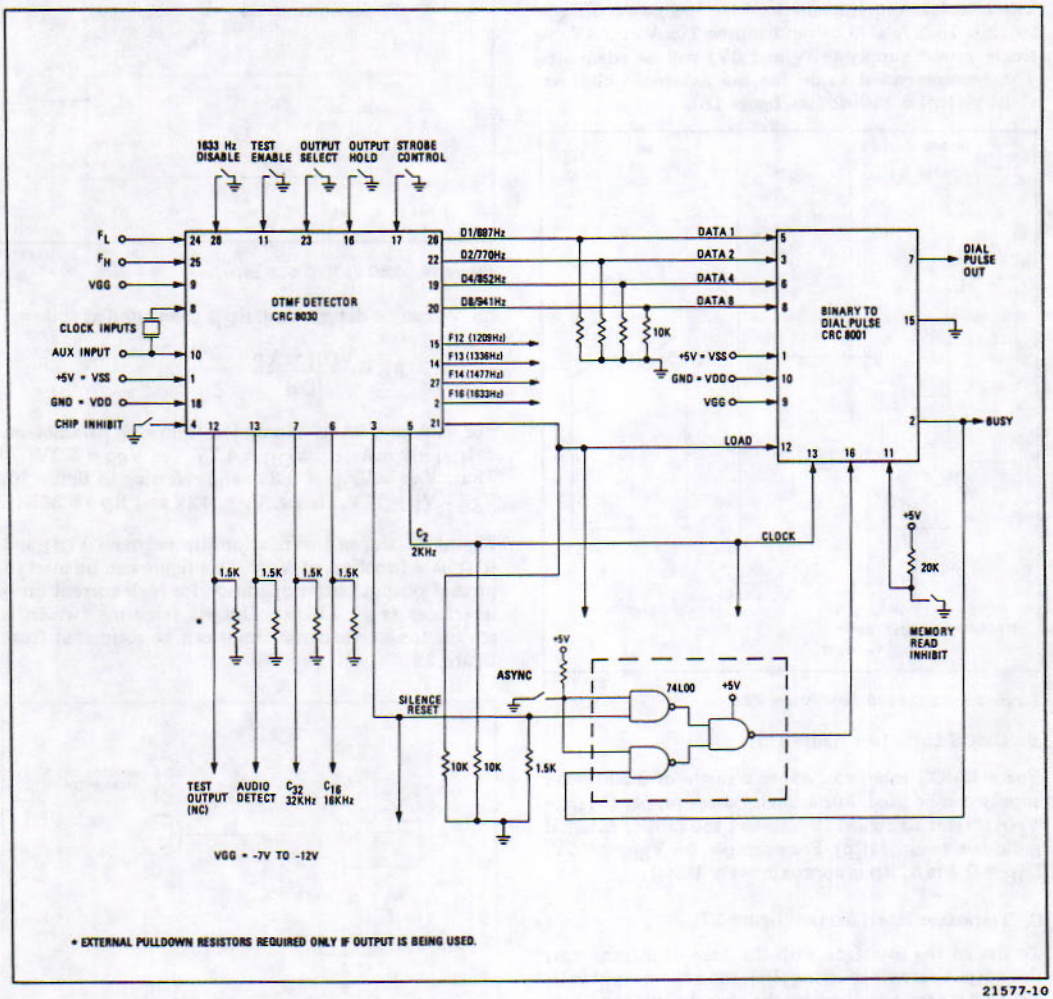
## VII. DTMF to Dial Pulse Conversion

A DTMF to dial pulse converter can be easily implemented with the CRC 8030 and the CRC 8001 — a Binary to Dial Pulse Dialer. A block diagram of the function is shown in figure 13 and a wiring diagram is shown in figure 14. The wiring diagram includes manual switches which can be used to operate the various features. Refer to the CRC 8000, 8001 and the CRC 8030 data sheets for performance details.




11477-13

*Figure 13. Block Diagram DTMF to Dial Pulse Conversion*




21577-10

*Figure 14. DTMF to Dial Pulse Conversion.*

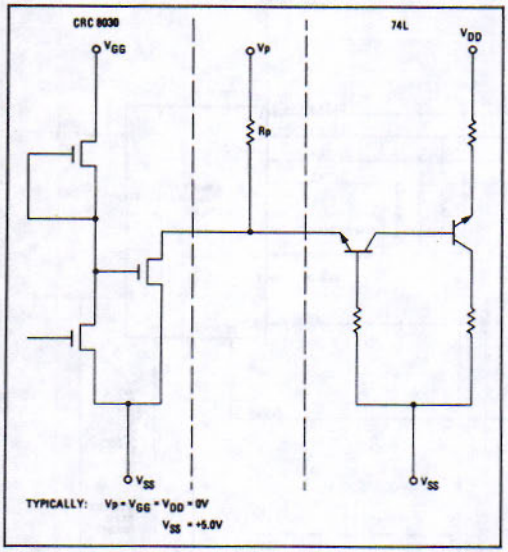
## VIII. Interface Capabilities of the CRC 8030

All control inputs of the CRC 8030 are MOS compatible. When not in use, they can be left floating without any harm to the chip. When a function is desired, the proper input is taken to a logic "0"; otherwise, a logic "1" is implied when the input is left floating.

The output buffers can drive Low Power TTL, MOS, CMOS logic or the base of a transistor (i.e., in case of a relay). The configuration of all these buffers consists basically of an open-drain device. Thus, an external pulldown resistor is needed to provide the correct interface.

A. Low Power TTL Drive (see figure 15):

The interface requirement to drive low power TTL is to sink 180$\mu$A at 0.3V and source 10$\mu$A at 2.4V. A single power supply (+5V and 0V) will be adequate. The recommended value for the external pulldown resistor (Rp) is 1500Ω (see figure 18).




21577-11

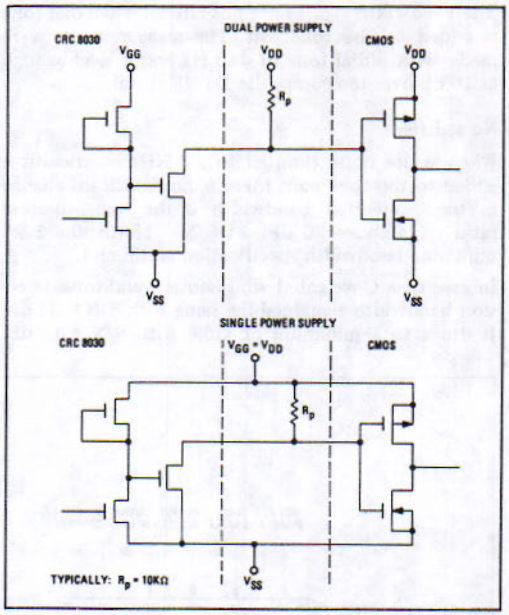
*Figure 15. CRC 8030/Low Power TTL.*

B. CMOS Drive (see figure 16):

For a CMOS interface, either a single or dual power supply can be used. For a single power supply ($V_{GG}$ = $V_{DD}$), refer to figure 19 to select the proper external pulldown resistor (Rp). For example, for $V_{SS}$ = +5.0V, $I_{OH}$ = 0.4 mA, Rp is approximately 10KΩ.

C. Transistor Interface (see figure 17):

To design the interface with the base of a transistor, the output current sourcing ($I_{OH}$) and the output voltage ($V_{OH}$) are specified by the user. In this case, two power supplies are required: Typically $V_{SS}$ = +5V, $V_{DD}$ = 0V, and $V_{GG}$ = Vp. From figure 20, the value




21477-2

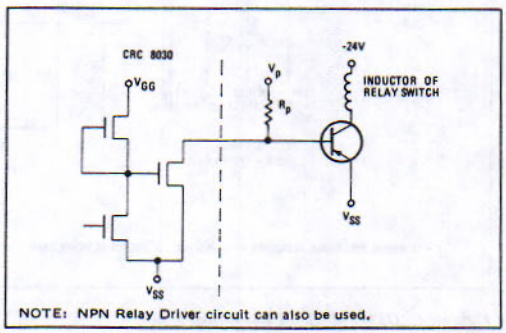
*Figure 16. CRC 8030/CMOS Interface*

for Vp can be determined. Rp is calculated as follows:

$$Rp = \frac{V_{OH} - Vp}{I_{OH}}$$

For example, let us choose the following parameters:
$I_{OH}$ = 2 mA $V_{OH}$ = 4.7V $V_{SS}$ = 5.0V
Thus, $V_{SS} - V_{OH}$ = 0.3V, and referring to figure 20, $V_{SS} - Vp$ = 17V. Hence, Vp = -12V and Rp = 8.35KΩ.

Figure 21 shows the relationship between $V_{OH}$ and $I_{OH}$ as a function of $V_{SS}$. This figure can be used to predict output buffer operation for high current drive interfaces (e.g., LED's). Output fall time (which is always longer than rise time) can be estimated from figure 22.




21577-12

*Figure 17. CRC 8030/Transistor Interface.*

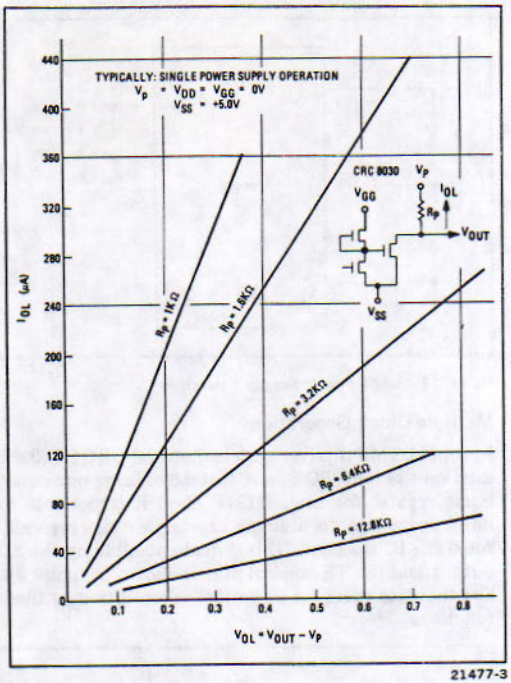



*Figure 18. LPTTL Interface: $I_{OL}$ vs. $V_{OL}$*

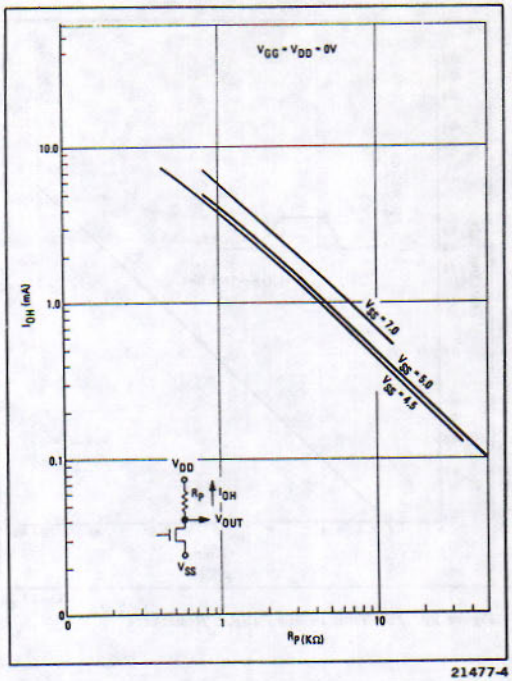



*Figure 19. CMOS Interface: $I_{OH}$ vs. $R_P$*

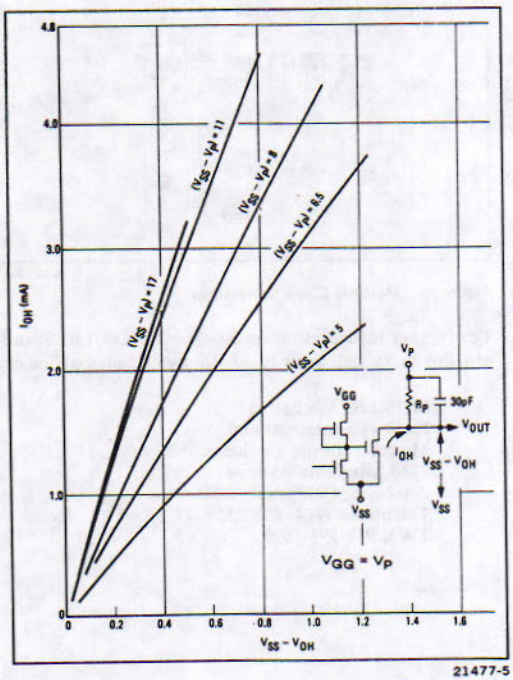



*Figure 20. Transistor Interface: $I_{OH}$ vs. $(V_{SS} - V_{OH})$*

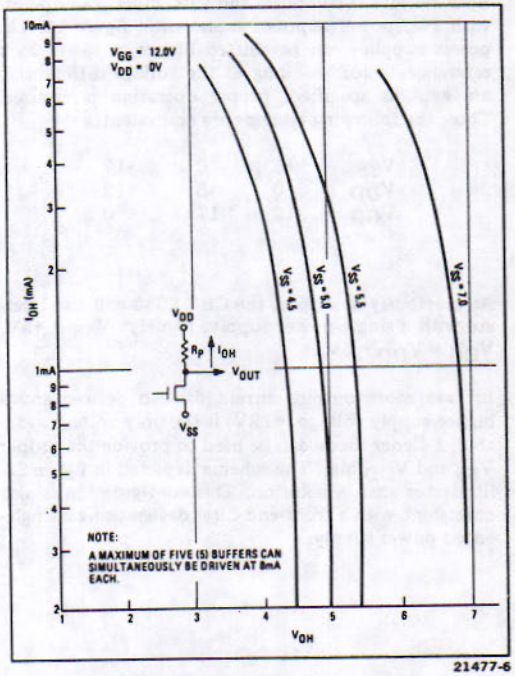
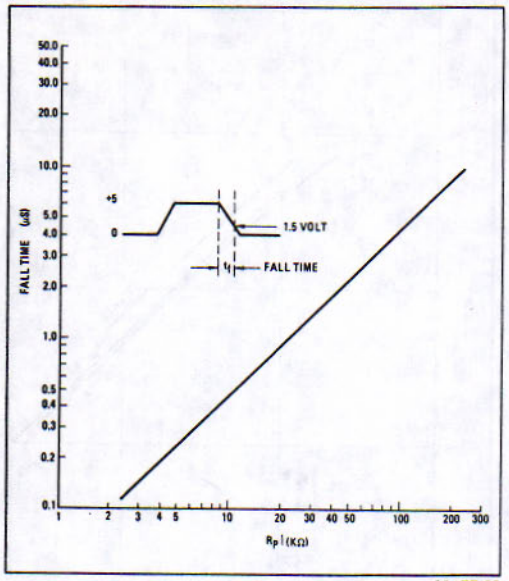



*Figure 21. Output Current Capability*




11477-22

*Figure 22. Fall Time versus Pull Up Resistance*

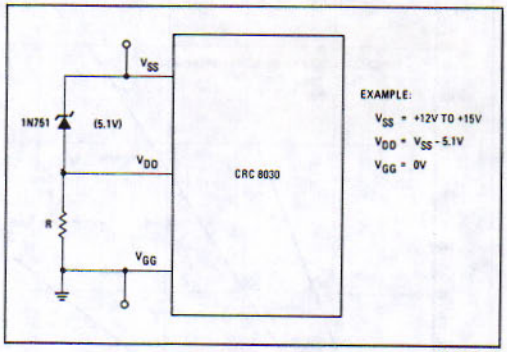
**Power Supply Considerations:**

Both devices (CRC 8030 and CRC 8001) can operate with two power supplies as shown in figure 14. The power supplies can be shifted higher or lower by a reference factor. As long as the voltage differentials are kept as specified, proper operation is ensured. Thus, the following systems are equivalent:

| | | | |
|---|---|---|---|
| $V_{SS}$ | +5 | 0 | +17 |
| $V_{DD}$ | 0 | -5 | +12 |
| $V_{GG}$ | -12 | -17 | 0 |

As previously described, the CRC 8030 will also operate with a single power supply, namely: $V_{SS}$ = +5V, $V_{GG} = V_{DD} = 0V$.

In case more output current drive is desired and a higher supply voltage (+12V) is the only voltage available, a Zener diode can be used to provide the proper $V_{SS}$ and $V_{DD}$ bias. The scheme depicted in figure 23, illustrates such a solution. This configuration is also consistent with a front-end filter design using a single-edged power supply.

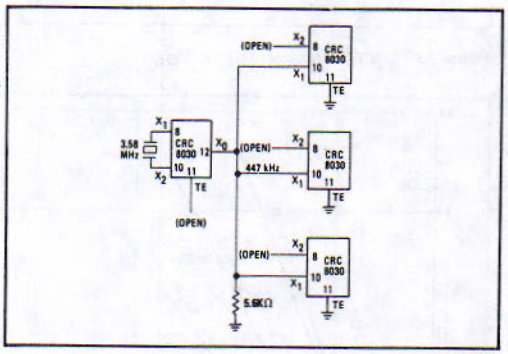



21577-13

*Figure 23. Single Power Supply Operation*

**Multiple Clock Generation**

In some DTMF receiver systems, several CRC 8030 are used on the same PC Board. Instead of using one color-burst crystal for each DTMF chip, it is possible to limit the usage to a single crystal for all (typically four) the IC's present. This is made possible by the X0 output and the TE control pins as shown in figure 24. See the data sheet for a complete description of these functions.




90877-11

*Figure 24. Multiple Clock Generation*

For further information on Rockwell MOS/LSI Standard Products, call your local Rockwell Sales office or:

MOS/LSI Marketing
Rockwell International
Microelectronic Devices
3310 Miraloma Avenue
Anaheim, California 92803
Telephone (714) 632-2558
TWX 910-591-1698

*NOTE: Collins MOS/LSI Products is now a part of Microelectronic Devices, Rockwell International.*

Rockwell

# MOS/LSI TELECOMMUNICATIONS DEVICES

## TECHNICAL BULLETIN

## CRC 8030 Front-End Components

The purpose of this document is to list some of the commercially available components that can be utilized to design the front-end filter/limiter for the CRC 8030. The requirements for this front-end are described in the CRC 8030 Application Note. Not all of the components listed meet the suggested specifications of this Application Note, but they may provide satisfactory performance in particular applications.

1. **Input Transformer:** 600 ohm 1:1

| | |
|---|---|
| PICO | A1160 |
| Bourns | 4212-0011 |
| Aladdin | 317-0330 |

2. **Chokes** (needed only for providing power to Touch-Tone® pad).

| | |
|---|---|
| Torotel | 13086 150 mH |

3. **Hybrid Integrated Filter/Limiter**

The following product is designed specifically to meet CRC 8030 front-end filter/limiter requirements. These hybrids provide all of the functions shown in figure 5 of the CRC 8030 Application Note (except line coupling).

| Mfr | Ident. | Type |
|---|---|---|
| North Microsystems | 3040 | Low-Group |
| North Microsystems | 3041 | High-Group |

4. **Low-Group Filters**

| Mfr | Ident. | Type |
|---|---|---|
| Amperex | AFM710 | Active, Band Pass |
| Amperex | AFM724 | Active, Low Pass |
| BEI | FM953 | Active, Band Pass |
| Cermetek | CH-1295 | Active, Band Pass |

5. **High-Group Filters**

| Mfr | Ident. | Type |
|---|---|---|
| Amperex | AFM711 | Active, Band Pass |
| Amperex | AFM725 | Active, High Pass |
| BEI | FM954 | Active, Band Pass |
| Cermetek | CH-1296 | Active, Band Pass |

6. **Dial Tone Reject Filter:**

| Mfr | Ident. | Type | Impedance |
|---|---|---|---|
| BEI | FM853 | Active, Single Notch | $Z_{in}$ High, $Z_{out}$ Low |
| National | AF-102 | Active, Single Notch | $Z_{in}$ High, $Z_{out}$ Low |

7. **AGC Amplifier**

| Mfr | Ident. |
|---|---|
| BEI | FM800 |
| National | AF-104 |

8. **Comparator:**

LM 339 or equivalent.

9. **Squaring Translator:** (contains AGC and limiting circuitry).

| Mfr | Ident. |
|---|---|
| BEI | FM900 |

10. **Crystal:**

3.57954 MHz
Tolerance: +0.005% at 25°C. Parallel resonant.
HC-33/V type holder.
18 pF load capacitance.
Mfr: M-tron, Electrodynamics, CTS.

®Registered trademark of AT&T

REV NOV 77

# CRC 8030 Front-End Suppliers' Addresses

1. Amperex Electronics Corp.
   (A North American Philips Company)
   P.O. Box 98
   Slatersville, RI 02876
   (401) 762-3800
   Lee Hermanson

2. B.E.I. Microelectronics (formerly KTI)
   1101 McAlmont Street
   Little Rock, Arkansas 72203
   (501) 372-7351
   Mike Hollingsworth

3. Cermetek
   660 National Avenue
   Mountain View, California 94043
   (415) 969-9433
   Jim Cremer

4. CTS Microelectronics, Inc.
   1201 Cumberland Avenue
   West Lafayette, Indiana 47906
   (317) 463-2565
   Brian R. Hess

5. National Semiconductor Corporation
   2900 Semiconductor Drive
   Santa Clara, California 95051
   (408) 732-5000

6. North Microsystems
   Division of North Electric Company
   700 Hillsboro Plaza
   Deerfield Beach, Florida 33441
   (305) 421-8450
   David Speed





Printed in USA/Nov. 1977

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APRIL 1979

PART NUMBER
R8040

Rockwell

# MOS/LSI TELECOMMUNICATIONS DEVICES
## DATA SHEET

# T-1 TRI-PORT MEMORY

## OVERVIEW

The Tri-Port Memory circuit is designed to function as an assembly point and temporary storage area for 8-bit T-1 data. It provides 64 8-bit locations of on-chip random access memory which can be accessed via external addresses or internal sequential addressing.

### TRI-PORT MEMORY OPERATION

The Tri-Port Memory device accepts 8-bit parallel input data on lines A through H. This data is stored in an internal memory location that is selected by either random address lines R01 through R32 or by the device's Sequential Address Counter. Write Select signal WSEL determines the source of the address; in the logic 0 state, WSEL selects the random address, in the logic 1 state, WSEL selects the internal sequential address.

The state of Write Enable signal $\overline{WE}$ determines whether or not the data on lines A through H will be written into memory. Data will only be written into memory when $\overline{WE}$ goes low (to a logic 0 state) and the address inputs have stabilized.

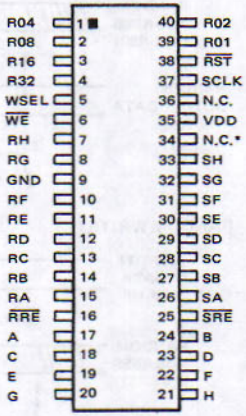
The on-chip, six-bit Sequential Address Counter is a binary counter that increments on each positive transition of Sequential Clock (SCLK). When the Counter attains binary 111111, the next positive transition on SCLK will clear it to binary 000000. The Counter will also be cleared unconditionally if Reset signal $\overline{RST}$ has been set to logic 0 when the positive transition of SCLK occurs.

The Sequential Read Enable signal, $\overline{SRE}$, enables sequentially-addressed read operations. If $\overline{SRE}$ is logic 0, the sequential accessed data outputs (SA through SH) will become valid within 430 ns after the next positive transition on SCLK. If $\overline{SRE}$ is logic 1, and 350 ns have elapsed since the positive transition of SCLK, the sequential accessed data outputs will become valid 80 ns after the negative transition of $\overline{SRE}$. The Sequential Read Data will cease to be valid within 100 ns after the positive transition of $\overline{SRE}$, or within 340 ns after the negative transition of $\overline{WE}$ (in the case of a same-location read/write cycle), or within 430 ns after the next positive transition of SCLK.

The Random Read Enable signal, $\overline{RRE}$, enables random-accessed read operations. If $\overline{RRE}$ is logic 0, the random accessed data outputs (RA through RH) will become valid within 380 ns after the random address lines have stabilized. If $\overline{RRE}$ is logic 1, and 300 ns have elapsed since the random address lines have stabilized, the random accessed data outputs will become valid 80 ns after the negative transition of $\overline{RRE}$. The random accessed data outputs cease to be valid after a positive transition of $\overline{RRE}$, or within 340 ns after the negative transition of $\overline{WE}$ (in the case of a same-location read/write cycle) or within 380 ns after the random address input lines change.

## FEATURES

- 64 x 8 bit static memory
- Single +5V supply
- Two totally independent read ports
- Multiple Read access time <430 ns (worst case)
- Selectable random- or sequential-address Write operation
- On-chip sequential address counter
- Tri-state drivers, for chip-selectable bus operation
- 40-pin plastic dual in-line package



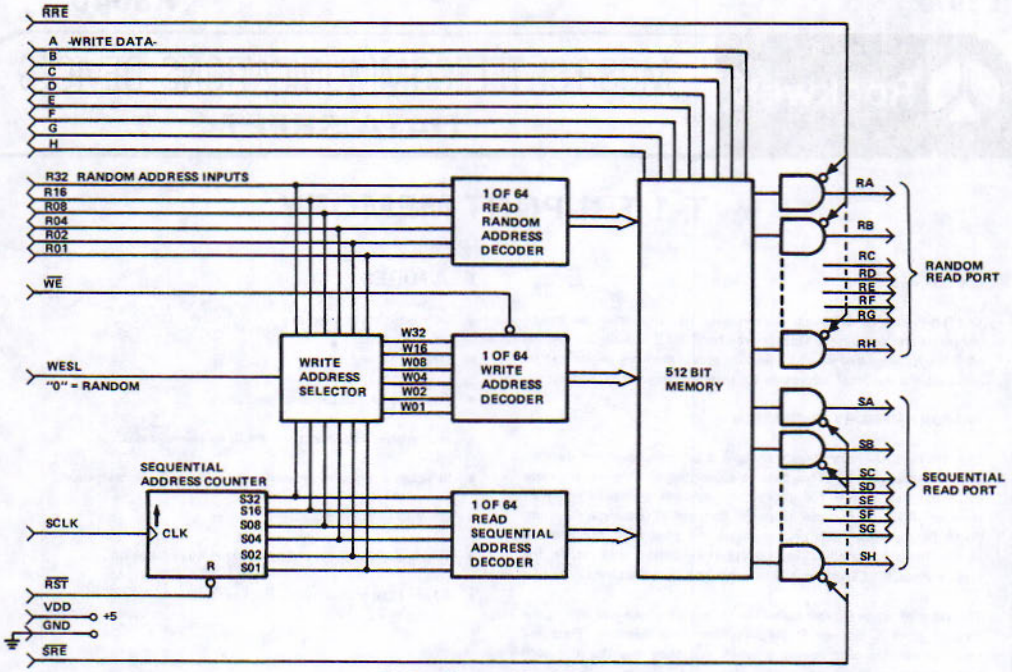

*PIN 34 HAS AN OUTPUT SIGNAL APPLICABLE ONLY TO ROCKWELL TESTING. MAKE NO CONNECTION TO THIS PIN.

**Pin Configuration**



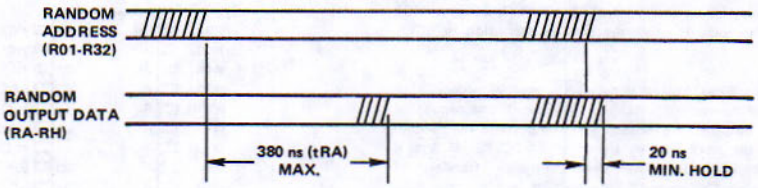


Specifications subject to change without notice

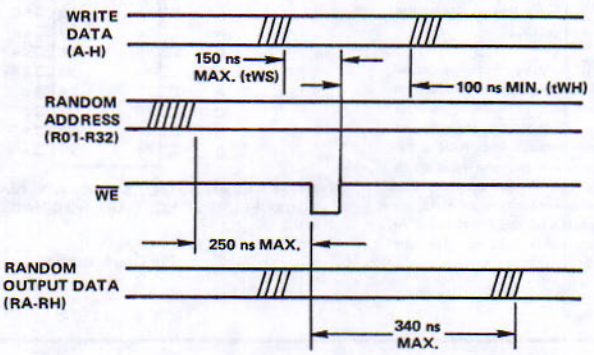



Tri-Port Memory Block Diagram

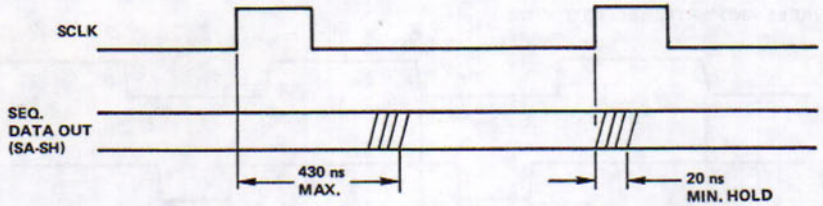
RANDOM READ



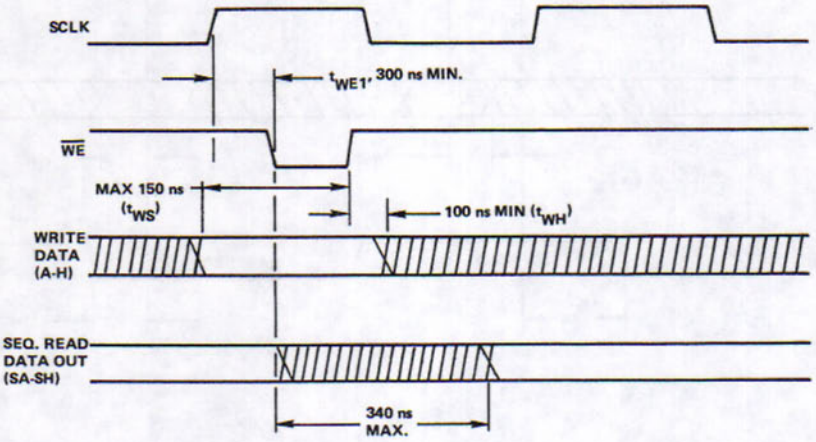

RANDOM WRITE



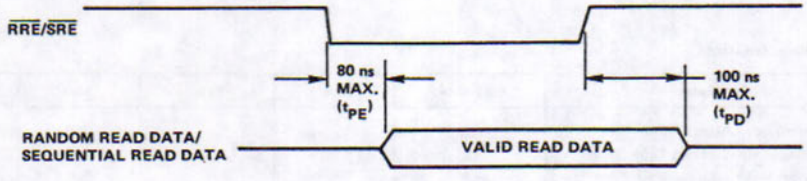
## SEQUENTIAL READ



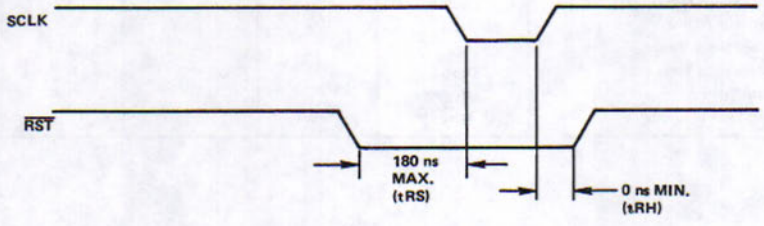

## SEQUENTIAL WRITE



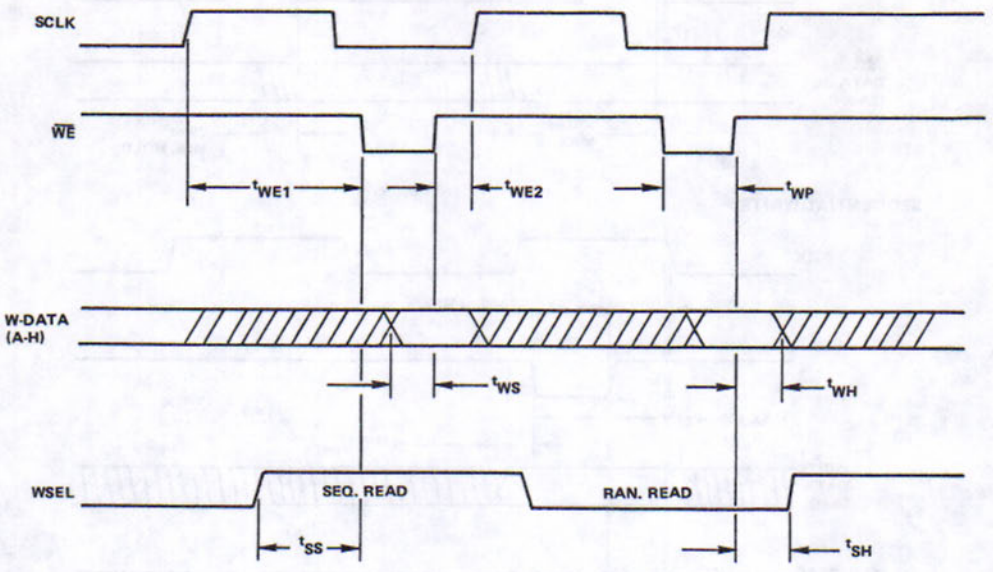

## READ PORT ENABLES ($t_{PE}/t_{PD}$)




## SEQUENTIAL COUNTER RESET



## WRITE ENABLE AND WRITE SELECT TIMING




### Timing Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Random Read Access Time | $t_{RA}$ | | | 380 | ns |
| Sequential Read Access Time | $t_{SA}$ | | | 430 | ns |
| Random Read Address Setup Time | $t_{AS}$ | | | 380 | ns |
| Read Port Disable (to Hi Z) | $t_{PD}$ | | | 100 | ns |
| Read Port Enable | $t_{PE}$ | | | 80 | ns |
| $\overline{WE}$ Pulse Width | $t_{WP}$ | 170 | 300 | | ns |
| $\overline{WE}$ Pulse Delay | $t_{WE1}$ | 300 | | | ns |
| $\overline{WE}$ Pulse Setup | $t_{WE2}$ | | | 0 | ns |
| SCLK Pulse Width | $t_{SP}$ | 220 | 325 | | ns |
| SCLK Frequency | f | | 1.544 | | MHz |
| Write Data Setup Time | $t_{WS}$ | | | 150 | ns |
| Write Data Hold Time | $t_{WH}$ | 100 | | | ns |
| Write Select Setup Time | $t_{SS}$ | | | 280 | ns |
| Write Select Hold Time | $t_{SH}$ | 0 | | | ns |
| $\overline{RST}$ Setup Time | $t_{RS}$ | | | 180 | ns |
| $\overline{RST}$ Hold Time | $t_{RH}$ | 0 | | | ns |

## SPECIFICATIONS

### Maximum Ratings

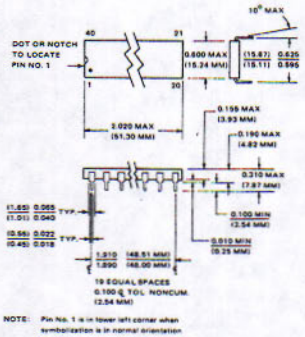
| Rating | Symbol | Voltage | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | +4.5 to +5.5 | V |
| Operating Temperature Range | $T_{OP}$ | 0 to 70 | $^{o}C$ |
| Storage Temperature Range | $T_{STG}$ | -55 to +150 | $^{o}C$ |

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

### Electrical Characteristics

($V_{DD}$ = +5V ±10%, $V_{SS}$ = 0V, $T_A$ = 25°C)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Logic "1" Voltage | $V_{IH}$ | 2.0 | | V |
| Input Logic "0" Voltage | $V_{IL}$ | | 0.8 | V |
| Output Logic "1" Voltage | $V_{OH}$ | 2.4 | | V |
| Output Logic "0" Voltage | $V_{OL}$ | | 0.4 | V |
| Output Source Current | $I_{OH}$ | -100 | | µA |
| Output Sink Current | $I_{OL}$ | 400 | | µA |
| Input Capacitance | $C_I$ | | 5 | pF |
| Output Capacitance | $C_O$ | | 25 | pF |
| Power Dissipation (at 25°C) | $P_{DSS}$ | | 300 | mW |




**Packaging Diagram**

**DOCUMENT NO. R8050D**
**APRIL 1979**

**PART NUMBER**
**R8050**

Rockwell

# MOS/LSI TELECOMMUNICATIONS DEVICES
## DATA SHEET

# T-1 SERIAL TRANSMITTER

## GENERAL DESCRIPTION

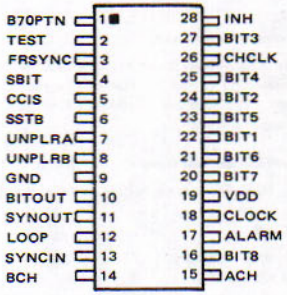
The Rockwell T-1 Serial Transmitter formats data to be serially transmitted according to T-1 D2 or T-1 D3 specifications, inserting framing and signalling bits along with 24 channels of 8-bit channel data. The T-1 Serial Transmitter also provides for alarm reporting via the Bit 2 inhibit method or, with minimal external logic, via the multiframe alignment signal ($F_S$) modification.

Figure 1 is a functional block diagram of the T-1 Serial Transmitter. The Mod 193 counter is driven by the clock at 1.544 MHz and is either synchronized to the driving system by input signal SYNCIN or provides synchronization via output signal SYNOUT. Input signal FRSYNC applies synchronization to a Mod 12 counter, which identifies the frame of the 12-frame multiframe being processed.

The input data register latches data during each bit period, when the 8th bit of a channel sample is being transmitted. The data selector outputs the proper sequence of bits, as controlled by a bit count and frame count.

The zero channel monitor function causes Bit 8 or Bit 7 (as selected by B7OPTN) to be transmitted as a "one" if the channel data sample is all "zeros" for any frame except signalling frame (Frame 6 or 12). Input INH provides a means to inhibit the zero channel monitor function.

Two types of transmit formats are provided, a binary output and a paired unipolar output. The unipolar pair provides a means to externally create a single bipolar output with minimal logic.




**Pin Configuration**

## FEATURES

- Single 5V supply, low power Schottky TTL compatible
- Accepts 8 bits of parallel data as input
- Generates output as 193 bit serial data stream in T-1, D2 or T-1, D3 data format
- Provides a channel and frame timing signal.
- Provides alternate control for alarm reporting and signalling
- Provides automatic bit insertion for all zero channel samples.

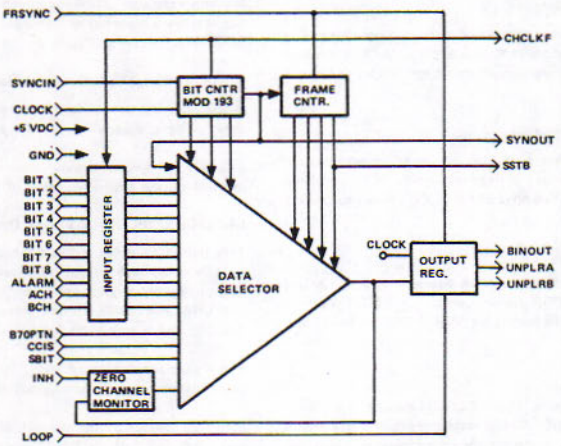



**Figure 1. T-1 Serial Transmitter**



Specifications subject to change without notice

## T-1 Transmitter Inputs

Any input ≤0.8V = logic 0, low. Any input ≥2.0V = logic 1, high. The transition from a low level to a high level is called a rising edge, while the converse is defined as a falling edge.

**FRSYNC: Frame Synchronization**

Frame sync allows the user to force the frame counter to the frame count of 1. (The first frame of a possible 12.) When high, FRSYNC directly sets the frame count to be frame 1. If FRSYNC does not return to zero before the rising edge of CLOCK, BINOUT, UNPLRA are transmitted high and UNPLRB is transmitted low. Refer to Figure 6 and Figure 7.

**SYNCIN: Synchronization Input**

Provides a means to directly reset the Mod 193 bit counter to a bit position corresponding to the first bit of channel 1. The high level causes the reset. The first bit of channel 1 will be transmitted following the release of SYNCIN.

**TEST: Rockwell Device Test Input**

Used only for Rockwell device testing. **Keep this input grounded.**

**CLOCK: T-1 Clock**

Maximum frequency = 1.6 MHz
Minimum pulse width = 275 ns
The T-1 bit period is bounded by the rising edges of this input.

**INH: Inhibit Zero Channel Monitor**

If INH is high, the zero channel monitor function is disabled, and Bits 7 and 8 are transmitted per corresponding inputs received. See Table 1.

For any frame except a signalling frame (Frame 6 or 12) Bit 8 or Bit 7 as selected by B7OPTN will be transmitted as a "one" if the channel input data is "zero" and INH is low.

**BITS 1-8: Parallel Channel Data Inputs**

Bit 1, the sign bit, will be serially transmitted first, followed by Bits 2 through 8. The falling edge of CHCLKF indicates input channel data has been clocked into the input register and always occurs during the transmission of the final bit (Bit 8) of each channel data sample.

**ACH: "A" Channel Highway Signalling**

ACH allows the user to transmit a one bit of signalling per channel as Bit 8 of each channel data sample in Frame 6 only. ACH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

**BCH: "B" Channel Highway Signalling**

BCH allows the user to transmit a one bit of signalling per channel as Bit 8 of each channel data sample in Frame 12 only. BCH is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

**S-BIT: Multiframe Signalling Bit**

SBIT, in conjunction with CCIS, provides an alternate way to control the multiframe signalling bit ($F_S$) transmission. The S-Bit input is transmitted as the multiframe signalling bit ($F_S$) if CCIS is held high. Refer to Table 2.

**ALARM: Local Alarm**

Used for reporting alarm conditions. If the ALARM signal is high, Bit 2 (the most-significant bit) of every channel data sample of every frame is transmitted as a zero. This is commonly called remote alarm signalling. ALARM is clocked into the input register by the falling edge of CHCLKF. Refer to Table 1 and Figure 4.

**LOOP: Loop Strap**

Provided to aid testing of user applications. When enabled to a high level, LOOP forces the unipolar outputs to transmit alternating ones and zeros, regardless of input conditions. Refer to Figure 3.

**CCIS: Common Channel Interoffice Signalling Strap**

Provides optional control for transmitting an alternate multiframe (even-numbered frames) signalling pattern via the S-Bit input. Automatically programmed S-Bit ($F_S$) transmission following Table 2 is achieved by holding CCIS at a low level.

**B7OPTN: Bit 7 Option**

Provides Bit 7 as an alternate bit position for "one" stuffing, as programmed by the zero channel monitor function. Refer to Table 1.

**VSS, VDD: Ground and Power**

VDD = +5 ±0.5 Vdc
VSS = Ground, 0 Vdc

## T-1 Transmitter Outputs

Low power TTL Schottky compatible. "1" ≥2.4 Vdc, "0" ≤0.4 Vdc, $C_L$, 25 pf.

**SSTB: 4 kHz Signalling Channel Strobe**

SSTB is the least-significant bit of the frame counter. Unless it is directly set by FRSYNC, SSTB will go high as each framing bit ($F_T$) is serially transmitted, and will return low as each multiframe alignment signal ($F_S$) is transmitted. Refer to Figure 2.

**SYNOUT: Channel Sync Output**

SYNOUT provides a means to synchronize to the internal bit counter (Mod 193). SYNOUT is high for one bit time, beginning just prior to the first data bit of a frame being serially transmitted. Refer to Figure 8.

**CHCLKF: Channel Clock False**

The falling edge of CHCLKF, occurring as Bit 8 of any channel is being serially transmitted, indicates input data has been clocked into the input register. With the exception of an extra bit period extending the low level duration at frame bit time, CHCLKF is a divide-by-eight of CLOCK. Refer to Figure 2.

**BINOUT: Serial Data Output, Binary Formatted**

BINOUT is the binary formatted serial conversion of the parallel input data. The programmed format of BINOUT follows Table 1 and 2.

BINOUT is synchronously transmitted as a high level if FRSYNC remains during the rising edge of CLOCK. Refer to Figure 6 and 7.

**UNPLRA, UNPLRB: T-1 Serial Data Unipolar Outputs**

Two paired unipolar outputs are provided for the purpose of creating a single serial data output transmission in bipolar format. The unipolar output register toggles for each "one" bit to be serially transmitted. UNPLRA and UNPLRB are transmitted as complements for "one" data bits and as low levels for "zero" data bits. See Figure 3.

The input signal loop, if high, forces the unipolar outputs to toggle every bit time, regardless of input data.

FRSYNC perturbs the current bits being transmitted by UNPLRA and UNPLRB. If FRSYNC remains high during the rising edge of CLOCK, UNPLRA will be transmitted as a high level and UNPLRB will be low. Refer to Figures 6 and 7.

### Table 1. Serial Output Data Processing for Channel Sample Data (Not $F_T$ or $F_S$)

BINOUT representing the serial data out will be a "1" if the below equations are true.

| SERIAL DATA BIT TO BE TRANSMITTED (NEXT BINOUT) | FRAME = 6 OR FRAME = 12 AND CCIS = 0 | CCIS = 1 AND ANY FRAME (2) |
|---|---|---|
| 1st | Bit 1 = 1 (1) | Bit 1 = 1 |
| 2nd | B2 = 1 (see equation below) | B2 = 1 |
| 3rd | Bit 3 = 1 | Bit 3 = 1 |
| 4th | Bit 4 = 1 | Bit 4 = 1 |
| 5th | Bit 5 = 1 | Bit 5 = 1 |
| 6th | Bit 6 = 1 | Bit 6 = 1 |
| 7th | Bit 7 or B7X = 1 | B7 = 1 |
| 8th | Bit 8 or B8X = 1 | Sig = 1 |

(1) Terms Bit 1 thru Bit 8, ACH, BCH and ALARM are the clocked data from the parallel data input register. All other terms are either complex equation terms or unstored device inputs.

(2) If CCIS = 1 the T-1 transmitter can not uniquely identify Frame 6 or Frame 12.

$B2 = BIT2 \cdot \overline{ALARM}$

$B7 = BIT7 + \overline{SIG} \cdot \overline{BIT1} \cdot \overline{B2} \cdot \overline{BIT3} \cdot \overline{BIT4} \cdot \overline{BIT5} \cdot \overline{BIT6} \cdot \overline{INH}$

$Sig = ACH \cdot FRAME = 6 + BCH \cdot FRAME = 12$

$B7X = B7OPTN \cdot \overline{BIT1} \cdot \overline{B2} \cdot \overline{BIT3} \cdot \overline{BIT4} \cdot \overline{BIT5} \cdot \overline{BIT6} \cdot \overline{INH} \cdot \overline{BIT8}$

$B8X = \overline{B7OPTN} \cdot \overline{BIT1} \cdot \overline{B2} \cdot \overline{BIT3} \cdot \overline{BIT4} \cdot \overline{BIT5} \cdot \overline{BIT6} \cdot \overline{INH} \cdot \overline{BIT7}$

### Table 2. Serial Output Data Processing for Framing Bits $F_T$, $F_S$

| CURRENT FRAME NUMBER | REPRESENTED BIT | BINOUT BECOMES A "1" IF: (UNLESS STATED OTHERWISE) |
|---|---|---|
| 1 | $F_S$ | SBIT and CCIS = 1 |
| 2 | $F_T$ | "0" |
| 3 | $F_S$ | SBIT and CCIS = 1 |
| 4 | $F_T$ | "1" |
| 5 | $F_S$ | SBIT = 1 or CCIS = 0 |
| 6 | $F_T$ | "0" |
| 7 | $F_S$ | SBIT = 1 or CCIS = 0 |
| 8 | $F_T$ | "1" |
| 9 | $F_S$ | SBIT = 1 or CCIS = 0 |
| 10 | $F_T$ | "0" |
| 11 | $F_S$ | SBIT and CCIS = 1 |
| 12 | $F_T$ | "1" |

$F_T$ = Framing Bit

$F_S$ = Multiframing Alignment Bit

NOTE: $F_T$ Bit insertion is automatic and no optional control is provided.

Table 3. Input Timing

| | | MIN | MAX | UNITS |
|---|---|---|---|---|
| $t_{1S}$ | Buffered Data Setup Time | 450 | | ns |
| $t_{1H}$ | Buffered Data Hold Time | 0 | | ns |
| $t_{2S}$ | Control Input Setup Time | 400 | | ns |
| $t_{2H}$ | Control Input Hold Time | 20 | | ns |
| $t_{3S}$ | Asynchronous Control Input Setup Time | 350 | | ns |
| $t_{3H}$ | Asynchronous Control Input Hold Time | 20 | | ns |
| $t_{4S}$ | SYNCIN Setup Time | 200 | | ns |
| $t_{4H}$ | SYNCIN Hold Time | 20 | | ns |
| | SYNCIN Pulse Width | 100 | | ns |
| $t_{5S}$ | Frame Sync Setup Time (Return to Zero) | 250 | | ns |
| $t_{5H}$ | Frame Sync Hold Time (Return to Zero) | 20 | | ns |
| | Frame Sync Pulse Width | 200 | | ns |
| $t_{5S}$ | Frame Sync Setup Time (Non-Return to Zero) | 525 | | ns |
| $t_{5H}$ | Frame Sync Hold Time (Non-Return to Zero) | 20 | | ns |

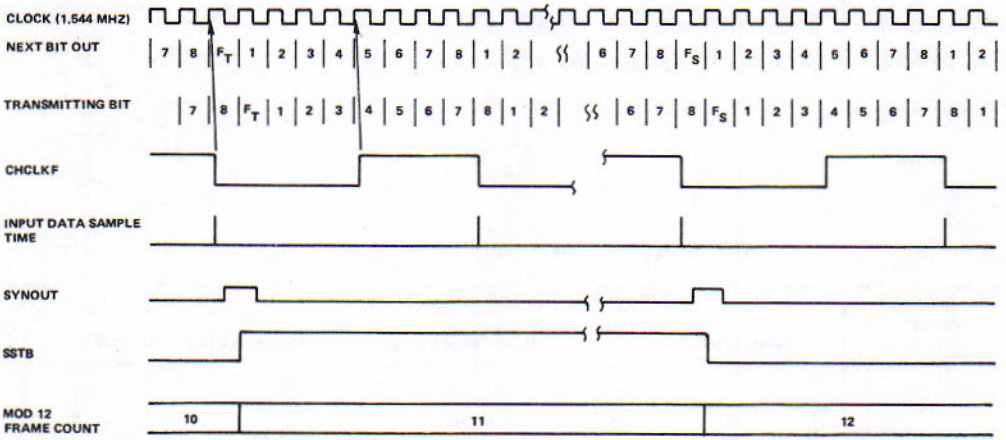



Figure 2. T-1 Transmitter Output Signal Relationship

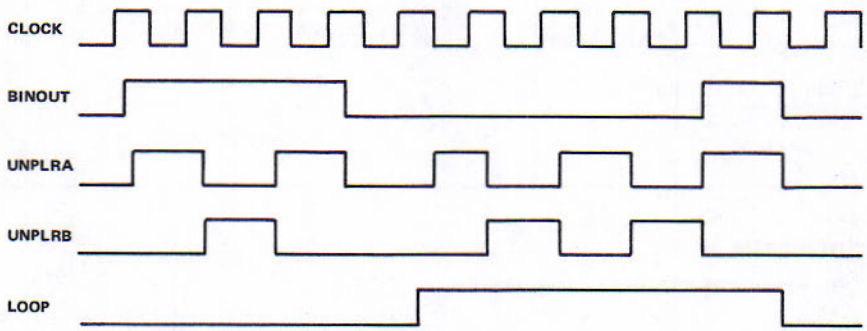



Figure 3. T-1 Transmitter Binary, Unipolar Format

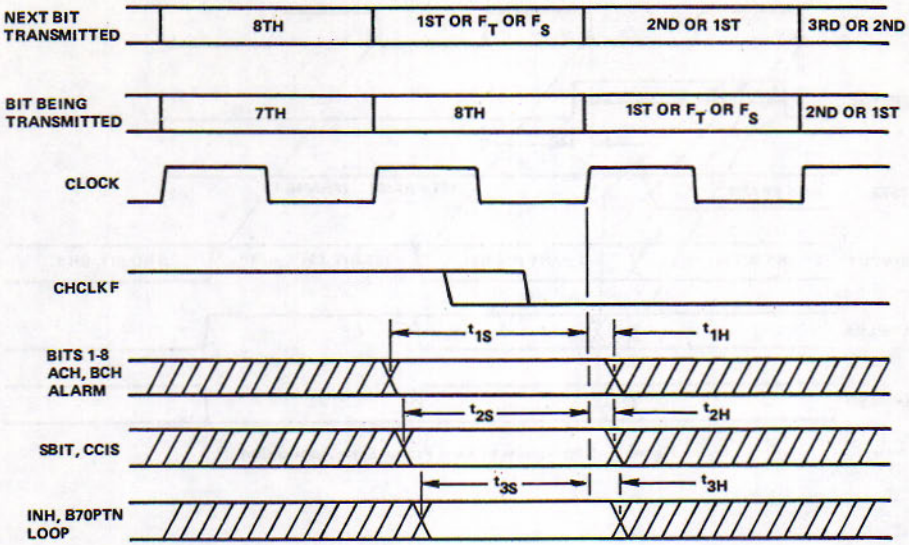



Figure 4. Input Timing Relationships

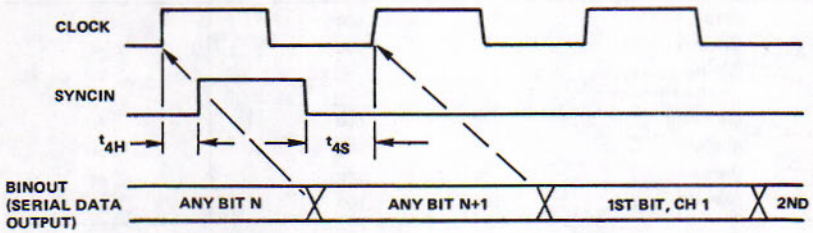



Figure 5. SYNCIN Timing Relationship

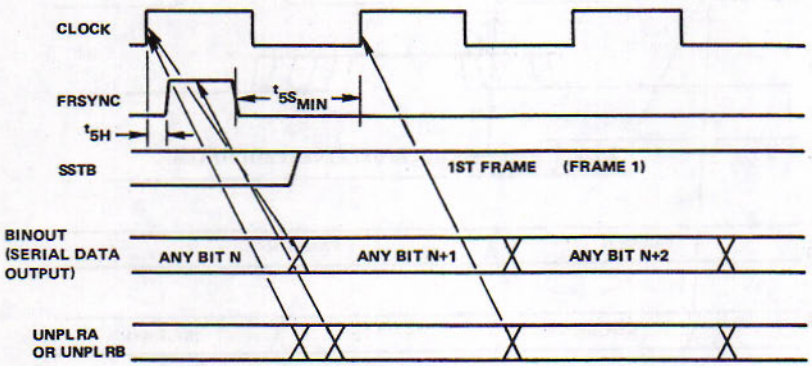



Figure 6. Return to Zero Frame Sync Application

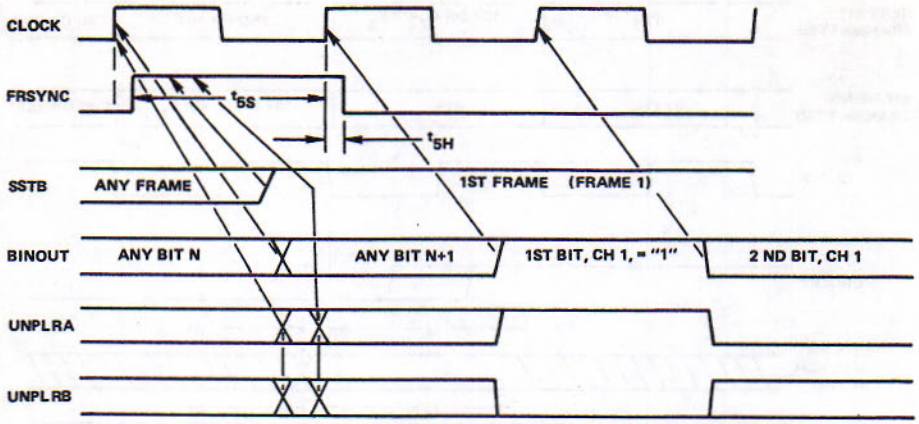



Figure 7. Non-Return to Zero Frame Sync Application

Table 4. Output Propagation Delay, Worst Case (Measured from Rising Edge of Clock Unless, Stated Otherwise)

| OUTPUT | MAX DELAY | UNIT |
|---|---|---|
| SSTB | 500 | ns |
| SYNOUT | 500 | ns |
| Ref from Falling Edge of Clock | | |
| CHCLKF | 500 | ns |
| BINOUT | 500 | ns |
| UNPLRA | 500 | ns |
| UNPLRB | 500 | ns |

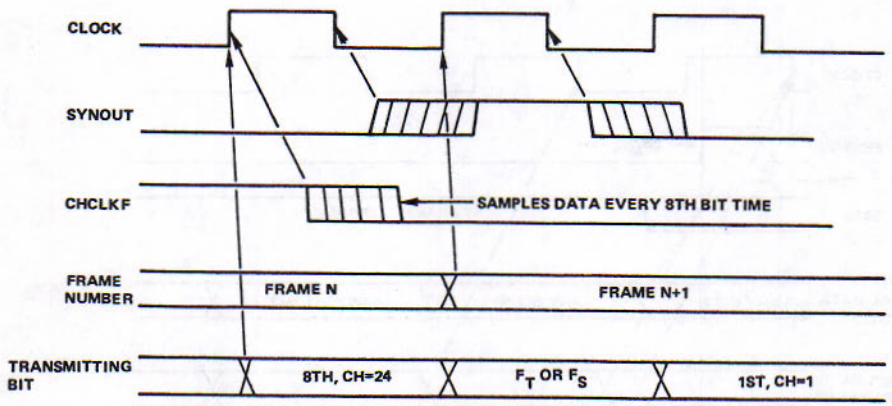



Figure 8. SYNOUT Signal Relationship

## SPECIFICATIONS

### Maximum Ratings

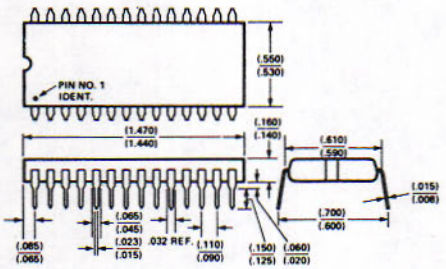
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | +4.5 to +5.5 | Vdc |
| Operating Temperature | $T_{OP}$ | 0 to +70 | °C |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C |

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

### Electrical Characteristics

($V_{DD}$ = 5.0 ±5%)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Logical "1" Input Voltage | $V_{OH}$ | 2.0 | $V_{DD}$ + 0.3 | V |
| Logical "0" Input Voltage | $V_{IL}$ | -0.3 | 0.8 | V |
| Logical "1" Output Voltage | $V_{OH}$ | 2.4 | – | V |
| Logical "0" Output Voltage | $V_{OL}$ | – | 0.4 | V |
| Output Source Current | $I_{OH}$ | -100 | – | μA |
| Output Sink Current | $I_{OL}$ | 400 | – | μA |
| Capacitance Load | C | – | 25 | pF |
| Input Capacitance (any input) | $C_{IN}$ | – | 5 | pF |
| Clock Frequency | | – | 1.6 | MHz |
| Power Dissipation | $P_D$ | – | 250 | mw |




Packaging Diagram

DOCUMENT NO. R8060D
APRIL 1979

PART NUMBER
R8060

Rockwell

# MOS/LSI TELECOMMUNICATIONS DEVICES
## DATA SHEET

# T-1 SERIAL RECEIVER

## DESCRIPTION

The Rockwell T-1 Receiver processes serial unipolar data of a T-1, D2 or T-1, D3 line from which data and a 1.544 MHz clock have been extracted.

Frame synchronization is accomplished by locating the frame bit ($F_T$) alternating every 386 bits. Loss of frame sync is indicated if a frame bit error occurs within two to four F-Bit frames since the previous frame bit error.

A loss of carrier is indicated if 31 consecutive bit times yield "zeros" at the input. Carrier loss is reset and frame sync search begins when a "one" reappears at the TDATA input.

Signaling bits, which occur 193 bit positions after a framing bit, are monitored to detect signaling frames. The signaling frame output, SIGFR, identifies the present frame as a signaling frame, and the S-Bit output at that time identifies which signaling frame is being processed.

Remote alarm reporting is detected by monitoring the second received bit of every channel sample of every frame. An alarm is indicated if 255 consecutive Bit 2 zeros are received.

Channel data bits are output by an eight-bit parallel register. The rising edge of the signal called channel clock (CHCLK) indicates the extraction of new output channel data.

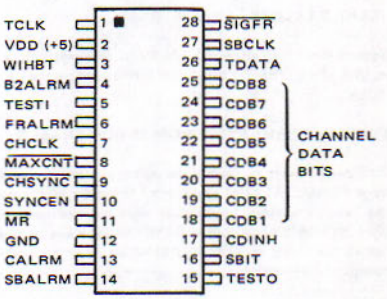
Several signals developed from a MOD 386 counter are provided to aid in the external processing and storage of channel data. Signals are provided to increment counters, synchronize counters, strobe data into memories, etc.

The Rockwell T-1 Receiver chip operates on a single 5 volt supply and directly interfaces to the low power TTL Schottky logic family. The Receiver is packaged in a 28 pin dual in-line (DIP).

Timing relationships are given in figures 3 through 5.

## FEATURES

- Synchronizes serial T-1, D2 or T-1, D3 signals in less than 5 ms.
- Extracts 8-bit parallel channel data
- Provides timing signals to capture and synchronize channel and frame information
- Monitors and detects
  - Errors in signaling bit pattern
  - Loss of frame sync
  - Loss of carrier
  - Remote alarm reporting
- Single 5V supply
- LPTTL Schottky compatible




**Pin Configuration**

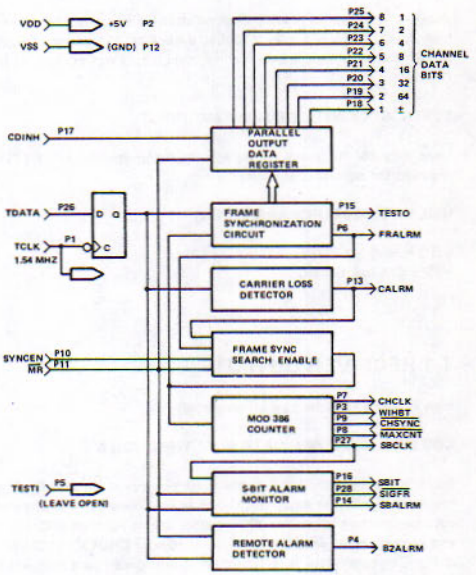



**Figure 1. R8060 Block Diagram**





Specifications subject to change without notice

## T-1 RECEIVER INPUTS

Any input ≤0.8V = LOGIC 0, LOW, ZERO. Any input ≥2.0V = LOGIC 1, HIGH, ONE. A transition from a low level to a high level is called a rising edge, while the converse is true for the falling edge.

**TDATA: UNIPOLAR T-1-D2, T-1-D3 SERIAL DATA INPUT**

Unipolar T-1 Data is clocked in on the falling edge of TCLK. Thereafter, TDATA is processed on the rising edge of TCLK. TDATA must be stable 100 ns before and remain stable 100 ns after the falling edge of TCLK.

**TCLK: T-1 CLOCK**

Typical clock frequency is 1.544 MHz. Maximum clock frequency is 1.85 MHz. The T-1 bit period is bounded by the rising edges of TCLK.

**SYNCEN: FRAME SYNCHRONIZATION ENABLE**

Provides a means to disable the automatic resync search initiated by a FRAME ALARM condition. If the SYNCEN signal is low, the synchronization function is inhibited and remains inhibited until SYNCEN transitions high. SYNCEN must be stable 200 ns before the rising edge of FRALRM, in order to inhibit the synchronization function.

**MR: MASTER RESET**

Master Reset, when low, performs an initialization clear of the T-1 Receiver; SBALRM and CALRM are reset to low levels while FRALRM, CHCLK, WIHBT and CHSYNC are set to high levels. Frame synchronization search begins on the rising edge of $\overline{MR}$ provided that SYNCEN signal has been high for 200 ns. Minimum pulse width is one T-1 clock period.

**CDINH: CHANNEL DATA INHIBIT**

Provides a means to disable channel data bit outputs. When at a high level, CDINH forces channel data Bits 1 through 7 high. Bit 8, the least significant channel data bit, is not controlled by CDINH.

**TESTI: ROCKWELL DEVICE TEST INPUT**

Used only for Rockwell device testing, no connection to TESTI is required for normal operation.

**VSS, VDD: GROUND AND POWER**

VDD = +5.0 ±0.5 VDC
VSS = Ground, 0 VDC

## T-1 RECEIVER OUTPUTS

Low Power TTL Schottky – compatible

**CDB (1-8): CHANNEL DATA BIT 1 THROUGH 8**

Bit 1 is the sign bit, Bit 2 is the most significant bit and Bit 8 is the least significant bit. If CDINH is low, new parallel channel data becomes valid within 200 ns after the rising edge of CHCLK and remains valid until the next rising edge of CHCLK. If CDINH is high, channel data Bits 1 through 7 are forced to a high level. Bit 8, the least significant bit, is not controlled by CDINH. Channel data Bits 1 through 7 are enabled or disabled within 150 ns by CDINH. Refer to Figures 3 through 5.

**CHCLK – CHANNEL CLOCK**

The rising edge of CHCLK indicates a change of parallel output channel data. CHCLK is four TCLKS high then four TCLKS low except for when an "F" or "S" bit is received. Then CHCLK stretches to five TCLKS high and four TCLKS low. Refer to Figures 3 and 4.

**$\overline{CHSYNC}$: CHANNEL SYNC**

Channel Sync occurs one time in a 24 channel period, making it suitable for synchronizing external counters to the T-1 Frame rate. $\overline{CHSYNC}$ goes low one TCLK period before the rising edge of CHCLK at channel 24 data sample time. $\overline{CHSYNC}$ returns high 1 TCLK period after the rising edge of CHCLK. Refer to Figures 3 through 5.

**TESTO: ROCKWELL DEVICE TEST OUTPUT**

Designed to aid in Rockwell device testing. No connection required for normal operation.

**WIHBT: WRITE INHIBIT**

WIHBT covers the parallel channel data transition period. WIHBT is suitable for clocking or strobing channel data into external memories. WIHBT is high for two TCLK periods, beginning one TCLK period before the rising edge of CHCLK. Refer to Figures 3 and 4.

**$\overline{MAXCNT}$: MAXIMUM COUNT OF 386 MODULOUS**

$\overline{MAXCNT}$ is low for one TCLK period, marking the completion of a two-frame period corresponding to the expected receipt of an F-bit at the TDATA input. Refer to Figures 4 and 5.

**SBCLK: S-BIT CLOCK**

SBCLK will be high during the S-Bit frame and low during the F-bit frame. The transitions will occur within 300 ns after the rising edge of TCLK as channel 24 data is being transferred to the parallel channel outputs. Refer to Figures 3 through 5.

**S-BIT: SIGNALING BIT OUTPUT**

The S-Bit output monitors the previous S-Bit received which occurred two frames before the receipt of the current S-Bit. An S-Bit output transition occurs one TCLK period after the rising edge of SBCLK.

During a signaling frame (SIGFR is low), channel 6 or "A" highway signaling is identified by S-Bit output being low. If S-Bit is high during a signaling frame, channel 12 or "B" highway signaling is identified. Refer to Figures 3 through 5.

**$\overline{SIGFR}$: SIGNALING FRAME**

$\overline{SIGFR}$ identifies frame 6 or 12 when low. If the sequence of five consecutive received S-Bits is either 0111X or 1X001 (left to right, as received), $\overline{SIGFR}$ shall go low after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time. $\overline{SIGFR}$ returns high one frame later (193 bits). Refer to Figures 3 through 5.

**SBALRM: S-BIT ALARM**

SBALRM goes high if the sequence of five S-Bits received contains four consecutive ones (01111), and remains high until three consecutive "zero" bits are preceded and followed by a "one" S-Bit (10001). The actual transition of SBALRM output occurs after the rising edge, but at least 375 ns before the falling edge of WIHBT corresponding to channel 1 data sample time.

**B2ALRM: BIT 2 ALARM**

B2ALRM goes high, detecting a remote alarm condition, if 255 consecutive channel data samples are received with Bit 2 low. B2ALRM returns high upon the receipt of any channel sample with Bit 2 high.

**CALRM: CARRIER LOSS ALARM**

A carrier loss is detected and CALRM is set high if 31 consecutive low level TDATA bits are received. CALRM is reset low, FRALRM is set high and frame sync search begins when the first TDATA high level is received.

**FRALRM: FRAME ERROR ALARM**

FRALRM detects an out-of-frame condition. FRALRM goes high if:

A) The framing synchronization function is in progress.
B) Within 250 ns after the falling edge of MR.
C) An F-Bit is received which is not the inverse of the last F-Bit and the same condition also occurred two or three or four F-Bit frames earlier.
D) Within 250 ns after the falling edge of CALRM, (CALRM being reset by high level TDATA bit).

FRALRM goes low upon completion of the synchronization function or within 250 ns after the rising edge of CALRM. (Carrier loss condition during frame synchronization function).

**OUTPUT CLOCK SIGNALS DURING FRAME SYNCHRONIZATION FUNCTION**

Following the Declaration of Frame Sync loss (FRALRM goes high), output signals will continue normally for a two-frame period with the exception of CHSYNC, which has the above mentioned second frame sync pulse inhibited. Following the two-frame period CHCLK, CHSYNC, and WIHBT are held high until frame sync has been located, as indicated by the falling edge of FRALRM. Frame synchronization takes less than five milliseconds. See Figure 2.

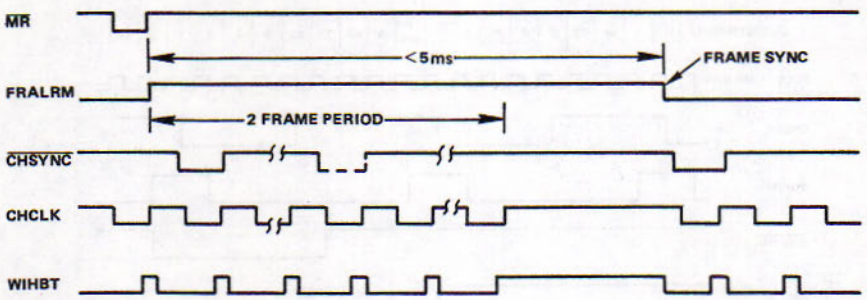



**Figure 2. Signal Relationship During Frame Alarm and Search for Resynchronization**

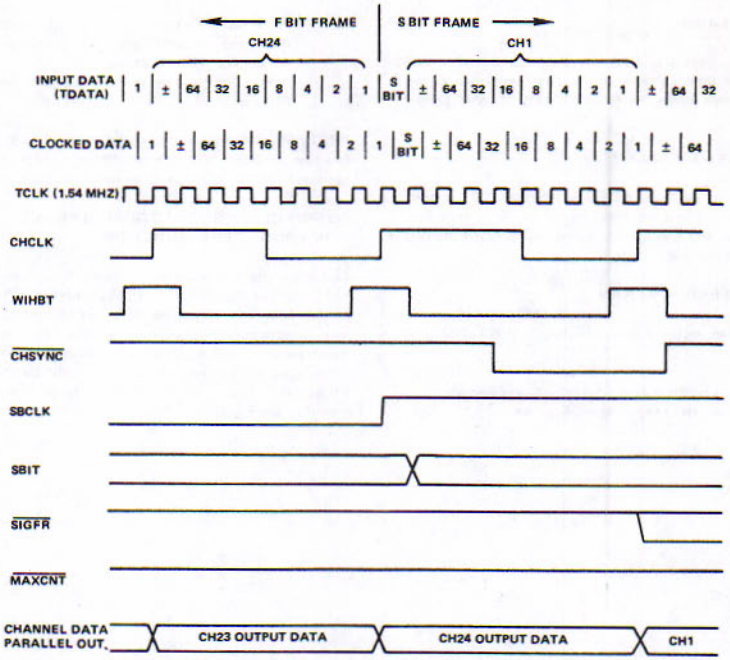



Figure 3. Signal Relationships at Beginning of $F_S$ Frame (S-BIT)

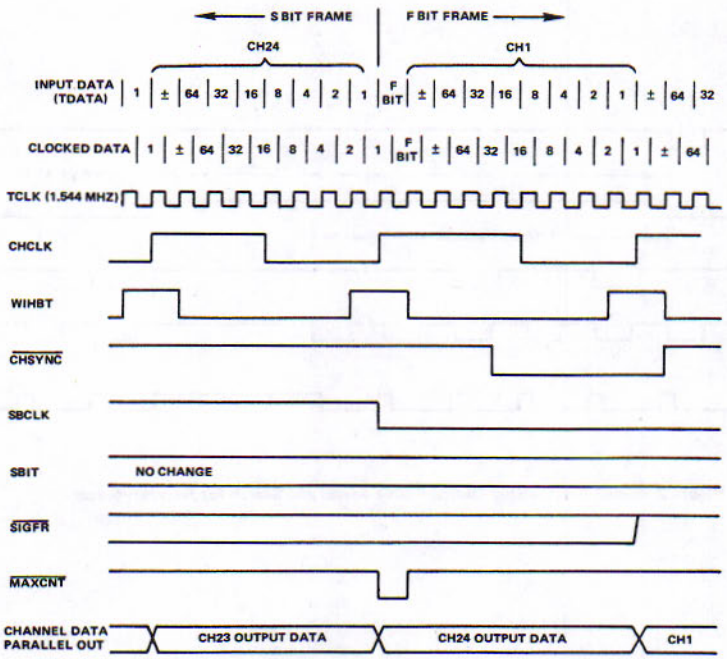
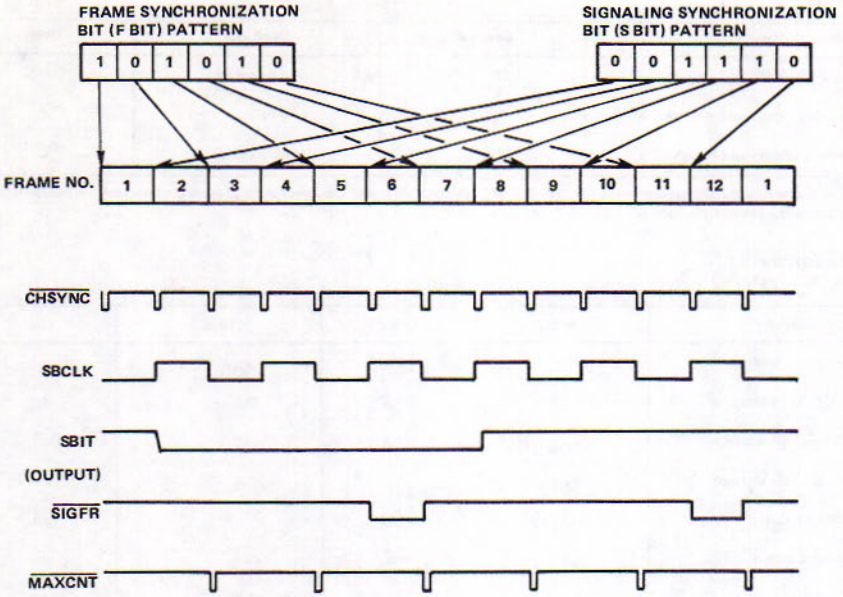



Figure 4. Signal Relationships at Beginning of $F_T$ Frame (F-BIT)




FRAME = 24 TIME SLOTS = 193 BITS = 125μS
TIME SLOT = 5.18μS ONE BIT = 648 μS
MULTIFRAME = 12 FRAMES = 1.5 MS.

F BIT ($F_T$) FRAME ALIGNMENT SIGNAL
(ODD-NUMBERED FRAMES)

| FRAME | FIRST BIT |
|---|---|
| 1 | 1 |
| 3 | 0 |
| 5 | 1 |
| 7 | 0 |
| 9 | 1 |
| 11 | 0 |

S BIT ($F_S$) MULTIFRAME ALIGNMENT SIGNAL
(EVEN-NUMBERED FRAMES)

| FRAME | FIRST BIT |
|---|---|
| 2 | 0 |
| 4 | 0 |
| 6 | 1 |
| 8 | 1 |
| 10 | 1 |
| 12 | 0 |

Figure 5. Multiframe Signal Relationships

Table 1. Output Propagation Delay Worst Case, From Rising Edge to TCLK

| OUTPUT | MAX DELAY | UNIT |
|---|---|---|
| CHCLK | 300 | NS |
| $\overline{\text{CHSYNC}}$ | 300 | NS |
| WIHBT | 300 | NS |
| $\overline{\text{MAXCNT}}$ | 300 | NS |
| SBCLK | 300 | NS |
| SBIT | 400 | NS |
| $\overline{\text{SIGFR}}$ | 475 | NS |
| SBALRM | 475 | NS |
| B2ALRM | 450 | NS |
| CALRM | 300 | NS |
| FRALRM | 600 | NS |
| CDB (1-8) | 400 | NS |

## SPECIFICATIONS

### Maximum Ratings

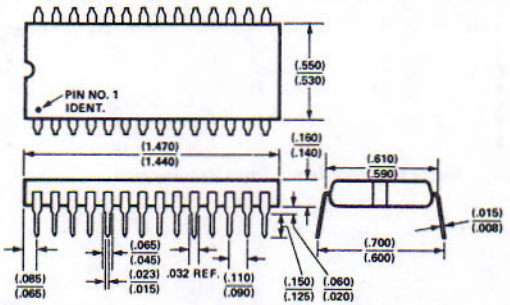
| Rating | Symbol | Voltage | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | +4.5 to +5.5 | V |
| Operating Temperature Range | $T_{OP}$ | 0 to 70 | °C |
| Storage Temperature Range | $T_{STG}$ | -55 to +150 | °C |

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

### Electrical Characteristics

$V_{DD}$ = +5V ±10%, $T_A$ = 25°C)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Logic "1" Voltage | $V_{IH}$ | 2.0 | $V_{DD}$ + 0.3 | V |
| Input Logic "0" Voltage | $V_{IL}$ | -0.3 | 0.8 | V |
| Output Logic "1" Voltage | $V_{OH}$ | 2.4 | | V |
| Output Logic "0" Voltage | $V_{OL}$ | | 0.4 | V |
| Output Source Current | $I_{OH}$ | -100 | | μA |
| Output Sink Current | $I_{OL}$ | 400 | | μA |
| Clock Frequency | $T_{CLK}$ | | 1.85 | MHz |
| Input Capacitance | $C_I$ | | 5 | pF |
| Output Capacitance | $C_O$ | | 25 | pF |
| Power Dissipation | $P_{DSS}$ | | 550 | mW |




Packaging Diagram

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May, 1979

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